# Certification of Design, Construction and Qualification

| Supplier Name: Texas Instruments | Date: 11/18/2021 |
|---|---|

| | Item Name | Supplier Response |
|---|---|---|
| 1. | User's Part Number: | SN74LVC1G97QDCKRQ1 |
| 2. | Supplier's Part Number / Data Sheet: | SN74LVC1G97QDCKRQ1 SCES561D |
| 3. | Device Description: | CONFIGURABLE MULTIPLE-FUNCTION GATE |
| 4 | Wafer/Die Fab Location & Process ID: | |
| | a. Facility name / plant #: | FFAB |
| | b. Street address: | Haggertystrasse 1, Freising Bayern, Germany 85356 |
| | c. Country: | Germany |
| 5. | Wafer Probe Location: | |
| | a. Facility name / plant #: | FFAB |
| | b. Street address: | Haggertystrasse 1, Freising Bayern, Germany 85356 |
| | c. Country: | Germany |
| 6. | Assembly Location & Process ID: | |
| | a. Facility name / plant #: | HEFEI TONGFU MICROELECTRONICS (HFTFAT) |
| | b. Street address: | No.578, Wei Xin Road, Economic -Technological Development, Hefei |
| | c. Country: | China |
| 7. | Final Quality Control A (Test) Location: | |
| | a. Facility name / plant #: | HEFEI TONGFU MICROELECTRONICS (HFTFAT) |
| | b. Street address: | No.578, Wei Xin Road, Economic -Technological Development, Hefei |
| | c. Country: | China |
| 8. | Wafer / Die: | |
| | a. Wafer size: | 200mm |
| | b. Die family: | RLVC1G97IZ |
| | c. Die mask set revision & name: | - 1G97 |
| | d. Die photo: | See attached ☐ Not available ☑ |
| 9. | Wafer / Die Technology Description: | |
| | a. Wafer / Die process technology: | ASL3C |
| | b. Die channel length: | 0.671UM |
| | c. Die gate length: | 0.671UM |
| | d. Die supplier process ID (Mask #) | 1LVC1G98IZX |
| | e. Number of transistors or gates | TI Information - NDA Restrictions |
| | f. Number of mask steps | TI Information - NDA Restrictions |
| 10. | Die Dimensions: | |
| | a. Die width: | 18.90 |
| | b. Die length: | 25.91 |
| | c. Die thickness (finished): | 7.5 MILS WAFER |
| 11. | Die Metallization: | |
| | a. Die metallization material(s): | TiW/Al Cu |
| | b. Number of layers: | 2 |
| | c. Thickness (per layer): | TiW 2000 \| 6000A Al Cu (2%) |
| | d. % of alloys (if present): | Cu 2% |
| 12. | Die Passivation: | |
| | a. Number of passivation layers: | 1 |
| | b. Die passivation material(s): | Nitride |
| | c. Thickness(es) and tolerances: | 10kA nominal |
| 13. | Die Overcoat Material (e.g. Polymide) | |
| 14. | Die Cross-Section Photo / Drawing: | See attached ☐ Not available ☑ |
| 15. | Die Prep Backside: | |
| | a. Die prep method: | Backgrind |
| | b. Die metallization: | None |
| | c. Thickness(es) and tolerances: | 7.5 MILS WAFER |

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| 16. Die Separation Method: | |
| a. Kerf width (µm): | N/A |
| b. Kerf depth (if not 100% saw): | 100% |
| c. Saw method: | Single ☑ Dual ☐ |
| 17. Die Attach: | |
| a. Die attach material ID: | ABLEBOND SID# A-03 |
| b. Die attach method: | Epoxy Dispense |
| c. Die placement diagram: | See attached ☐ Not available ☑ |
| 18. Package | |
| a. Type of package: | SOT DCK |
| b. Ball/lead count | 6 |
| c. JEDEC designation: | MO-203(AB) |
| d. Lead (Pb) free: | Yes ☑ No ☐ |
| e. Package outline drawing: | See attached ☐ Not available ☑ |
| 19. Mold Compound: | |
| a. Mold compound supplier and ID | Hitachi SID#R-27 |
| b. Mold compound type | Ion trapper version |
| c. Flammability rating | UL 94 V1 ☐ UL 94 V0 ☑ |
| d. Fire retardant type / composition: | None (self extinguishing resin) |
| e. Environmentally green | Yes |
| f. CTE (ppm / °C) ( (a)bove and (b)elow Tg ) | CTE (a): 40 CTE (b): 10 |
| 20. Wire Bond: | |
| a. Wire bond material: | Au |
| b. Wire bond diameter (mils): | 20.3 UM (0.8 MIL) |
| c. Type of wire bond at die: | Thermosonic Ball Bond |
| d. Type of wire bond at leadframe: | Thermosonic Stitch Bond |
| e. Wire bonding diagram | See attached ☐ Not available ☑ |
| 21. Leadframe: | |
| a. Paddle / flag material: | Cu Alloy |
| b. Paddle / flag width (mils): | 28.7 |
| c. Paddle / flag length (mils): | 36.6 |
| d. Paddle / flag plating composition: | None |
| e. Paddle/flag plating thickness (µin) | NA |
| f. Leadframe material: | Cu |
| g. Leadframe bonding plating composition: | Ag |
| h. Leadframe bonding plating thickness (µin): | 50 – 150 micro inches (1.27 – 3.81 um) |
| i. External lead plating composition: | Sn |
| j. External lead plating thickness (µin) | 275 – 787 u-in (7 – 20 um) |
| 22. Substrate (if applicable): | |
| a. Substrate material: | N/A |
| b. Substrate thickness (mm): | N/A |
| c. Number of substrate metal layers: | N/A |
| d. Plating composition of ball solderable surface | N/A |
| e. Panel singulation method: | N/A |
| f. Solder ball composition: | N/A |
| g. Solder ball diameter (mils): | N/A |
| 23. Unpackaged Die (if not packaged): | |
| a. Under Bump Metallurgy (UBM) composition: | N/A |
| b. Thickness of UBM metal: | N/A |
| c. Bump composition: | N/A |
| d. Bump size: | N/A |
| 24. Header Material (if applicable): | |

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| 25. Thermal Resistance<br>a. $\Theta_{JA}$ °C/W (approx)<br>b. $\Theta_{JC}$ °C/W (approx)<br>c. Special thermal dissipation construction techniques | @ 0 LFM High K:239.1<br>Top 114.1 Bottom (Exposed Pad) NA |
| 26. Test circuits, bias(es), and operational conditions imposed during the supplier's life and environmental tests | Not provided |
| 27. Fault Grade Coverage ( % ) | Not digital circuitry |
| 28. Maximum Process Exposure Conditions:<br>a. MSL @ rated SnPb temperature:<br>b. MSL @ rated Pb-free temperature:<br>c. Maximum dwell time @ maximum process temperature | *Temperatures measured on the center of plastic package body top surface.<br>at °C (SnPb)<br>1 at 260 °C (Pb-free)<br>Per IPC/JEDEC J-STD-020D; Time within 5 °C of the specified classification temperature; Sn-Pb Eutectic Assembly-20 seconds maximum; Pb-Free Assembly 30 seconds maximum |

| Attachments | | Requirements |
|---|---|---|
| Die Photo | ☐ | 1. A separate Design, Construction & Qualification must be submitted for each P/N, wafer fab, and assembly location. |
| Package Outline Drawing | ☐ | |
| Die Cross-Section Drawing | ☐ | 2. Design, Construction & Qualification shall be signed by the individual responsible at the supplier who can verify the above information is accurate an complete. Type name and sign below. |
| Wire & Die Placement Diagram | ☐ | |
| Test Circuits, Bias Levels, & Conditions | ☐ | |

| Completed by: | | Certified by: | |
|---|---|---|---|
| Date: | 11/18/2021 | Date: | 12/30/2014 |
| Name: | Muhammad Amirudin | Name: | Julia Streltsova |
| Signature: | Amir | Signature: | |
| Title: | Product Engineer | Title: | CQE |