

Quad Flatpack No-Lead Logic Packages

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ABSTRACT

Texas Instruments (TI) Quad Flatpack No-lead (QFN) 14/16/20-terminal Pb-free plastic packages meet dimensions specified in JEDEC standard MO-241, allow for board miniaturization, and hold several advantages over traditional SOIC, SSOP, TSSOP, and TVSOP packages. The packages are physically smaller, have a smaller routing area, improved thermal performance, and improved electrical parasitics, while giving customers a pinout scheme that is consistent with the previously mentioned packages. Additionally, the absence of external leads eliminates bent-lead concerns and issues. These QFN packages have reliable solderability with either SnPb or Pb-free solder paste and are packaged to industry-standard tape-and-reel specifications. Package marking is in accordance with TI standards.

Contents

1	Introduction	4
	1.1 Product Offerings.....	4
2	Physical Description	5
	2.1 Package Characteristics	5
	2.2 QFN Pinout	11
	2.3 Package Nomenclature	12
	2.4 Power Dissipation	12
	2.5 Electrical	21
	2.6 Board-Level Reliability	24
3	Board-Level Assembly	25
	3.1 PCB Design Guidelines	25
	3.2 PCB Land-Pattern Design	26
	3.3 Stencil Design.....	29
	3.4 Component Placement and Reflow	31
	3.5 Rework.....	34
4	Tape-and-Reel Packing	35
	4.1 Material Specifications.....	35
	4.2 Labels	38
	4.3 Dry-Pack Requirements for Moisture-Sensitive Material	40
	4.3.1 Symbols and Labels.....	42
5	Symbolization	44
6	Test Sockets	44
7	Features and Benefits	45
8	Conclusion	45
9	Acknowledgments	45
10	References	46

Figures

Figure 1. Cross Section of a Generic QFN Package	5
Figure 2. 14-Pin QFN Package Dimensions	6
Figure 3. 16-Pin QFN Package Dimensions	7
Figure 4. 20-Pin QFN Package Dimensions	8
Figure 5. 20-Pin QFN Comparison to Alternative Package Solutions.....	9
Figure 6. 16-Pin QFN Comparison to Alternative Package Solutions.....	10
Figure 7. 14-Pin QFN Comparison to Alternative Package Solutions.....	10
Figure 8. 20-Pin QFN Package Standard Pinout.....	11
Figure 9. 14-Pin QFN Package Standard Pinout.....	12
Figure 10. 20-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card	15
Figure 11. 16-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card	15
Figure 12. 14-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card	16
Figure 13. The Effect of Board Layers and Vias on 20-Pin QFN Power Dissipation (JEDEC Test Cards and Zero Airflow)	16
Figure 14. Effect of Board Layers and Vias on θ_{JA} (JESD 51-3 vs JESD 51-5).....	17
Figure 15. Effect of Board Layers and Vias on θ_{JA} (JESD 51-7 vs JESD 51-5).....	17
Figure 16. Modeled θ_{JA} vs Number of Thermal Vias on JESD 51-5 Test Card (20-Pin QFN)	18
Figure 17. Modeled Thermal Impedance of 20-Pin QFN vs Alternative Packaging.....	19
Figure 18. Modeled Thermal Impedance of 16-Pin QFN vs Alternative Packaging.....	19
Figure 19. Modeled Thermal Impedance of 14-Pin QFN vs Alternative Packaging.....	20
Figure 20. Modeled 20-Pin Package-Parasitics Comparison	22
Figure 21. Modeled 16-Pin Package-Parasitics Comparison	23
Figure 22. Modeled 14-Pin Package-Parasitics Comparison	23
Figure 23. Critical Dimensions of 14-Pin QFN Package Land Pad.....	25
Figure 24. Cross Section of QFN Terminal-Land-Pad Geometry	26
Figure 25. Recommended PCB Land-Pad Design for 20-Pin QFN Package	27
Figure 26. Recommended PCB Land-Pad Design for 16-Pin QFN Package	28
Figure 27. Recommended PCB Land-Pad Design for 14-Pin QFN Package	28
Figure 28. Stencil-Design Recommendation for 20-Pin QFN Package	30
Figure 29. Stencil-Design Recommendation for 16-Pin QFN Package	30
Figure 30. Stencil-Design Recommendation for 14-Pin QFN Package	31
Figure 31. Pb-Free-Paste Reflow Profile	32
Figure 32. Generic SnPb Reflow Profile	33
Figure 33. Carrier-Tape Dimensions	36
Figure 34. Reel Specifications	37
Figure 35. Carrier-Tape Cavity Quadrant Location for Pin 1, Per EIA-481B	37
Figure 36. Pin-1 Orientation of QFN Packages in Carrier Tape	38
Figure 37. Reel Labeling.....	38
Figure 38. Regular Shipping-Box Label Placement.....	39
Figure 39. Label Placement On Shipping Box with Flap	39
Figure 40. Child-Lot Label Placement on Shipping-Box Label Flap	39
Figure 41. Humidity Indicator Card	40
Figure 42. Label Placement on Tape-and-Reel Moisture-Barrier Bag.....	41
Figure 43. Moisture-Sensitivity Symbol	42
Figure 44. MSID Label.....	42
Figure 45. Moisture-Sensitivity Caution Label for Levels 2–5a.....	43

Tables

Table 1.	Product Technology Families for 14-, 16-, and 20-Pin QFN Packages	4
Table 2.	QFN Package Physical Attributes.....	5
Table 3.	Modeled 20-Pin QFN Thermal-Impedance Values.....	13
Table 4.	Modeled 16-Pin QFN Thermal-Impedance Values.....	14
Table 5.	Modeled 14-Pin QFN Thermal-Impedance Values.....	14
Table 6.	Modeled 20-Pin QFN Package-Parasitics Comparison.....	21
Table 7.	Modeled 16-Pin QFN Package-Parasitics Comparison.....	21
Table 8.	Modeled 14-Pin QFN Package-Parasitics Comparison.....	22
Table 9.	Board-Level Package Shear Values for QFN Packages (n = 19).....	24
Table 10.	Carrier-Tape Dimensions.....	36
Table 11.	Dry-Pack Requirements for MSL Level 1 and Level 2 Packages	40
Table 12.	Floor Life Under Conditions Other Than 30°C and 60% Relative Humidity.....	41
Table 13.	Device-Marking Guidelines.....	44

1 Introduction

As worldwide mobility increases, consumers wanting to "stay connected" in the digital world have demanded smaller and lighter products. Consumer-electronics manufacturers are striving to reduce product size to meet this demand. Smaller, thinner, and thermally enhanced packages help achieve product miniaturization. A performance analysis has shown that quad flatpack no-lead (QFN) packages have better thermal performance than dual in-line surface-mount technology (SMT) packages. Other benefits of the QFN packages are low inductance and capacitance, small package volume, smaller board routing area, and no external leads, compared to conventional leaded packages. Texas Instruments (TI) has chosen the QFN packages as one of the vehicles that allows electronic-component manufacturers to achieve product miniaturization.

QFN packages of 14-, 16-, and 20-pins will be offered in many logic or linear product families, as defined in Section 1.1, *Product Offerings*. This package is ideal for space-constrained products such as cellular, DVD/CD players, MP3 players, VCRs, digital STB, DSC, notebook computers, PC cards, and personal digital assistants (PDAs). These packages also are best suited for products with increased thermal and electrical requirements.

The QFN packages are depopulated and dimensionally align with JEDEC standard MO-241.[1] The package construction allows the pinout to remain consistent with current SOIC, SSOP, TSSOP, and TVSOP packages. Package features, characteristics, and performance are defined in this application report.

1.1 Product Offerings

Table 1 shows the product families to be offered initially in 14-, 16-, and 20-pin QFN packages. Available functions are too numerous to list. Additionally, based on customer demand, the product-family list is expected to grow. Please see the TI website at www.ti.com for the latest list of product families and functions.

Table 1. Product Technology Families for 14-, 16-, and 20-Pin QFN Packages

Family	Description	Pins
ABT	Advanced BiCMOS Technology	14, 20
AHC/AHCT	Advanced High-Speed CMOS	14, 16
ALVC	Advanced Low-Voltage CMOS Technology	14
CBT	Crossbar Technology	14, 16, 20
CBTLV	Low-Voltage Crossbar Technology	14, 16, 20
GTLP	Gunning-Transceiver Logic Plus	16
LV	Low-Voltage HCMOS Technology	14, 16, 20
LVC	Low-Voltage CMOS Technology	14, 16, 20
LVT	Low-Voltage BiCMOS Technology	14, 20

2 Physical Description

2.1 Package Characteristics

Figure 1 shows the cross section of a generic QFN package.

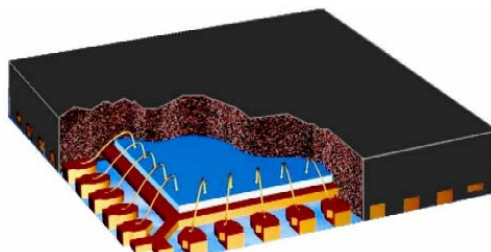
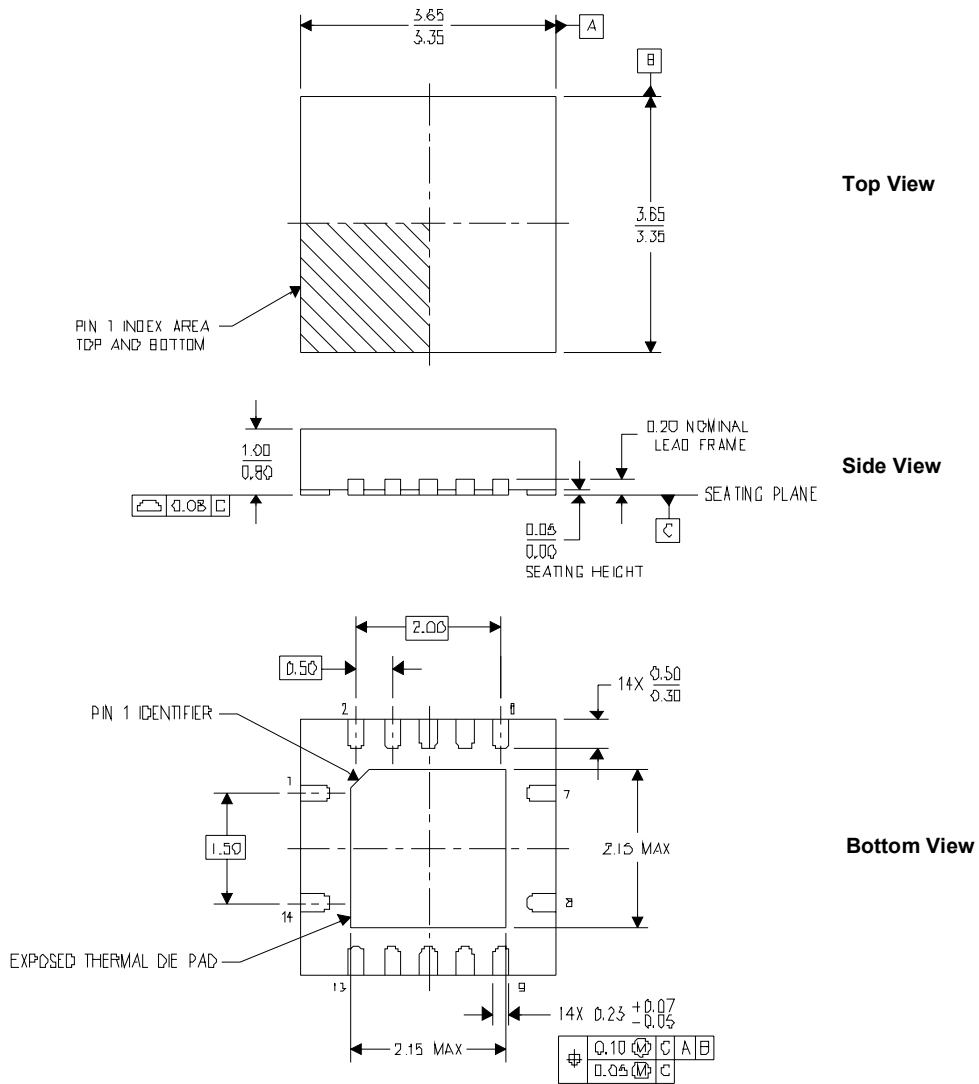


Figure 1. Cross Section of a Generic QFN Package

Table 2 summarizes the package attributes for the 14-, 16-, and 20-pin QFN packages. Figures 2, 3, and 4 show dimensions on package outline drawings.

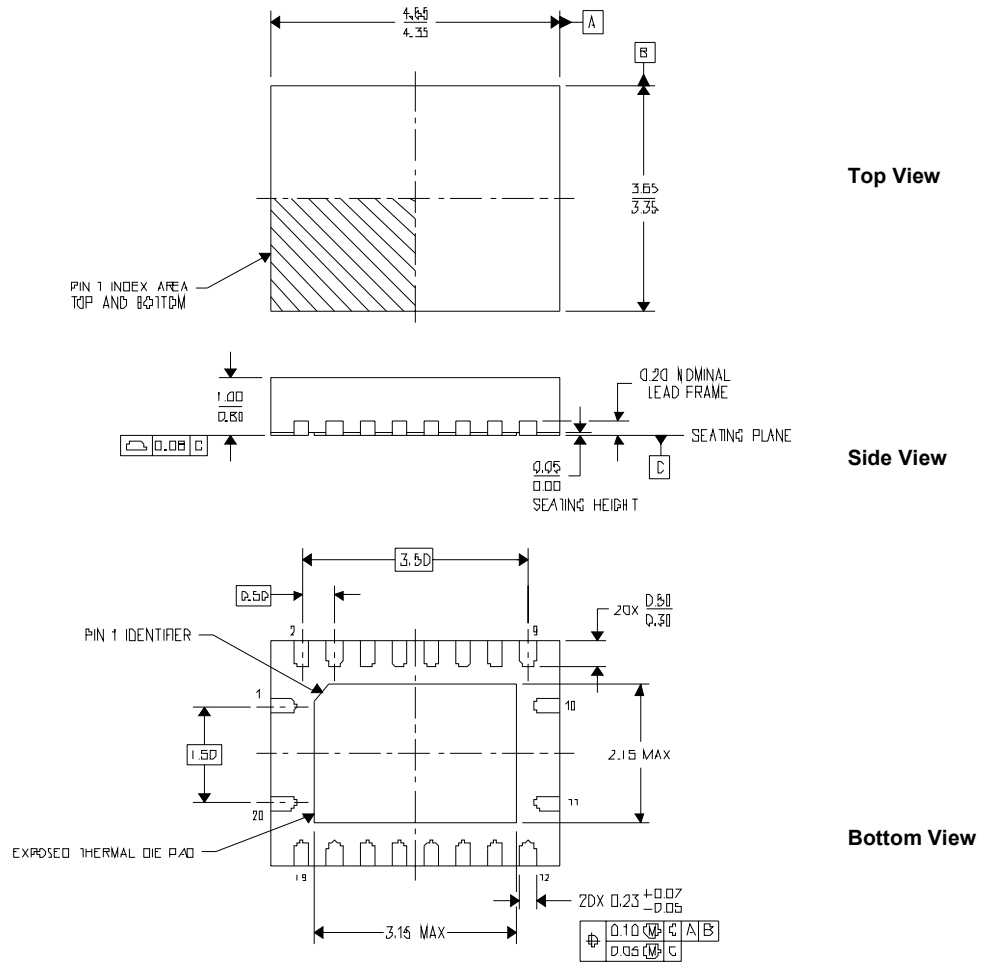
Table 2. QFN Package Physical Attributes

Attribute	QFN-14	QFN-16	QFN-20
Pin count	14	16	20
Square/rectangular	Square	Rectangular	Rectangular
Package length, mm nominal	3.5	4.0	4.5
Package width, mm nominal	3.5	3.5	3.5
Lead finger length, mm nominal	0.4	0.4	0.4
Lead finger width, mm nominal	0.23	0.23	0.23
Exposed pad length, mm max.	2.15	2.65	3.15
Exposed pad width, mm max.	2.15	2.15	2.15
Thickness, mm nominal	0.90	0.90	0.90
Package weight, g	0.032	0.036	0.043
Lead finish	Matte tin	Matte tin	Matte tin
Shipping media, tape and reel (units per reel)	1000	1000	1000
MSL level	Level 2/260°C	Level 2/260°C	Level 2/260°C



All dimensions are in mm.

Figure 2. 14-Pin QFN Package Dimensions



All dimensions are in mm.

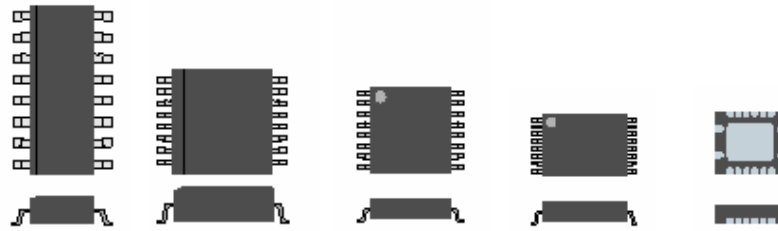
Figure 4. 20-Pin QFN Package Dimensions

Figures 5 through 7 compare the QFN package size, height, and weight to that of alternative package solutions.



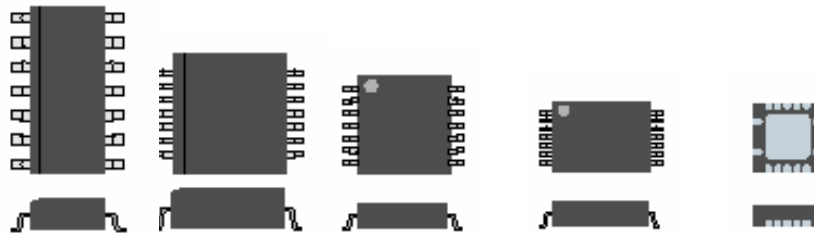
Attribute	SOIC-20 (DW)	SSOP-20 (DB)	TSSOP-20 (PW)	TVSOP-20 (DGV)	QFN-20 (RGY)
Length, mm	12.82 ±0.13	7.20 ±0.30	6.50 ±0.10	5.00 ±0.10	4.50 ±0.15
Width, mm	10.40 ±0.25	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Height, Max. mm	2.65	2.00	1.20	1.20	1.00
Pitch, mm	1.27	0.65	0.65	0.40	0.50
Footprint, mm ²	133.33	56.16	41.60	32.00	15.75
Weight, g	0.495	0.151	0.075	0.055	0.043
Area savings, %	88.19	71.96	62.14	50.78	-

Figure 5. 20-Pin QFN Comparison to Alternative Package Solutions



Attribute	SOIC-16 (D)	SSOP-16 (DB)	TSSOP-16 (PW)	TVSOP-16 (DGV)	QFN-16 (RGY)
Length, mm	9.90 ±0.10	6.20 ±0.30	5.00 ±0.10	3.60 ±0.10	4.00 ±0.15
Width, mm	6.00 ±0.20	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Height, Max. mm	1.75	2.00	1.20	1.20	1.00
Pitch, mm	1.27	0.65	0.65	0.40	0.50
Footprint, mm ²	59.40	48.36	32.00	23.04	14.00
Weight, g	0.150	0.140	0.062	0.040	0.036
Area savings, %	76.43	71.05	56.25	39.24	-

Figure 6. 16-Pin QFN Comparison to Alternative Package Solutions



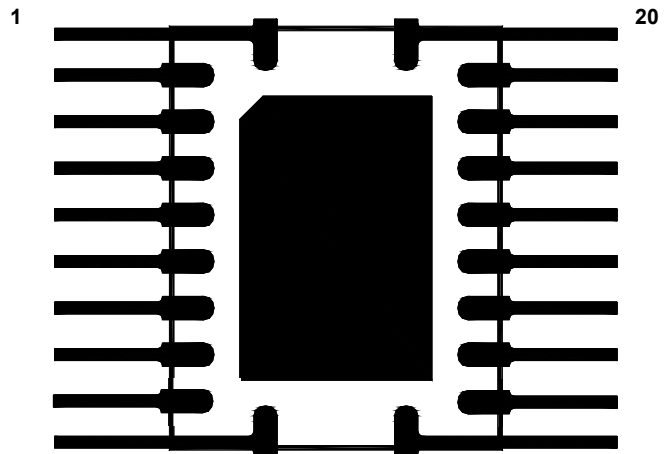
Attribute	SOIC-14 (D)	SSOP-14 (DB)	TSSOP-14 (PW)	TVSOP-14 (DGV)	QFN-14 (RGY)
Length, mm	8.65 ±0.10	6.20 ±0.30	5.00 ±0.10	3.60 ±0.10	3.50 ±0.15
Width, mm	6.00 ±0.20	7.80 ±0.40	6.40 ±0.20	6.40 ±0.20	3.50 ±0.15
Height, Max., mm	1.75	2.00	1.20	1.20	1.00
Pitch, mm	1.27	0.65	0.65	0.40	0.50
Footprint, mm ²	51.90	48.36	32.00	23.04	12.25
Weight, g	0.127	0.122	0.055	0.040	0.032
Area savings, %	76.40	74.67	61.72	46.83	-

Figure 7. 14-Pin QFN Comparison to Alternative Package Solutions

2.2 QFN Pinout

The standard pinout configurations for 14-, 16-, and 20-pin QFN packages resemble the conventional arrangement of 14-, 16-, and 20-pin dual-in-line packages. Figures 8 and 9 show standard QFN pinouts for 14- and 20-pin QFN packages. These pinouts are accurate for most devices; however, some functions vary, especially in the 16-pin package. Please refer to the device data sheet to confirm specific pinouts. Note the flow-through design afforded by the package configuration.

	1 §		20 †	
2 ‡				19 §
3 ‡				18 ‡
4 ‡				17 ‡
5 ‡				16 ‡
6 ‡				15 ‡
7 ‡				14 ‡
8 ‡				13 ‡
9 ‡				12 ‡
				10 ¶



† = V_{CC}

‡ = I/O and Signal

§ = Control

¶ = Ground

NOTES: A. Schematic is not drawn to scale.

B. No ground connection exists through die back side to pad.

Figure 8. 20-Pin QFN Package Standard Pinout

	1 ‡		14 †	
2 ‡				13 ‡
3 ‡				12 ‡
4 ‡				11 ‡
5 ‡				10 ‡
6 ‡				9 §
	7 ¶		8 §	

† = V_{CC}

‡ = I/O and Signal

§ = Control

¶ = Ground

NOTES: A. Schematic is not drawn to scale.

B. No ground connection exists through die back side to pad.

Figure 9. 14-Pin QFN Package Standard Pinout

2.3 Package Nomenclature

These packages are referred to generically in this application report as QFN. The TI package designator for these 14-, 16-, and 20-pin QFN packages is RGY. This common designator refers to these three packages with a common width of 3.5 mm. The designator is extended to RGYR to designate parts packed using the tape-and-reel method (see Section 5, *Tape-and-Reel Packing*).

2.4 Power Dissipation

When thermal dissipation is crucial, the QFN package has an advantage over standard dual and quad leaded packages. The leadframe die pad is exposed at the bottom of the package and should be soldered to a properly designed thermal pad on the printed circuit board (PCB). This provides a more direct heat-sink path from the die to the board, and the addition of thermal vias from the thermal pad to an internal ground plane will dramatically increase power dissipation. Soldering the exposed pad also significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests.

Unless otherwise stated, the model data shown in Tables 3, 4, and 5 assume that the packages have the exposed pad soldered to the thermal pad on the PCB. The thermal effects of intentionally omitting solder from the exposed pad also is shown later in this section for informational purposes. The standards used for these models are available for downloading at <http://www.jedec.org/download/default.cfm>. [2,3,4] Customers are highly encouraged to familiarize themselves with these standards when comparing the power-dissipation performance of similar or alternative packaging, to ensure that the comparison is made on equivalent terms.

It is important to understand that the modeled data is intended for comparison of the QFN package to alternative packages under similar conditions (the standards mentioned previously). System-level performance is heavily dependent upon board thickness, metal layers, component spacing (thermal coupling), airflow, and board orientation in the system. The model data provided also can be used to construct system-level thermal models to predict performance in any particular system, but does not reflect the package's performance in any system as listed, except in accordance with the standards under which it was modeled.

For data in Tables 3, 4, and 5, values are given for each standard. All standards use the same land pad and thermal pad design; however, they differ in internal board construction. Test cards that comply with JESD 51-3 do not have internal metal layers and are, naturally, the worst case in performance. The shorthand reference for this board design is 1S0P, meaning one signal, zero planes. JESD 51-5 has two internal metal layers and thermal vias connecting the upper layer to the thermal pad. These vias are 0.30-mm diameter and are spaced 1.2 mm, center to center. The vias are allowed to populate only the region defined by the perimeter of the thermal pad and cannot extend beyond the perimeter. This is referred to as 1S2P direct-attached method. JESD 51-7 test cards have the same two metal layers as the JESD 51-5 test card, but no vias are allowed. This is referred to as 1S2P. The standards also allow for a second signal trace on the backside (2S2P or 2S0P), but the backside signal traces make little difference (<2%) in most cases. These three standards give a wide range of conditions under which alternative packages can be compared.

Table 3. Modeled 20-Pin QFN Thermal-Impedance Values

20-Pin QFN Per JESD 51-5 (1S2P Direct-Attach Method)				
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JP} (°C/W)	θ_{JB} (°C/W)
0	29.9	15.2	0.52	5.2
150	23.1			
250	21.2			
500	19.5			

20-Pin QFN Per JESD 51-7 (1S2P)			
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W)
0	46.8	15.2	8.7
150	40.5		
250	38.2		
500	36		

20-Pin QFN Per JESD 51-3 (1S0P)		
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)
0	77.5	15.2

NOTES: A. θ_{JB} is neither applicable nor defined for JESD 51-3 test cards.

B. θ_{JP} is junction-to-pad thermal impedance.

Table 4. Modeled 16-Pin QFN Thermal-Impedance Values

16-Pin QFN Per JESD 51-5 (1S2P Direct-Attach Method)				
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JP} (°C/W)	θ_{JB} (°C/W)
0	31.2	16.23	0.6	4.3
150	24.4			
250	22.5			
500	20.7			

16-Pin QFN Per JESD 51-7 (1S2P)				
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JP} (°C/W)	θ_{JB} (°C/W)
0	49.6	16.23	5.33	10.0
150	42.4			
250	40.1			
500	37.8			

16-Pin QFN Per JESD 51-3 (1S0P)		
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)
0	79.9	16.23

NOTES: A. θ_{JB} is neither applicable nor defined for JESD 51-3 test cards.

B. θ_{JP} is junction-to-pad thermal impedance.

Table 5. Modeled 14-Pin QFN Thermal-Impedance Values

14-Pin QFN Per JESD 51-5 (1S2P Direct-Attach Method)				
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JP} (°C/W)	θ_{JB} (°C/W)
0	31.6	17.37	0.75	4.9
150	25.1			
250	23.1			
500	21.4			

14-Pin QFN Per JESD 51-7 (1S2P)			
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)	θ_{JB} (°C/W)
0	52.5	17.37	10.3
150	46		
250	42.9		
500	40.5		

14-Pin QFN Per JESD 51-3 (1S0P)		
Airflow, LFM	θ_{JA} (°C/W)	θ_{JC} (°C/W)
0	81.9	17.37

NOTES: A. θ_{JB} is neither applicable nor defined for JESD 51-3 test cards.

B. θ_{JP} is junction-to-pad thermal impedance.

Figures 10 through 12 show power dissipation of QFN packages on the JEDEC standard test cards.[2, 3, 4] All power-dissipation values assume a junction temperature of 150°C and are modeled.

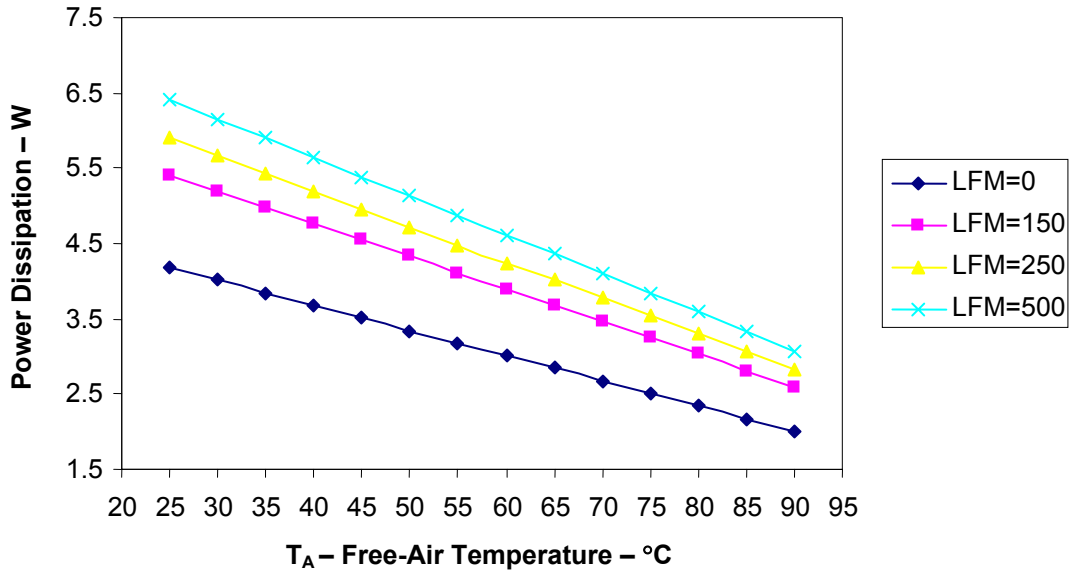


Figure 10. 20-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card

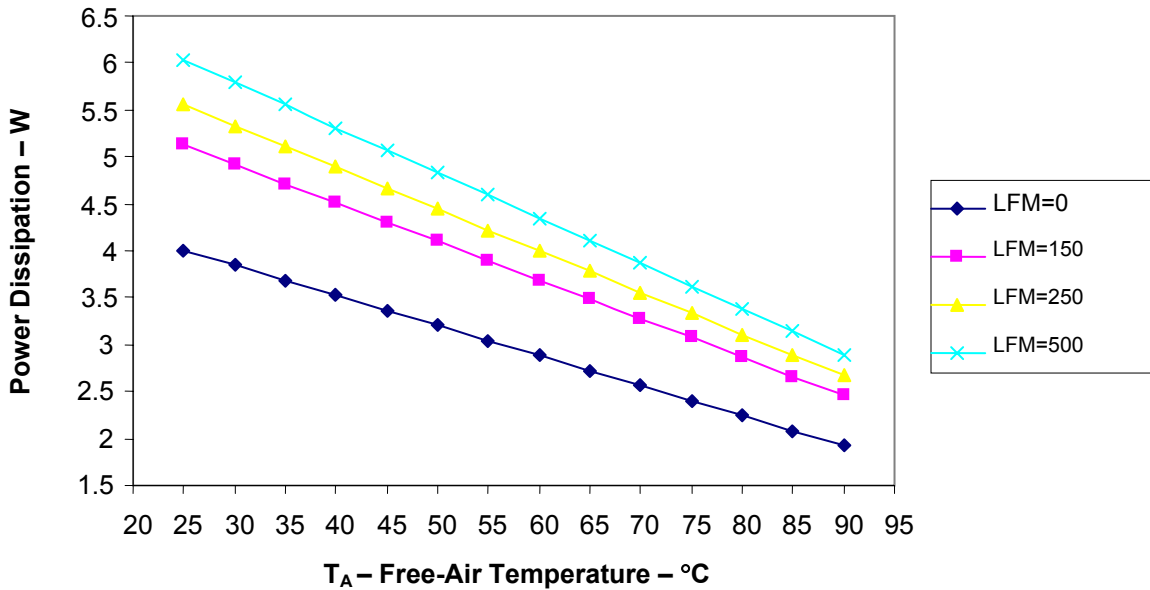


Figure 11. 16-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card

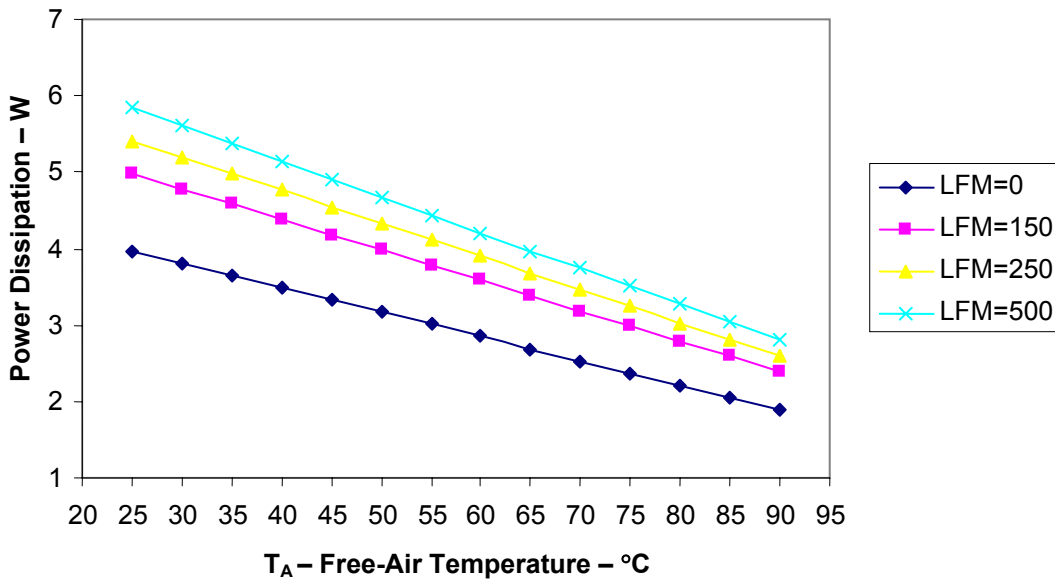


Figure 12. 14-Pin QFN Power Dissipation on JESD 51-5 (1S2P Direct Attach) Test Card

The largest single factor affecting power dissipation is board construction. For the JEDEC test cards that were used to obtain the results in Figures 10 through 12, the JESD 51-5 direct-attach standard offers the best performance. Figures 13 through 16 show the effect of board construction on power dissipation and thermal impedance for the QFN packages.

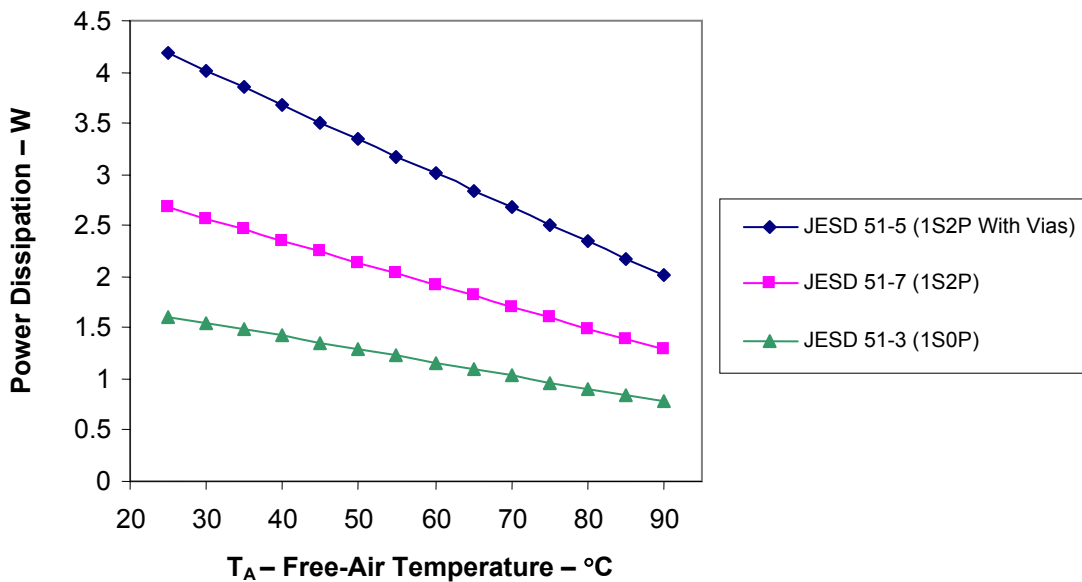


Figure 13. The Effect of Board Layers and Vias on 20-Pin QFN Power Dissipation (JEDEC Test Cards and Zero Airflow)

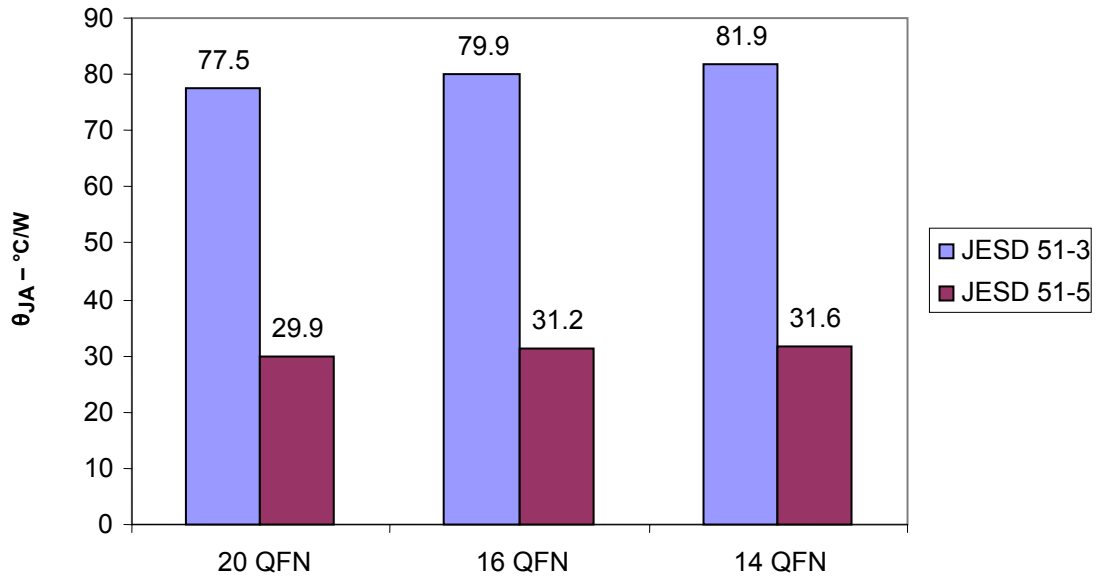


Figure 14. Effect of Board Layers and Vias on θ_{JA} (JESD 51-3 vs JESD 51-5)

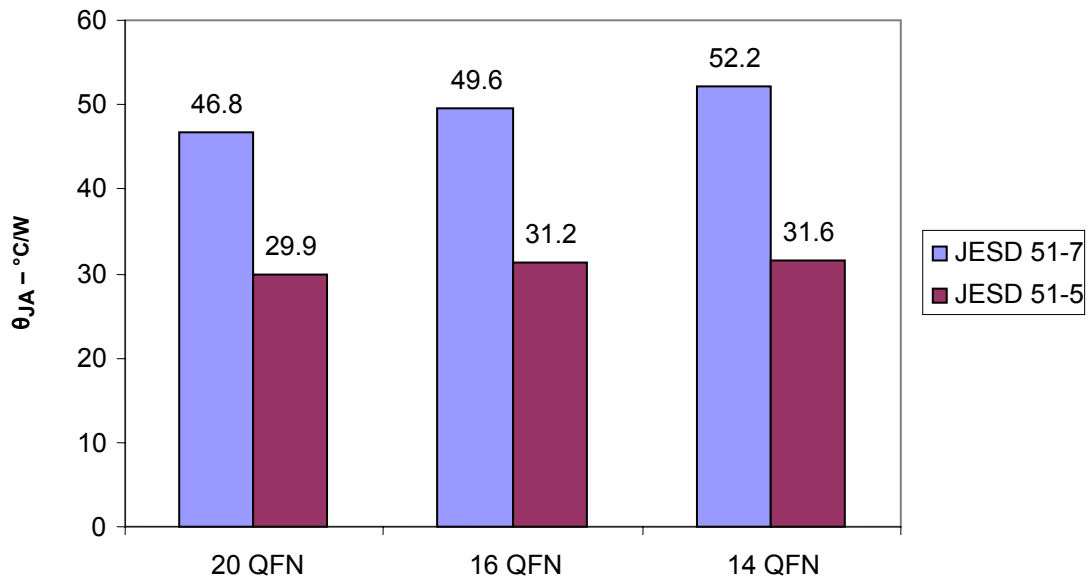


Figure 15. Effect of Board Layers and Vias on θ_{JA} (JESD 51-7 vs JESD 51-5)

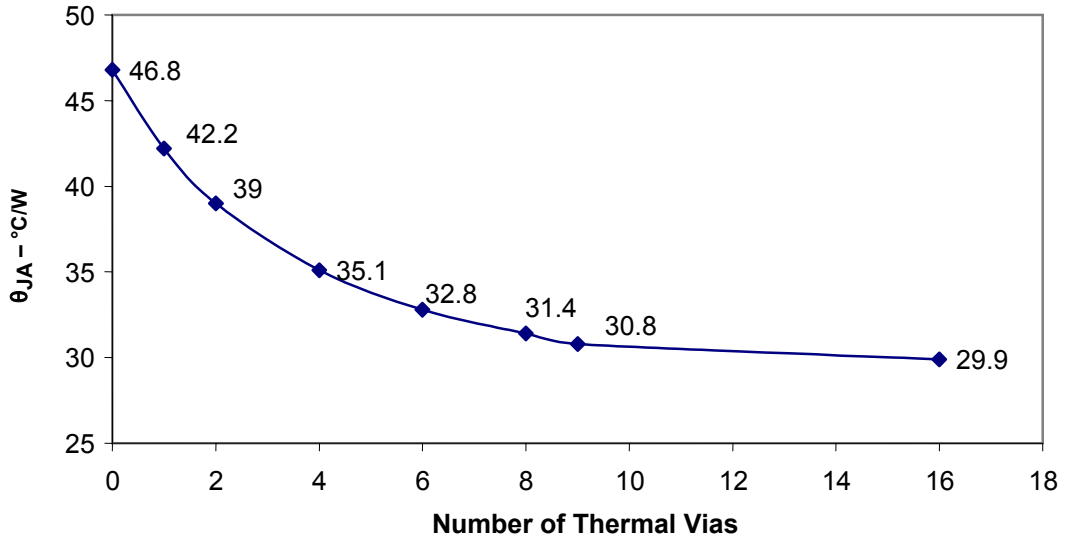


Figure 16. Modeled θ_{JA} vs Number of Thermal Vias on JESD 51-5 Test Card (20-Pin QFN)

Figures 17 through 19 compare the junction-to-ambient thermal impedance of the QFN packages to popular packaging alternatives. These modeled values are on the applicable high-thermal-conductivity boards, as specified by JESD 51-5 and JESD 51-7.

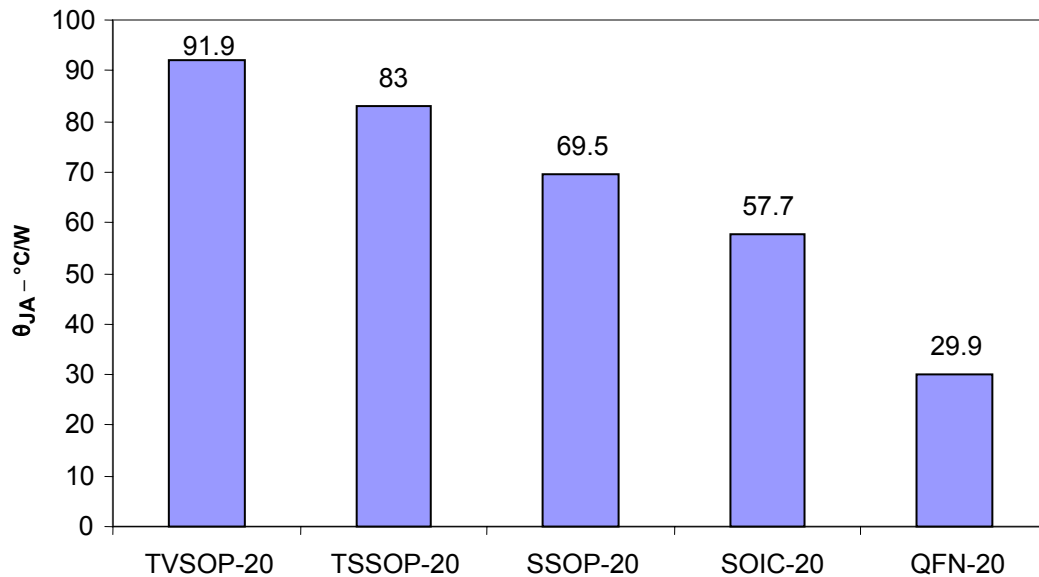


Figure 17. Modeled Thermal Impedance of 20-Pin QFN vs Alternative Packaging

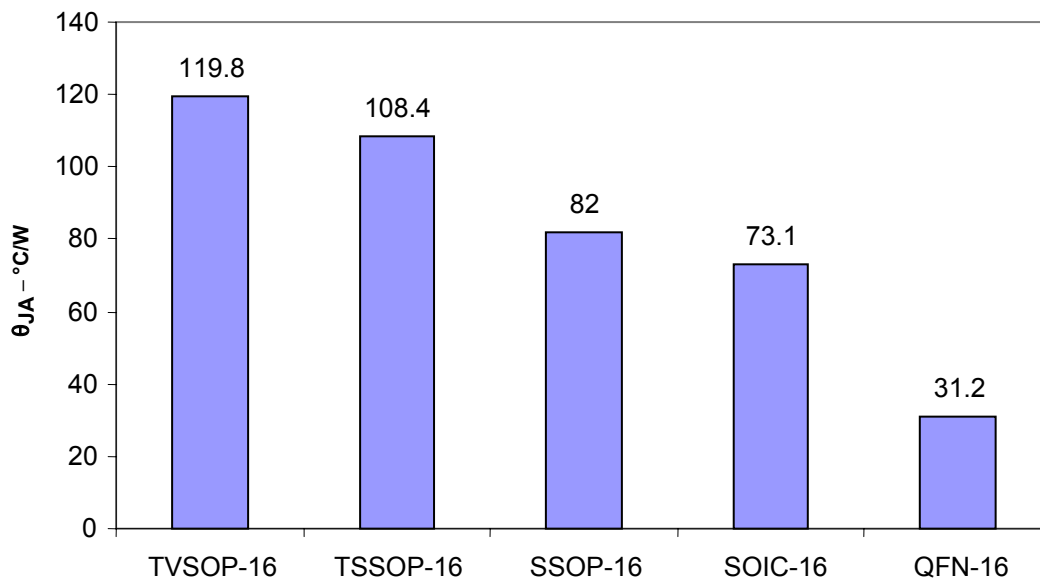


Figure 18. Modeled Thermal Impedance of 16-Pin QFN vs Alternative Packaging

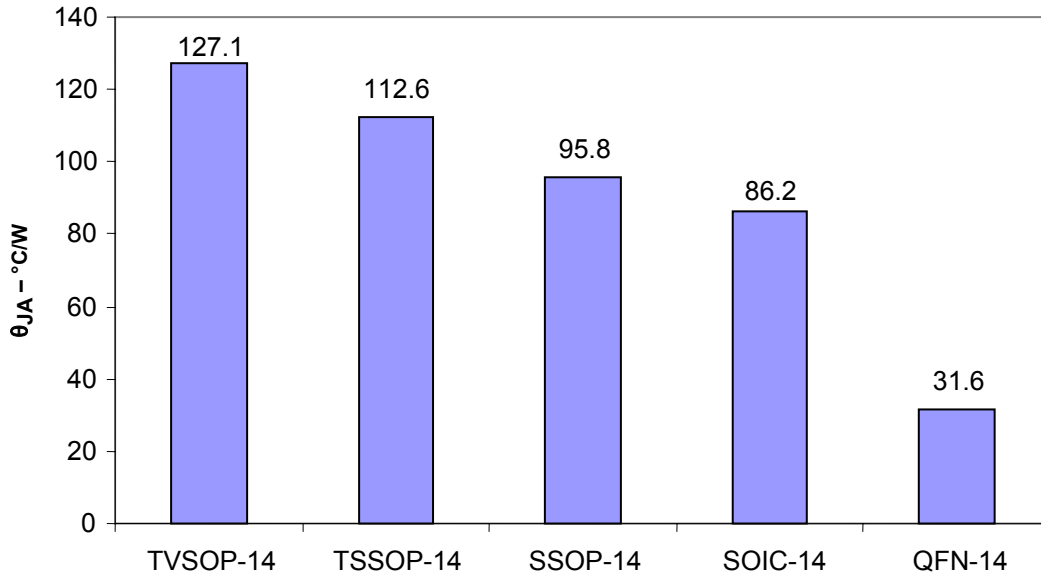


Figure 19. Modeled Thermal Impedance of 14-Pin QFN vs Alternative Packaging

2.5 Electrical

Inductance is related directly to the length of a wire and its proximity to the ground plane. Any wire naturally creates an inductor. The longer the wire, the greater its inductance. Inductance occurs when current is induced into a wire, creating an electromagnetic field. The closer this induced electromagnetic field is to ground, the less effective it becomes. As the wire gets shorter and/or closer to the ground plane, its inductance decreases.

Capacitance is created when two plates (wires, lines, or layers) overlap and are separated by a given distance. This distance can be insulated by air, plastic, glass, or other materials. Capacitance can be calculated by:

$$C = (0.225\epsilon_r A) / d \quad (1)$$

Where:

C = capacitance

ϵ_r = dielectric value of insulator

A = area that plates overlap

d = distance between plates

Area changes the most from package to package. The distances lead to lead and die pad to ground plane vary somewhat, while the dielectric value of the insulators (ϵ_r) remains relatively constant.

The unique construction of QFN packages reduces inductance. The exposed die pad of the QFN package is at board level, following assembly, which minimizes inductance. Tables 6 through 8 and Figures 20 through 22 compare modeled package parasitics of the QFN packages with other packaging options using the same die.

Table 6. Modeled 20-Pin QFN Package-Parasitics Comparison

	SOIC-20 (DW)	SSOP-20 (DB)	TSSOP-20 (PW)	TVSOP-20 (DGV)	QFN-20 (RGY)
Average R, Ω	0.038	0.040	0.050	0.044	0.050
Average L, nH	5.012	3.495	2.802	2.561	1.119
Average C, pF	0.717	0.420	0.317	0.342	0.352

Table 7. Modeled 16-Pin QFN Package-Parasitics Comparison

	SOIC-16 (D)	SSOP-16 (DB)	TSSOP-16 (PW)	TVSOP-16 (DGV)	QFN-16 (RGY)
Average R, Ω	0.039	0.048	0.045	0.039	0.039
Average L, nH	3.453	3.536	2.593	2.543	0.886
Average C, pF	0.521	0.376	0.281	0.386	0.327

Table 8. Modeled 14-Pin QFN Package-Parasitics Comparison

	SOIC-14 (D)	SSOP-14 (DB)	TSSOP-14 (PW)	TVSOP-14 (DGV)	QFN-14 (RGY)
Average R, Ω	0.031	0.044	0.032	0.035	0.033
Average L, nH	3.109	3.551	2.378	2.499	0.738
Average C, pF	0.473	0.402	0.314	0.361	0.316

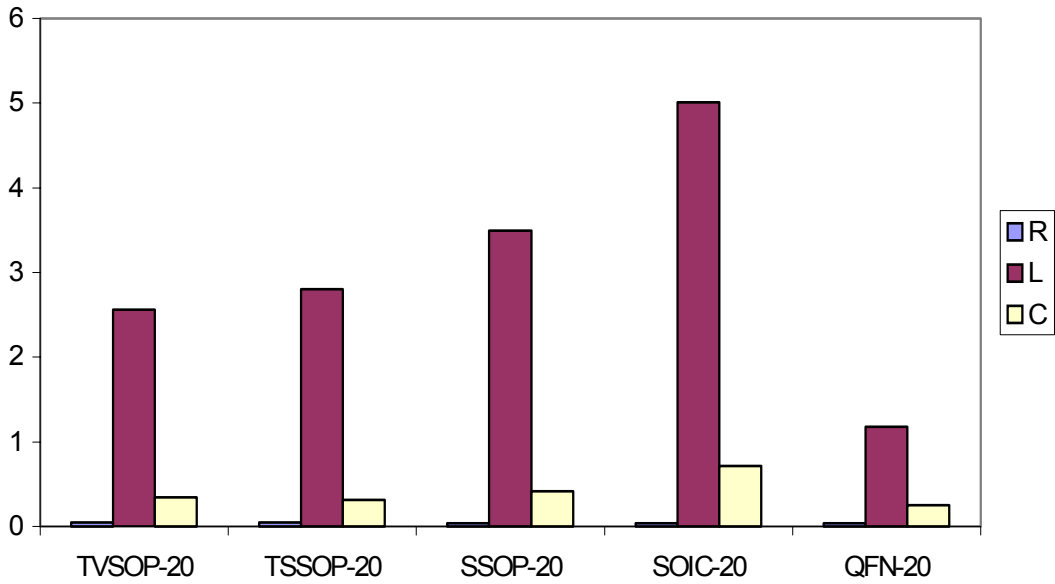


Figure 20. Modeled 20-Pin Package-Parasitics Comparison

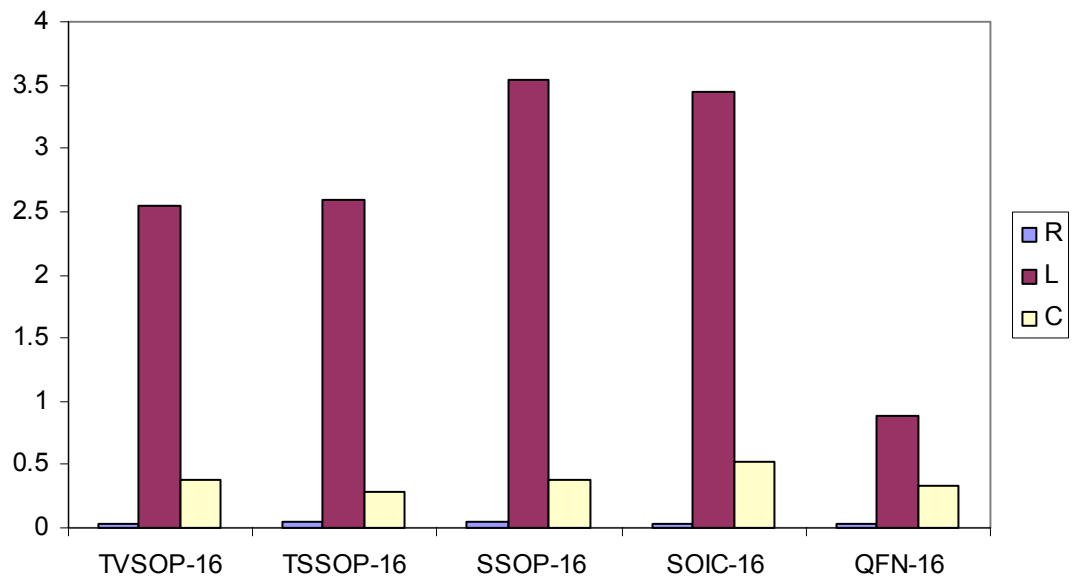


Figure 21. Modeled 16-Pin Package-Parasitics Comparison

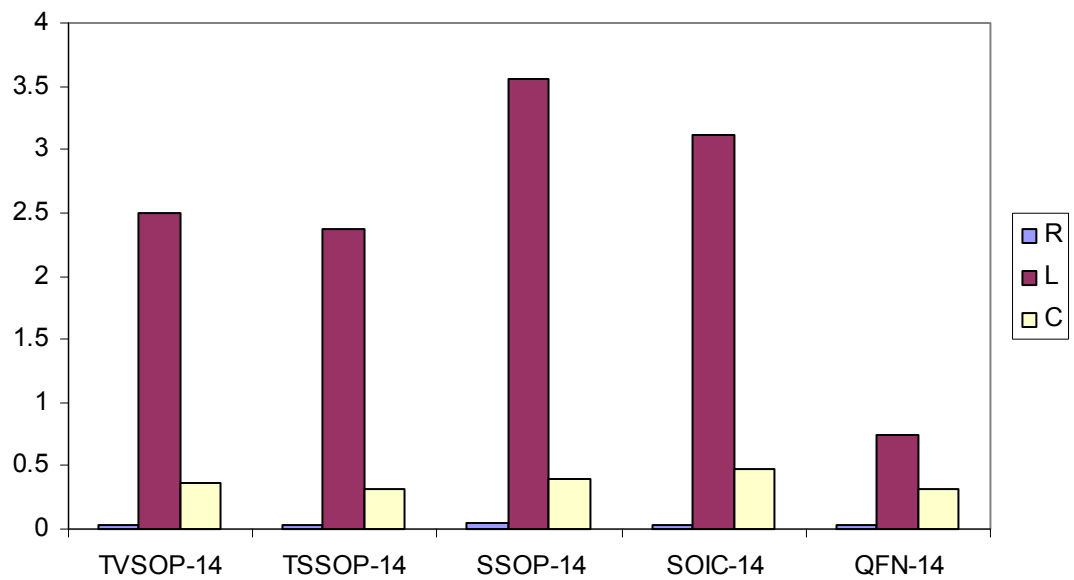


Figure 22. Modeled 14-Pin Package-Parasitics Comparison

2.6 Board-Level Reliability

When soldered, the QFN exposed-pad design acts as a package anchor, significantly increasing the board-level reliability over that of an LCC or other leadless packages. The exposed pad must be soldered to provide the structural integrity expected by industry, as well as optimal thermal performance.

The 14- and 20-pin QFN packages have passed 1000 thermal cycles from -40°C to 125°C , 2 cycles per hour, on a 1.5-mm-thick FR-4 PWB. Pad finishes were NiAu for the SnPb paste and pure Sn for the Pb-free paste. The pastes used were SnPb (63/37) and the Senju Pb-free 96.5Sn/3.0Ag/0.5Cu. The temperature cycling tests continue and will end when data collection is complete.

Board-level package shear also was measured for both packages and pastes. Table 9 summarizes the results.

Table 9. Board-Level Package Shear Values for QFN Packages (n = 19)

	20-Pin RGY		14-Pin RGY	
	Pb Free	SnPb	Pb Free	SnPb
Average, kg	29.378	31.360	24.580	25.405
Maximum, kg	31.392	34.775	30.34	28.845
Minimum, kg	27.314	27.285	21.131	20.217
Standard Deviation	1.087	2.073	2.167	2.614

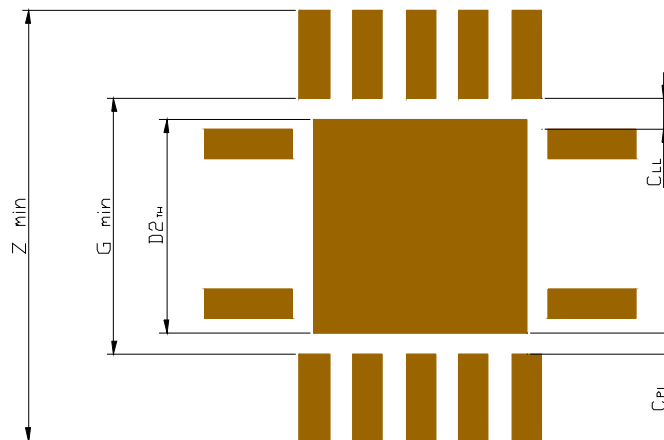
3 Board-Level Assembly

3.1 PCB Design Guidelines

One of the key efforts in implementing the QFN package is the design of the land pattern. The QFN has rectangular metal terminals exposed on the bottom peripheral surface of the package body. Electrical and mechanical connections between the component and the PCB are made by screen-printing solder paste on the PCB and reflowing the paste after placement. To ensure reliable solder joints, properly designing the land pattern to the QFN terminal pattern is essential. IPC-SM-782 is used as the standard for the PCB land-pad designs.

There are two basic designs for PCB land pads for the QFN package: non-solder-mask-defined (NSMD) and the solder-mask-defined (SMD) styles. The industry has debated the merits of both styles of land pads and, although we recommend the NSMD pad, both styles are acceptable for use with the QFN package. NSMD pads are recommended over SMD pads because of the tighter tolerance on copper etching than on solder masking. NSDM, by definition, also provides a larger copper-pad area and allows the solder to anchor to the edges of the copper pads, thus providing improved solder-joint reliability.

Figure 23 illustrates the critical dimensions of a generic QFN land pattern.



Symbol	Description
Z_{min}	Terminal land pad – outside dimension
G_{min}	Terminal land pad – inside dimension
X	Terminal land width
Y	Terminal land length
$C_{LL}†$	Minimum distance between two perpendicular lands in any corner
$C_{PL}†$	Minimum distance between die paddle and inside edge of terminal pad

† C_{LL} and C_{PL} are clearance dimensions defined to prevent solder bridging.

Figure 23. Critical Dimensions of 14-Pin QFN Package Land Pad

3.2 PCB Land-Pattern Design

As a general rule, for good solder filleting, the PWB terminal pads should be 0.2 mm to 0.5 mm longer (away from package center) than the package terminal length and also should be extended 0.05 mm toward the centerline of the package (see Figure 24). To minimize solder bridging, the pad width should be the maximum width of the component terminal for lead pitches below 0.65 mm. These pad designs are wide enough to allow for via-in-pad routing techniques to be employed on an economical basis. Single-layer routing or standard vias outside the package outline also is feasible because of flow-through design.

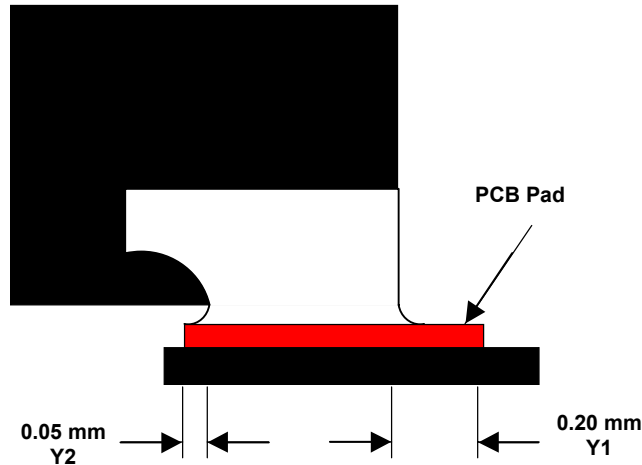


Figure 24. Cross Section of QFN Terminal-Land-Pad Geometry

Z_{min} should accommodate the maximum package length or width (D or E), the profile tolerances of the package body ($aaa = 0.15$ mm for these packages), plus the recommended extensions ($Y1$) for fillets on both ends of the package (0.2 mm \times 2). In other words:

$$Z_{min} = D_{bsc} + aaa + 2(Y1) = D + 0.15 \text{ mm} + 0.4 \text{ mm} \quad (2)$$

$$Z_{min} = E_{bsc} + aaa + 2(Y1) = E + 0.15 \text{ mm} + 0.4 \text{ mm} \quad (3)$$

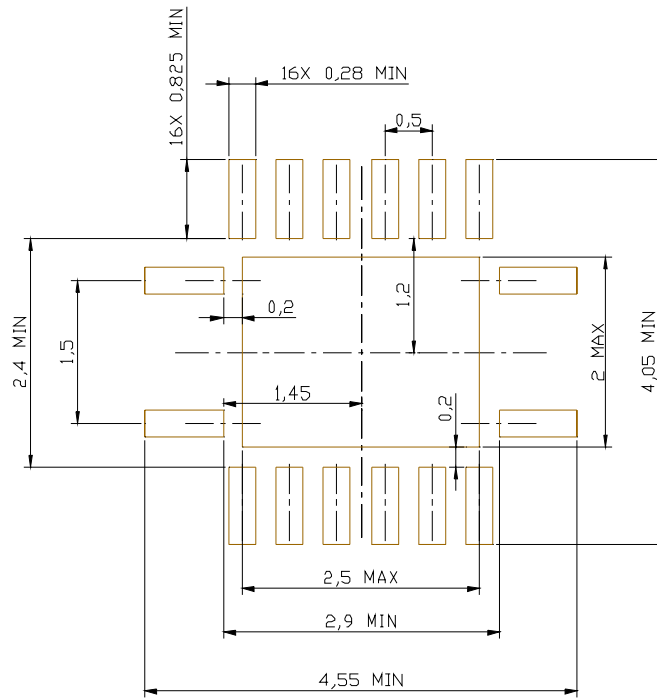
G_{min} should be designed so that the worst case of maximum terminal length is accommodated. In this case, G_{min} is calculated as follows:

$$G_{min} = D_{bsc} - 2(L_{max}) - 2(Y2) = D - 2(0.50) - 2(0.05) \quad (4)$$

$$G_{min} = E_{bsc} - 2(L_{max}) - 2(Y2) = E - 2(0.50) - 2(0.05) \quad (5)$$

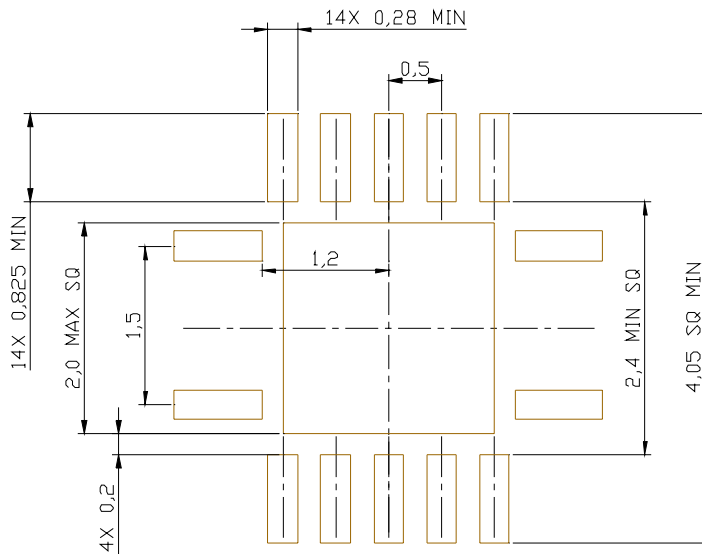
The construction of the exposed-pad QFN package provides enhanced thermal and board-level reliability characteristics. To take full advantage of this feature, the pad must be physically connected to the PCB substrate with solder.

The thermal pad (see $D2_{th}$ in Figure 23) should be greater than $D2$ (exposed pad width) of the package whenever possible. However, adequate clearance ($C_{PL} > 0.15$ mm) must be met to prevent solder bridging.



NOTE A. All dimensions are in mm.

Figure 26. Recommended PCB Land-Pad Design for 16-Pin QFN Package



NOTE A. All dimensions are in mm.

Figure 27. Recommended PCB Land-Pad Design for 14-Pin QFN Package

3.3 Stencil Design

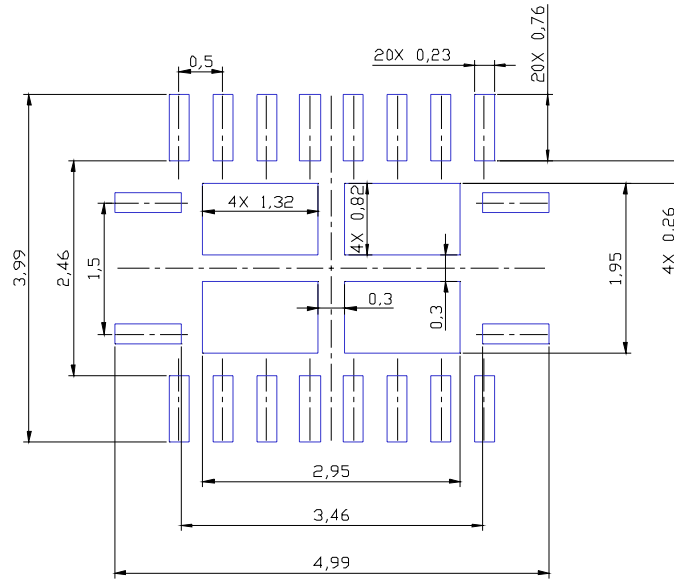
The difference in size between the large exposed pad and small terminal leads of the QFN presents a challenge in producing an even solder-line thickness. Because of this, careful consideration must be given to stencil design. Stencil thickness, as well as the etched-pattern geometry, determines the volume of solder paste deposited on the land pattern. Stencil alignment accuracy and consistent solder-volume transfer is critical for uniform results in the solder-reflow process. Usually, stencils are made of polymer or stainless steel, with stainless steel being more durable and providing less deformation in the squeegee step. Apertures should be trapezoidal in cross section to ensure uniform release of the solder paste and to reduce smearing. The solder-joint thickness for QFN terminal leads should be 50 μm to 75 μm . Stencil thickness usually is in the 100- μm to 150- μm (0.004 in. to 0.006 in.) range, assuming proper area ratio requirements are satisfied (see IPC-7525).[9] If a step-down stencil design is not used, the SMT device(s) that are the limiting factor on the PCB determine the actual thickness of the stencil.

A squeegee with a durometer measurement of 95, or harder, should be used. The blade angle and speed must be optimized to ensure even paste transfer. Characterization of the stencil output is recommended before placing parts.

As a guide, a stencil thickness of 0.1016 mm to 0.125 mm (4 mils to 5 mils) for these QFN packages is recommended. Figures 28 through 30 detail the stencil recommendations for the 14-, 16-, and 20-pin QFN packages. All designs below have area ratios >0.66 and paste-transfer efficiencies of 73% for terminal pads and 100% for thermal pads at a stencil thickness of 0.127 mm (5 mils). At a stencil thickness of 0.1016 mm (4 mils), the area ratio is 0.86, terminal-pad paste-transfer efficiency is 89% and 100% for the thermal pad. The slotted-thermal-pad stencil design is recommended to prevent the QFN package from floating during reflow and causing opens between the terminal leads and pads. This feature also allows adequate room for outgassing of paste during the reflow operation, thus minimizing voids.

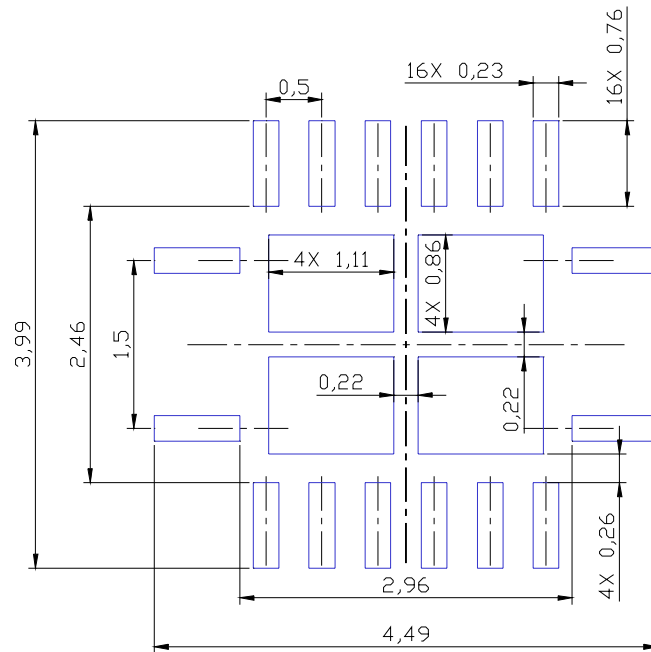
A low-residue, no-clean Type 3 or Type 4 solder paste is recommended.

Stencil design advice and parameters are provided courtesy of Cookson Electronics, Assembly Materials Group, at <http://www.cooksongroup.co.uk/>



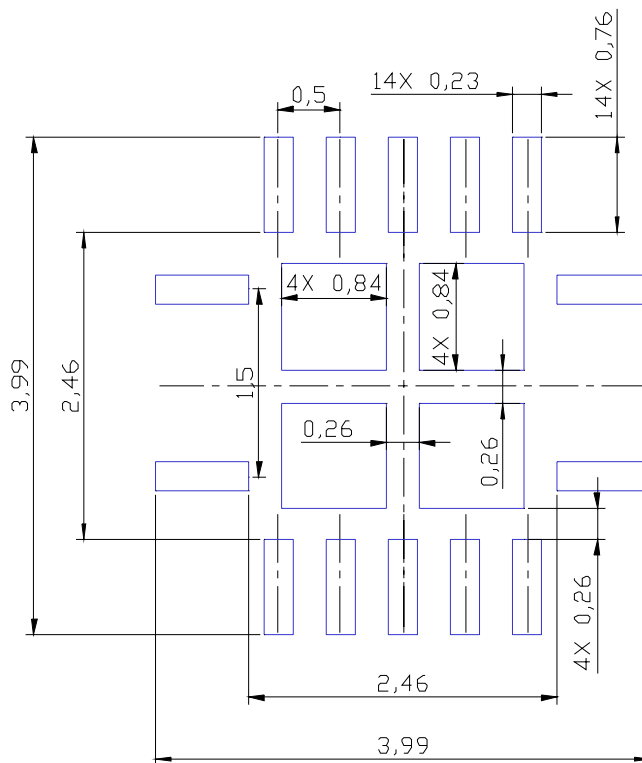
NOTE A. All dimensions are in mm.

Figure 28. Stencil-Design Recommendation for 20-Pin QFN Package



NOTE A. All dimensions are in mm.

Figure 29. Stencil-Design Recommendation for 16-Pin QFN Package



NOTE A. All dimensions are in mm.

Figure 30. Stencil-Design Recommendation for 14-Pin QFN Package

3.4 Component Placement and Reflow

The accuracy of the pick-and-place equipment governs the package placement and rotational (theta) alignment. Slightly misaligned parts (less than 50% off the terminal-pad center) automatically self-align during reflow. Grossly misaligned packages (greater than 50% off terminal-pad center) should be removed prior to reflow because they may develop electrical shorts from solder bridges.

There are two popular methods for package alignment using machine vision:

- Package silhouette—The vision system locates the package outline.
- Lead-frame recognition—Some vision systems can locate directly on the lead-frame pin-1 ID feature (chamfer on exposed pad).

Both methods are acceptable for QFN package placement, but both have advantages and disadvantages. Pad-recognition alignment tends to be more accurate, but is slower because more complex vision processing is required of the pick-and-place machine. The package silhouette method allows the pick-and-place system to run faster, but generally, is less accurate.

Both methods are acceptable and have been demonstrated successfully by major pick-and-place equipment vendors and contract assembly houses.

There are no special requirements when reflowing QFN packages. As with all components, it is important that reflow profiles be checked on all new board designs at different locations on the board because component temperatures may vary because of surrounding thermal sinks, location of the device on the board, and package densities.

Maximum reflow temperature, soak times, and ramp rates specified for a specific solder paste should not be exceeded. Please consult your paste manufacturer for specifics regarding your particular paste because target temperatures and their associated times can vary widely, depending upon metallurgy and flux composition. In general, SnPb peak temperatures are approximately 235°C and Pb-free paste is 250°C to 260°C. The matte tin finish used for these QFN packages has proven interchangeability with either paste type.

Generic Pb-free-paste and SnPb eutectic reflow profiles with time/temperature targets are shown in Figures 31 and 32. Figure 32 shows a generic SnPb profile.

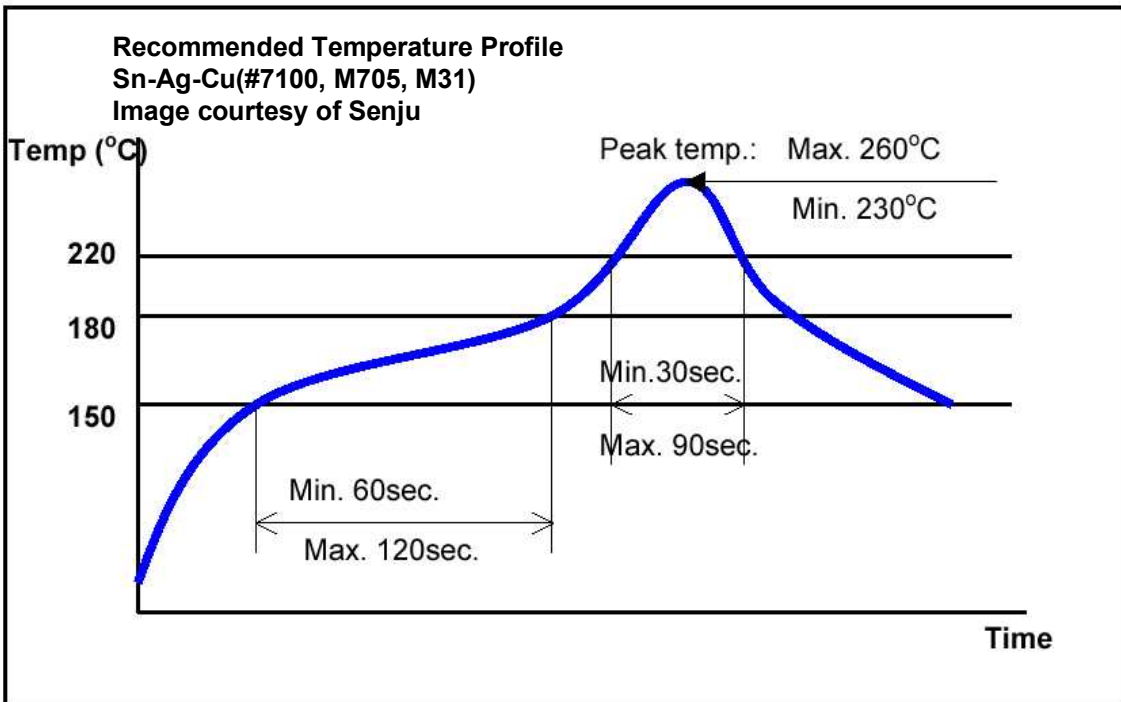


Figure 31. Pb-Free-Paste Reflow Profile

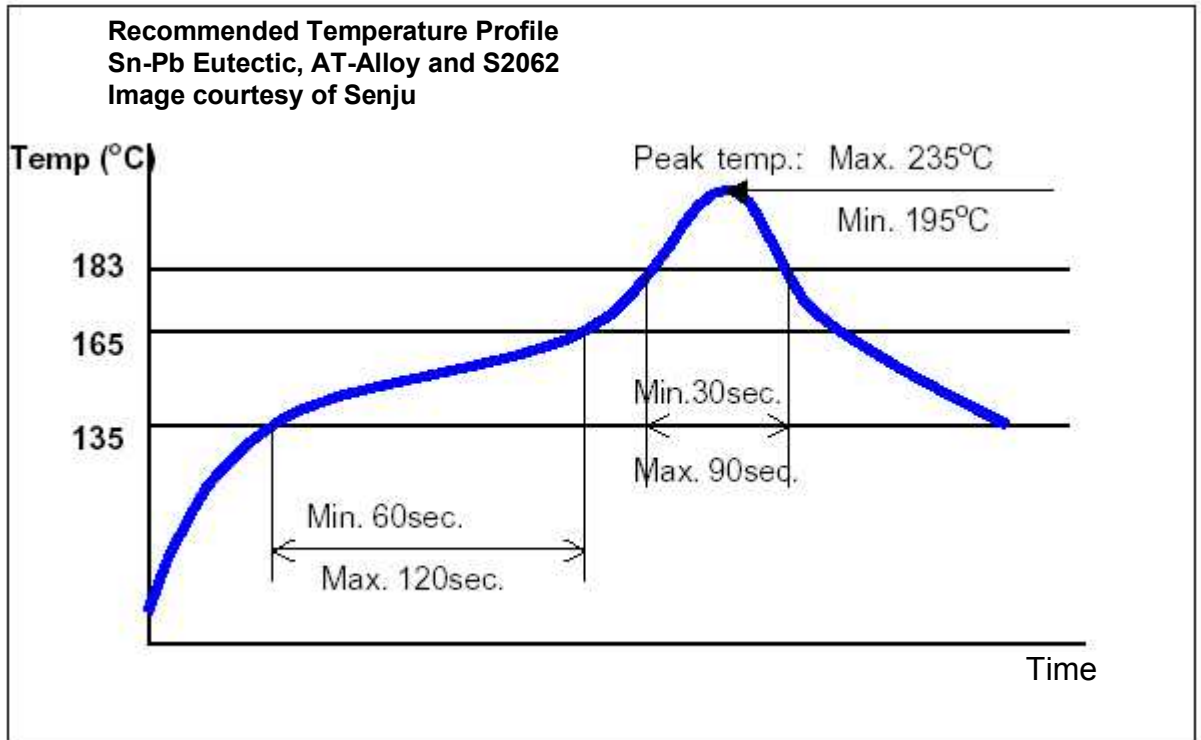


Figure 32. Generic SnPb Reflow Profile

3.5 Rework

QFN-rework processes are an adaptation (and in some cases a simplification) of ball grid array package-rework processes. The basic elements of this process are:

- Board preheat
- Reflow of component solder
- Vacuum removal of component
- Cleaning and preparation of PWB lands
- Screening of solder paste
- Placement and reflow of new component
- Inspection of solder joints

Several automated rework systems exist in the market and address the previous steps in a variety of ways. A system worth noting is by Air-Vac Engineering (<http://www.air-vac-eng.com>). The rework steps above (except inspection) can be accomplished with high precision on a single machine under either computer or manual control.

Another example of a well-established rework system is the Metcal APR-5000. This system contains the essential hardware and automated software features necessary for reworking QFN and other packages. This system takes up less than 6 ft² of manufacturing floor space. Both systems offer closed-loop, computer-controlled time, temperature, and airflow parameters to help ensure process control and repeatability. The system software manages the reflow profile: preheat, soak, ramp, reflow, and cooling. In addition, board temperature can be monitored using integrated thermocouples, and real-time adjustments can be made to all parameters while the profile is running.

A variety of off-the-shelf vacuum collets and solder screens are available from Metcal. Please reference <http://www.metcal.com> for open tools and for custom tooling requirements.

4 Tape-and-Reel Packing

4.1 Material Specifications

TI offers tape-and-reel packing for 14-, 16-, and 20-pin logic QFN packages in standard packing quantities (SPQ) of 1000 units/reel. The units are shipped in embossed carrier tape, sealed with heat-activated or pressure-sensitive cover tape, wound on plastic reels. All of the tape-and-reel materials comply with EIA-481 B, and EIA-541.[5,6] The EIA specifications are shown in Table 10 and Figures 33 through 35. The carrier tape is made of conductive polystyrene and has a surface resistivity that falls within the static-dissipative range (1×10^5 to $1 \times 10^{11} \Omega/\text{square}$). Heat-activated or pressure-sensitive, antistatic, clear polyester film is used for the cover tape. The dimensions of most interest to the end user are tape width (W), cavity pitch (P), and cavity size (A_0 , B_0 , K_0), as shown in Figure 33.

The units are placed in the carrier-tape cavity, with pin 1 located as specified in EIA-481B. The longest axis of the package is perpendicular to the tape sprocket holes, and pin 1 is closest to the round sprocket holes. Thus, for rectangular or square packages, pin 1 is located in quadrant 1 (see Figure 35). The 3.5-mm \times 4.5-mm 20-pin QFN package is shown in Figure 36. All dimensions are in millimeters.

Table 10. Carrier-Tape Dimensions

Package	Carrier-Tape Width (W)	Cavity Pitch (P)	Cavity Width (A ₀)	Cavity Length (B ₀)	Cavity Depth (K ₀)	Device Quantity Per Reel (SPQ)
14-Pin QFN	12.0 ± 0.30	8.0 ± 0.10	3.80 ± 0.10	3.80 ± 0.10	1.20 ± 0.10	1000
16-Pin QFN	12.0 ± 0.30	8.0 ± 0.10	3.80 ± 0.10	4.30 ± 0.10	1.20 ± 0.10	1000
20-Pin QFN	12.0 ± 0.30	8.0 ± 0.10	3.80 ± 0.10	4.80 ± 0.10	1.20 ± 0.10	1000

D ₀	D ₁ Min	E ₁	P ₀	P ₂	R Ref	S ₁ Min	T Max	T ₁ Max
1.5 + 0.1/ - 0.0	1.5	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	30	0.6	0.6	0.1

NOTE A. All dimensions are in mm.

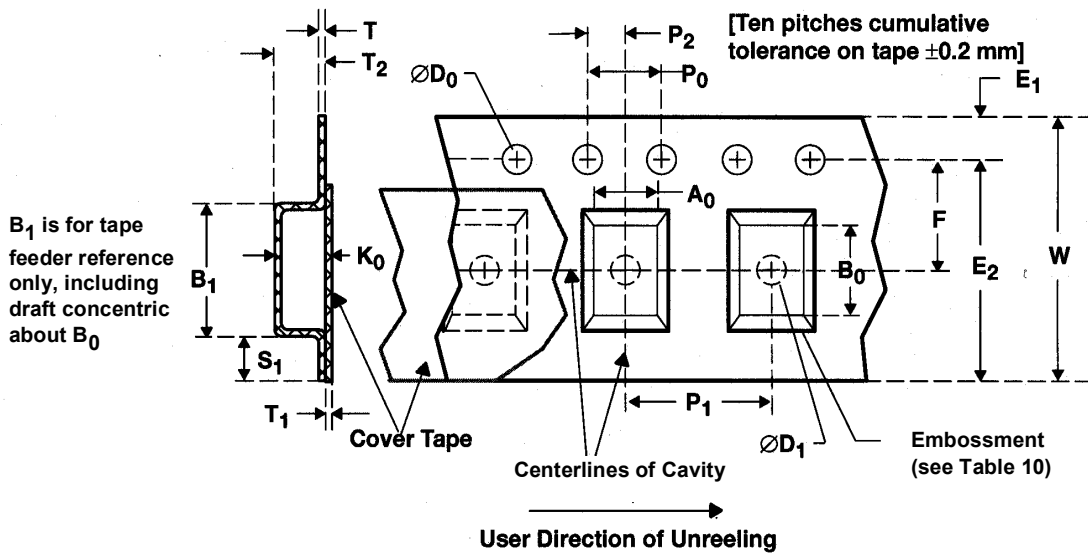
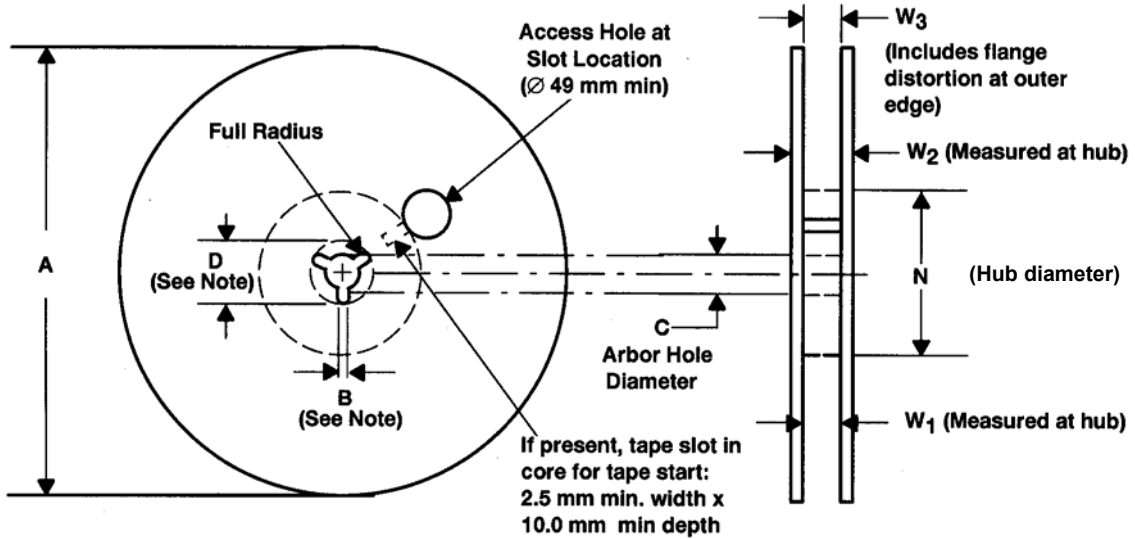


Figure 33. Carrier-Tape Dimensions



NOTE A. Drive spokes optional; if used, dimensions B and D shall apply.

Reel Diameter (A)	Reel Width (W ₁)	Hub Diameter Max (N)	Reel Thickness (W ₂)	Arbor-Hole Diameter (C)	Quantity/Reel
					14/16/20 Pins
180 ± 0.60	12.4 + 2.0/-0.0	60 ± 0.50	13.65 ± 1.95	13.0 + .5/-0.2	1000

NOTE B. All dimensions are in mm.

Figure 34. Reel Specifications

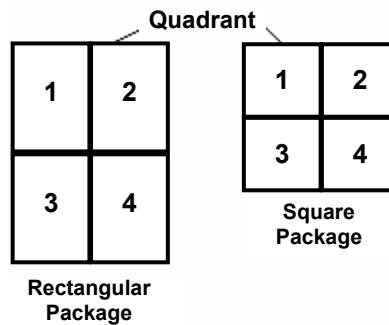


Figure 35. Carrier-Tape Cavity Quadrant Location for Pin 1, Per EIA-481B

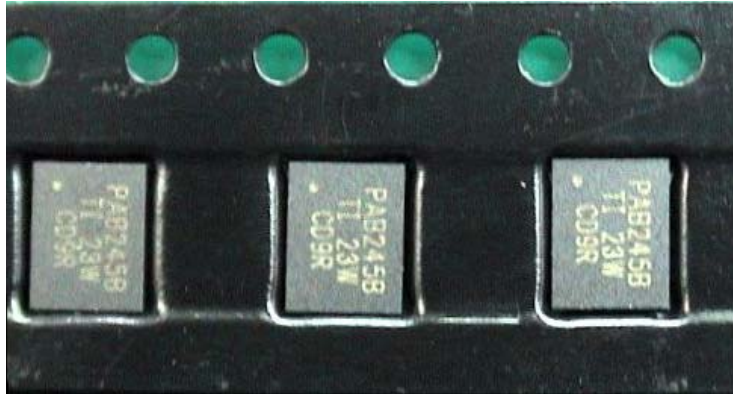


Figure 36. Pin-1 Orientation of QFN Packages in Carrier Tape

4.2 Labels

All reels have an ESD label or symbol on the hub or flange and have a bar-code label on the same side of the reel and on the side opposite the carrier-tape round sprocket holes, as shown in Figure 37.

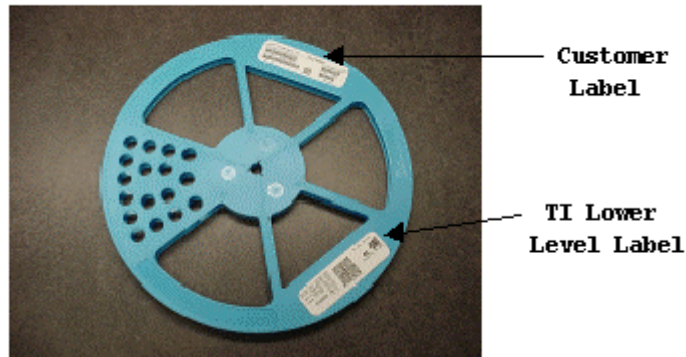


Figure 37. Reel Labeling

Intermediate container orientation and labeling specification for reels is shown in Figures 38, 39, and 40.

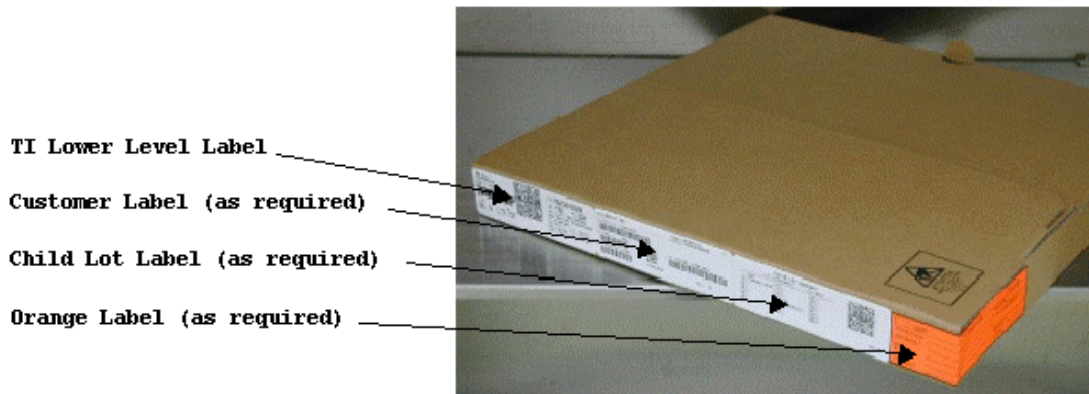


Figure 38. Regular Shipping-Box Label Placement

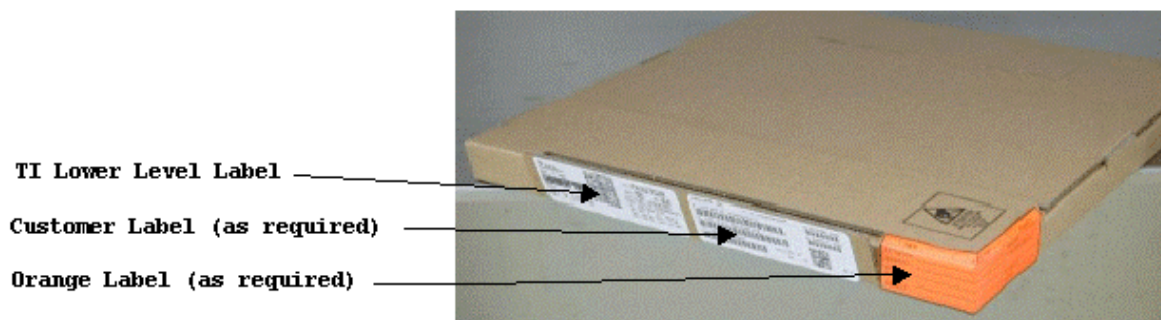


Figure 39. Label Placement On Shipping Box with Flap



Figure 40. Child-Lot Label Placement on Shipping-Box Label Flap

The moisture-sensitivity caution (MSID) label can appear on any surface of the box, except areas that will be occupied by other labels, but not on the bottom of the box.

4.3 Dry-Pack Requirements for Moisture-Sensitive Material

Moisture-sensitive material, as classified by JEDEC standard J-STD-020, must be dry packed (see Table 11).[7] Dry packing limits the exposure of the package to moisture so that it can be reflowed without “popcorning”. Dry packing consists of desiccant material and a humidity-indicator card (HIC) sealed with the populated reel inside a moisture-barrier bag (MBB) (see Figures 40 and 41, respectively).

Table 11. Dry-Pack Requirements for MSL Level 1 and Level 2 Packages

Level	Dry Before Bag	MBB	Desiccant	MSID Label	Moisture-Sensitivity Caution Label
1	Optional	Optional	Optional	Not Required	Not Required
2	Optional	Required	Required	Required	Required

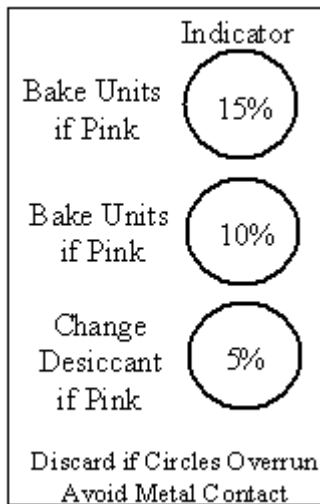


Figure 41. Humidity Indicator Card

Labels will be placed on moisture-barrier bags as shown in Figure 42.

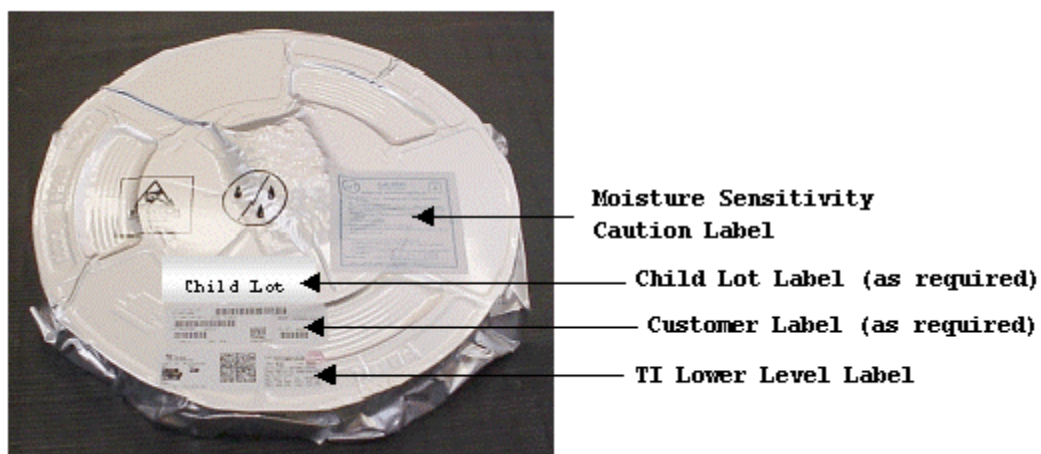


Figure 42. Label Placement on Tape-and-Reel Moisture-Barrier Bag

The required dry-pack labels are the moisture-sensitivity identification (MSID) label and the moisture-sensitivity caution label as specified in J-STD-033.[8] The MSID label is affixed to the lowest-level shipping container that contains the MBB. The caution label is affixed to the outside surface of the MBB.

The calculated shelf life for dry-packed components is a minimum of 12 months from the MBB seal date, when stored in a noncondensing atmospheric environment of <40°C and 90% relative humidity (see Table 12).

Table 12. Floor Life Under Conditions Other Than 30°C and 60% Relative Humidity

Level	Floor Life (out of bag) at Factory Ambient Environment of 30°C and 60% Relative Humidity, or as Stated
1	Unlimited at 30°C and 85% Relative Humidity
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory baking before use After baking, must be reflowed within the time limit specified on the label

4.3.1 Symbols and Labels

The symbol shown in Figure 43 indicates that devices are moisture sensitive at level 2, or lower, and must appear on all moisture-sensitivity caution labels.



Figure 43. Moisture-Sensitivity Symbol

The label shown in Figure 44 is affixed to the lowest-level shipping container to indicate that moisture-sensitive devices are in the container. It is recommended that this label be a minimum of 20 mm in diameter.



Figure 44. MSID Label

The moisture-sensitivity caution label (see Figure 45), is used for levels 2, 2a, 3, 4, 5, and 5a as defined by J-STD-020. This label is required on the MBB and provides the information as shown in Figure 45.


	<p>CAUTION</p> <p>This bag contains</p> <p>MOISTURE-SENSITIVE DEVICES</p>	<p>LEVEL</p> <div style="border: 1px solid black; width: 80px; height: 40px; margin: 0 auto;"></div> <p>If Blank, see adjacent bar code label</p>
<p>1. Calculated shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH)</p> <p>2. Peak package body temperature: _____ °C If Blank, see adjacent bar code label</p> <p>3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must</p> <p style="margin-left: 20px;">a) Mounted within: _____ hrs. of factory conditions If Blank, see adjacent bar code label ≤ 30°C/60% RH, OR</p> <p style="margin-left: 20px;">b) stored at <10% RH</p> <p>4. Devices require bake, before mounting, if:</p> <p style="margin-left: 20px;">a) Humidity Indicator Card is > 10% when read at 23 ± 5 °C</p> <p style="margin-left: 20px;">b) 3a or 3b not met.</p> <p>5. If baking is required, devices may be baked for 48 hrs. at 125 ± 5°C</p> <p style="margin-left: 40px;">Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure</p> <p>Bag Seal Date: _____ If Blank, see adjacent bar code label</p> <p style="margin-left: 20px;">Note: Level and body temperature defined by IPC/JEDEC J-STD-020</p>		

Figure 45. Moisture-Sensitivity Caution Label for Levels 2–5a

5 Symbolization

The top of the package is laser marked with device name, corporate ID, date code, assembly-site code, assembly-lot trace code, and pin-1 location. Table 13 shows the device-marking symbolization guidelines for 14-pin, 16-pin, and 20-pin QFN packages.

Table 13. Device-Marking Guidelines

QFN Symbolization Guidelines					
Pins	Package	Namerule and Format	Maximum Characters per Row	Maximum Rows	Symbol Format
14	QFN	C2	6	3	AB245B TI YMS LLLL O
16	QFN	C2	6	3	
20	QFN	C2	7	3	

The symbol-format column entry in Table 13 has the following meaning:

AB245B = Short name for SN74ABT245BRGYR
 TI = Texas Instruments
 Y = Year
 M = Month
 S = Site code
 LLLL = Lot trace code
 O = Pin-1 quadrant identifier (data sheet specifies exact pin-1 location)

For specific marking on any device, please see the device data sheet at www.ti.com.

6 Test Sockets

Test sockets for the 14-, 16-, and 20-pin QFN devices can be obtained from:

Plastronics
 2601 Texas Drive
 Irving, Texas 75062
 Phone: 972-258-2580
 Fax: 972-258-6771

Socket part numbers:
 20 Pin: 20QN50T14535
 16 Pin: 16QN50T23030
 14 Pin: 14QN50T23535

7 Features and Benefits

In summary, key features and corresponding advantages for logic products in the QFN package are:

- Superior package parasitics, compared to traditional dual in-line package solutions. Inductance ranges from 50% to 79% lower than alternative packages, and capacitance ranges from 12% to 50% over SSOP and SOIC packages.
- Superior thermal performance and board-level reliability, compared to alternative package solutions. QFN junction-to-ambient thermal impedance ranges from 67% to 75% lower than TVSOP, 64% to 73% lower than TSSOP, 57% to 67% less than SSOP, and 48% to 63% lower than SOIC. Mechanical integrity of the mounted package is greatly enhanced by the soldered exposed die pad.
- Conventional one-to-one pinout, resembling dual-in-line packages. Keeps ground, VCC, and signal pin numbers consistent with previous dual-in-line packages.
- Pb-free packages with backward-compatible solderability that can be soldered with either SnPb or Pb-free pastes.
- Significant area savings over traditional dual-in-line packages. QFN packages are 56% to 62% smaller than equivalent-pin TSSOP counterparts.
- Provides flow-through layout like conventional dual-in-line packages.

8 Conclusion

Texas Instruments 14-, 16-, and 20-pin QFN package offerings are leadframe-based leadless packages, with improved thermal performance, electrical performance, and reduced package volume over similar TSSOP, TVSOP, SSOP, and SOIC packages. Additionally, the QFN packages meet the industry's lead-free demands, have reliable solderability using either Pb or Pb-free solder pastes, and can be reworked and manufactured using conventional equipment. The packages allow for product miniaturization and comply with dimensional specifications of JEDEC standard MO-241.

9 Acknowledgments

The authors thank Ray Purdom for helping with package development, Muhammad Khan for providing electrical models, Bernhard Lange for board-assembly analysis, Cookson Electronics for stencil design, Senju Solder for solder information, Ron Eller and Terrill Sallee for QA support, and Dr. Sreenivasan Koduri for his guidance.

10 References

References 1 through 4 are available at:

<http://www.jedec.org/download/default.cfm>

1. JEDEC Standard MO-241, *Dual In-line Compatible, Thermally Enhanced, Plastic Very Thin Fine Pitch, QFN Packages.*
2. JESD 51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms.*
3. JESD 51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*
4. JESD 51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*
5. EIA-481 B, *Taping of Surface Mount Components for Automatic Placement.*
6. EIA-541, *Packing Material Standards for ESD Sensitive Items.*
7. J-STD-202, *Moisture/Reflow Classification for Non-Hermetic Solid State Surface Mount Devices.*
8. J-STD-033, *Standard for Handling and Shipping of Moisture/Reflow Sensitive Surface Mount Devices.*
9. IPC-7525, *Stencil Design Guidelines*, May 2000.

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