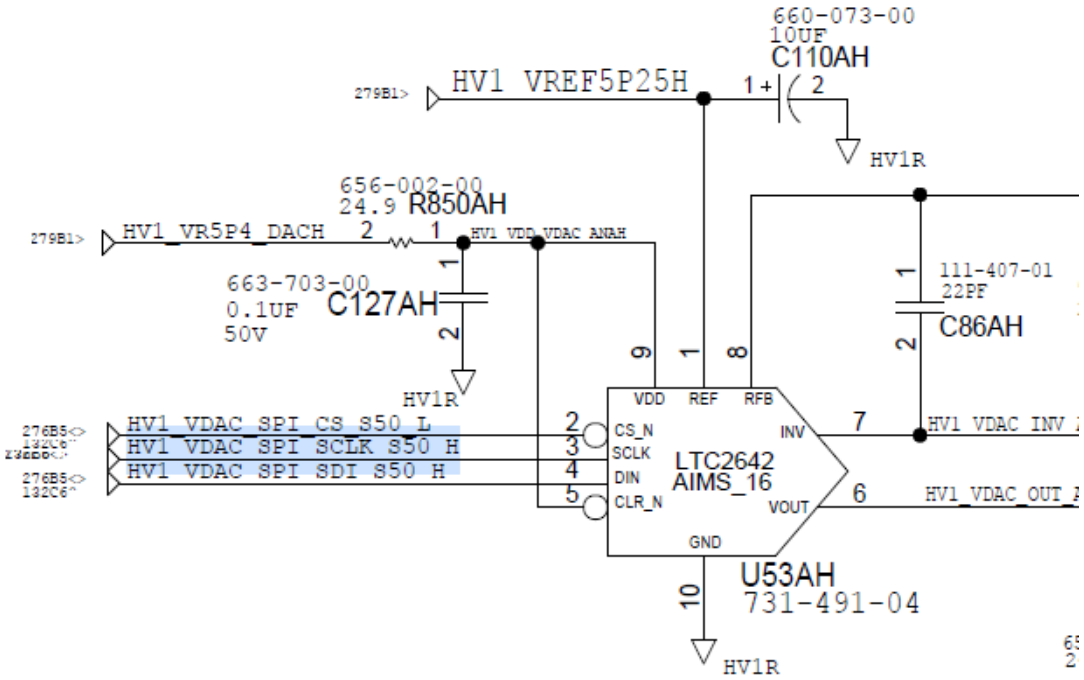
HV1_VDAC_SPI_SCLK_S50_H
3.3V driver and 5V receiver

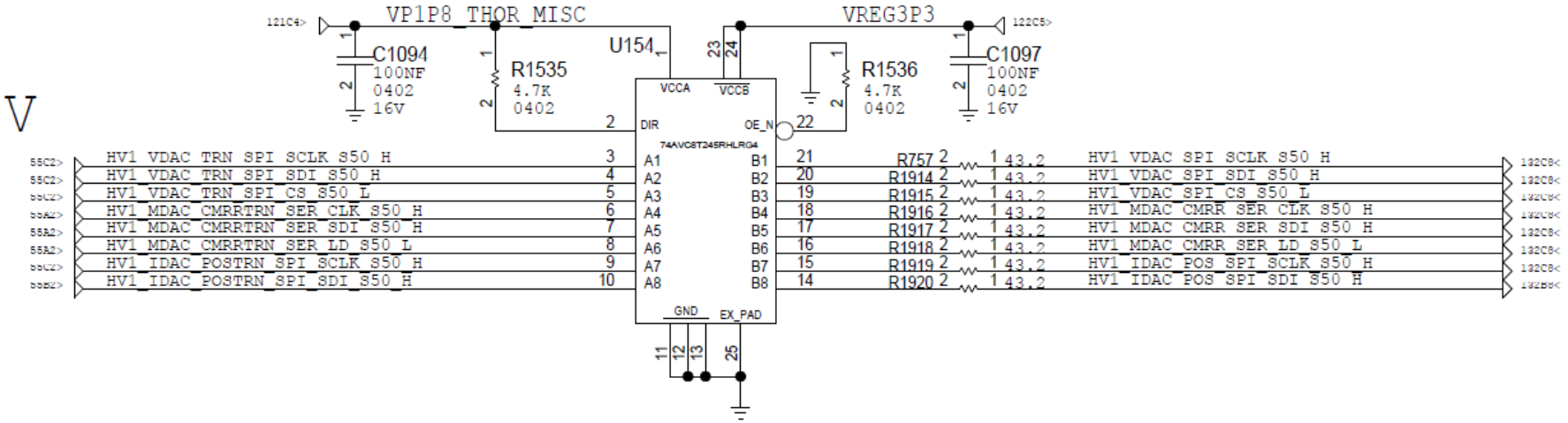
⊞ IL_18		1
⊟ U53AH		1
bufferModel	LTC2642_inpin_5v	1
mappingTag		1
⊟ U154		1
bufferModel	SN74AVC8T245_AVC8T245_IO_33	1
mappingTag		1
⊞ VIA10		1
⊞ VIA11		1



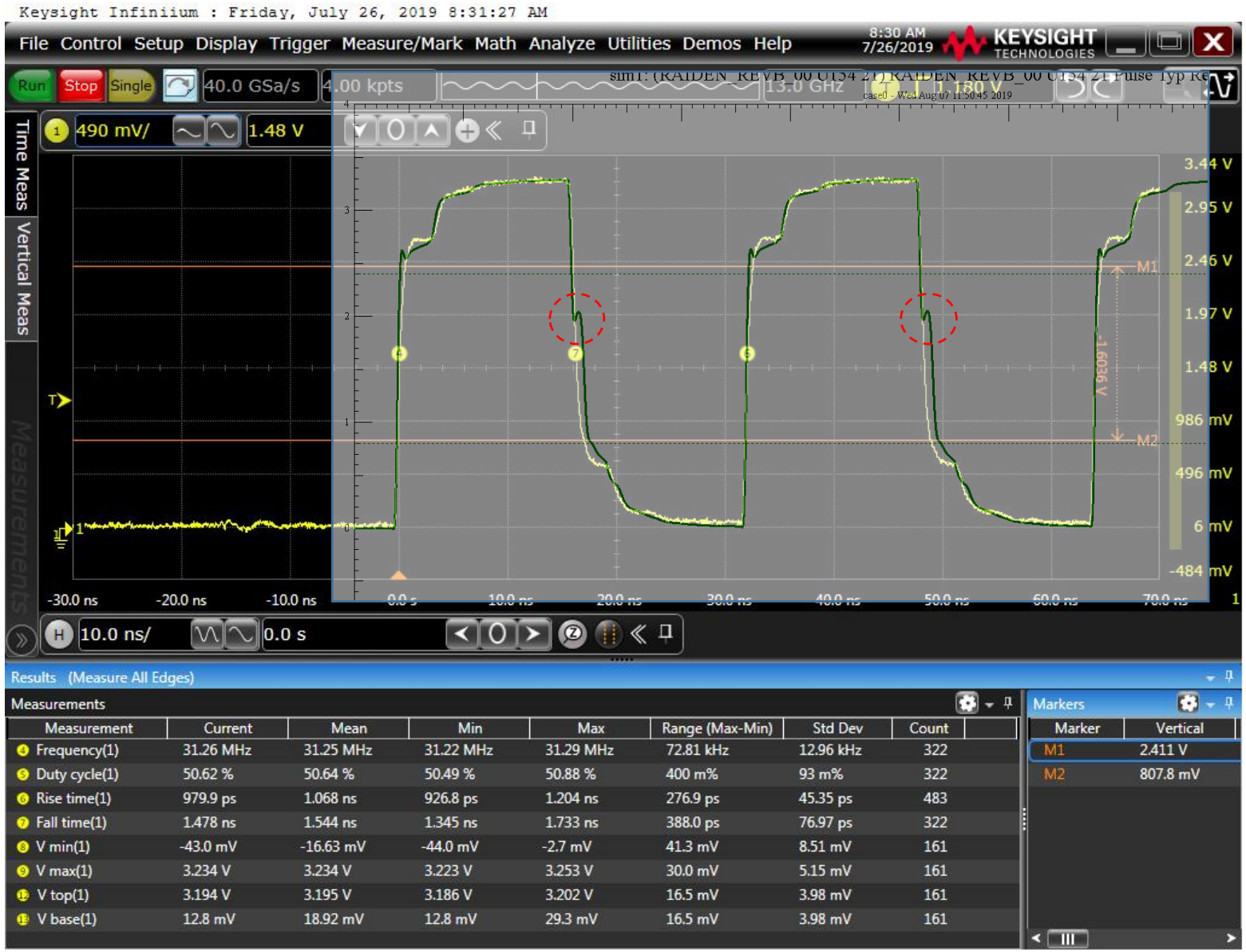
SEE

ZEUS 1.8V

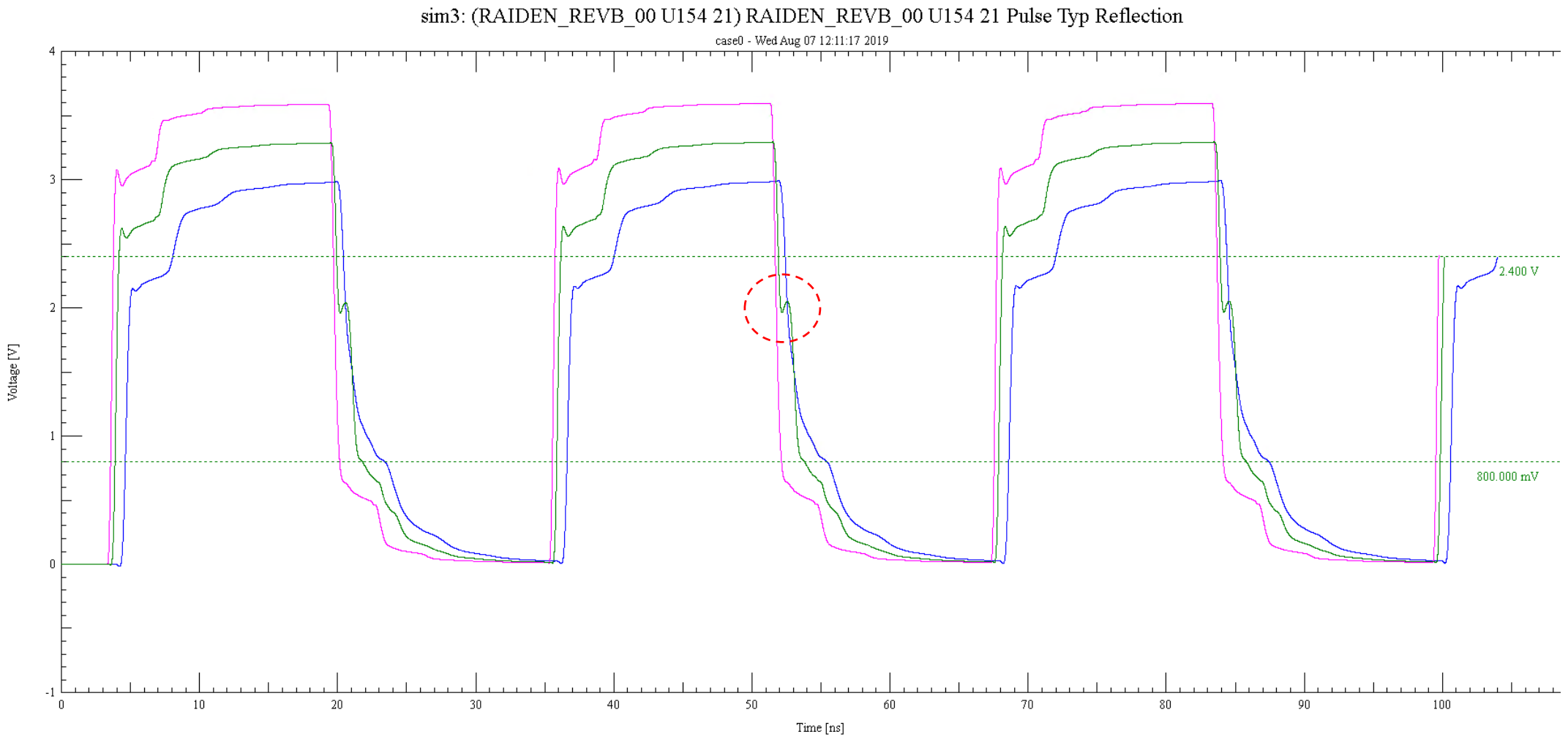
HVVI 3.3V



HV1_VDAC_SPI_SCLK_S50_H at U53AH.3
Green – simulation waveform with non-monotonic falling edge
Yellow - measurement



HV1_VDAC_SPI_SCLK_S50_H at U53AH.3
Simulation for fast, typ and slow cases
Typical case showed non-monotonic falling edge for typical case. Fast ans slow cases seem to be okay.



The non-monotonic falling edge seems to be due to some issue in how the VI and ramp interacts with the package parasitic in the model itself. Tested the model with a simple connection with no transmission line and it shows the same shelf. When remove the package effects, it's a smoother edge. Here is a compare of the fast typ and slow with and without package parasitics.

They all show some strange slow changes without the package. Then when add the packacge in, it shows up as a complete reversal in the typ case. There is something still there in the Fast and slow cases, but not as notiecable.

Maybe a bad relation of Ramp data to the package R L C values.