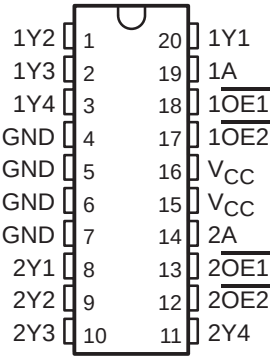
- **CDC209 Replaces 74AC11208**
- **CDC209-7 Replaces 74AC11208-7**
- **Low-Skew Propagation Delay Specifications for Clock-Driver Applications**
- **CMOS-Compatible Inputs and Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Characterized for Operation at 5-V and 3.3-V V_{CC}**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline Package (DW) and Standard Plastic 300-mil DIPs (N)**

DW OR N PACKAGE
(TOP VIEW)



description

The CDC209/209-7 contains dual clock-driver circuits that fanout one input signal to four outputs with minimum skew for clock distribution (see Figure 2). The device also offers two output-enable ($\overline{OE1}$ and $\overline{OE2}$) inputs for each circuit that can force the outputs to be disabled to a high-impedance state or to a high- or low-logic level independent of the signal on the respective A input.

Skew parameters are specified for a reduced temperature and voltage range common to many applications.

The CDC209/209-7 is characterized for operation from $T_A = -40°C$ to 85°C.

FUNCTION TABLES

INPUTS			OUTPUTS			
$1\overline{OE1}$	$1\overline{OE2}$	1A	1Y1	1Y2	1Y3	1Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

INPUTS			OUTPUTS			
$2\overline{OE1}$	$2\overline{OE2}$	2A	2Y1	2Y2	2Y3	2Y4
L	L	L	L	L	L	L
L	L	H	H	H	H	H
L	H	X	L	L	L	L
H	L	X	H	H	H	H
H	H	X	Z	Z	Z	Z

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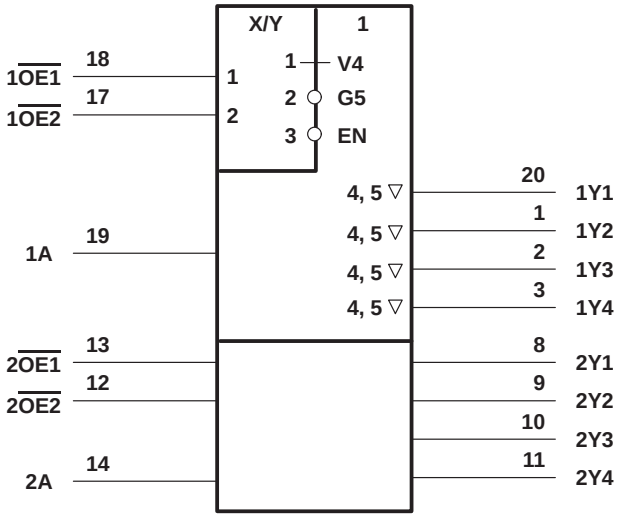
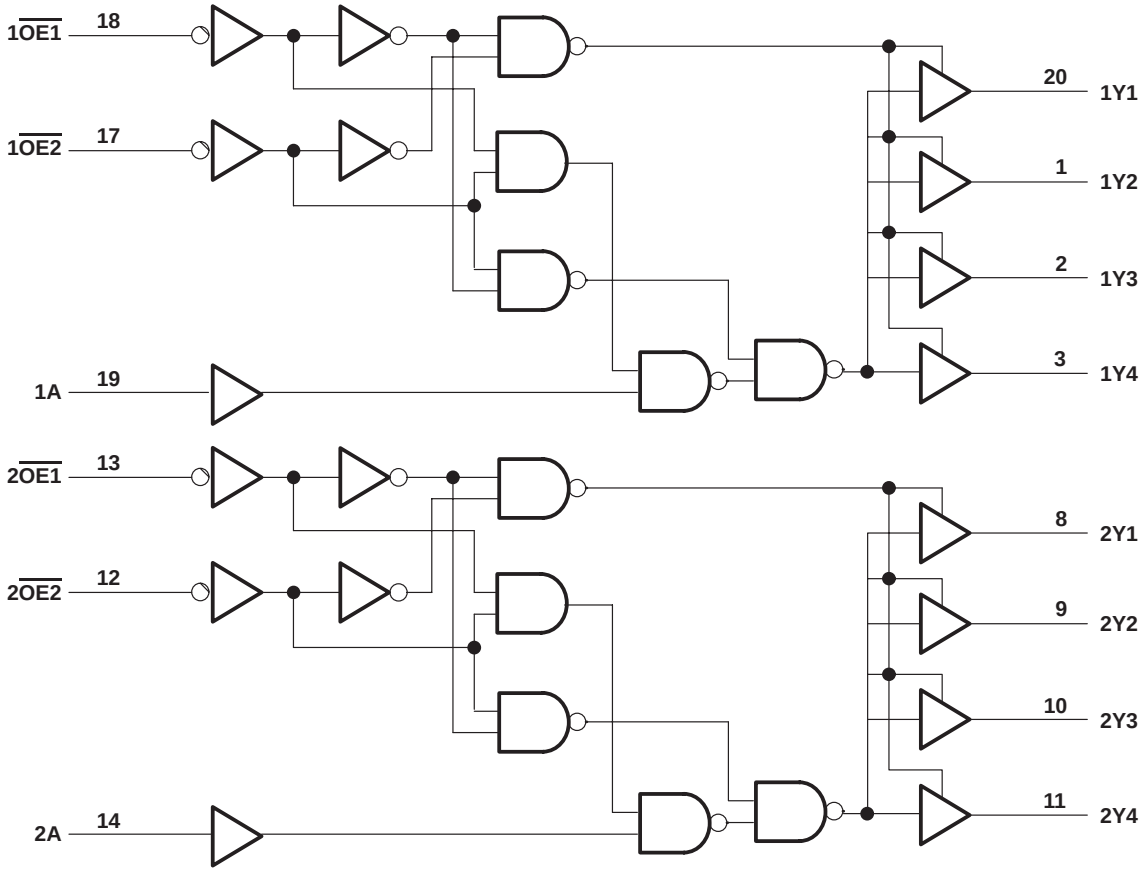
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DW package . . . . . 1.6 W
N package . . . . . 1.3 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4	mA
		V_{CC} = 4.5 V			–24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
f_{clock}	Input clock frequency				60	MHz
T_A	Operating free-air temperature		–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –50 μA	V_{CC} = 3 V	25°C	2.9			V
				Full range	2.9			
			V_{CC} = 4.5 V	25°C	4.4			
				Full range	4.4			
			V_{CC} = 5.5 V	25°C	5.4			
				Full range	5.4			
		I_{OH} = –4 mA	V_{CC} = 3 V	25°C	2.58			
				Full range	2.48			
		I_{OH} = –24 mA	V_{CC} = 4.5 V	25°C	3.94			
				Full range	3.8			
			V_{CC} = 5.5 V	25°C	4.94			
				Full range	4.8			
		I_{OH} = –75 mA‡,	V_{CC} = 5.5 V	Full range	3.85			
V_{OL}	Low-level output voltage	I_{OL} = 50 μA	V_{CC} = 3 V	25°C			0.1	V
				Full range			0.1	
			V_{CC} = 4.5 V	25°C			0.1	
				Full range			0.1	
			V_{CC} = 5.5 V	25°C			0.1	
				Full range			0.1	
		I_{OL} = 12 mA	V_{CC} = 3 V	25°C			0.36	
				Full range			0.44	
		I_{OL} = 24 mA	V_{CC} = 4.5 V	25°C			0.36	
				Full range			0.44	
			V_{CC} = 5.5 V	25°C			0.36	
				Full range			0.44	
		I_{OL} = 75 mA‡,	V_{CC} = 5.5 V	Full range			1.65	
I_I	Input current	V_I = V_{CC} or GND	V_{CC} = 5.5 V	25°C			±0.1	μA
				Full range			±1	
I_{OZ}	High-impedance output current	V_O = V_{CC} or GND	V_{CC} = 5.5 V	25°C			±0.5	μA
				Full range			±5	
I_{CC}	Supply current	V_I = V_{CC} or GND, I_O = 0	V_{CC} = 5.5 V	25°C			8	μA
				Full range			80	
C_i	Input capacitance	V_I = V_{CC} or GND	V_{CC} = 5 V	25°C		4		pF
C_o	Output capacitance	V_O = V_{CC} or GND	V_{CC} = 5 V	25°C		10		pF

† Full range is T_A = –40°C to 85°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level	1A and 2A	Any Y	25°C	4.8	11.1	13.1	ns
				Full range	4.8		14.6	ns
t_{PHL}	Propagation delay time, high-to-low level	1A and 2A	Any Y	25°C	5.1	12.2	14.3	ns
				Full range	5.1		15.6	ns
t_{PLH}	Propagation delay time, low-to-high level	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	25°C	5.2	11.9	14.2	ns
				Full range	5.2		15.8	ns
t_{PHL}	Propagation delay time, high-to-low level	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	25°C	7.8	13.3	15.7	ns
				Full range	7.8		17.4	ns
t_{PZH}	Enable time to the high level	1OE2 or 2OE2	Any Y	25°C	5.1	11.8	14.2	ns
				Full range	5.1		15.7	ns
t_{PZL}	Enable time to the low level	1OE1 or 2OE1	Any Y	25°C	6.8	16.3	19.5	ns
				Full range	6.8		22.8	ns
t_{PHZ}	Disable time from the high level	1OE2 or 2OE2	Any Y	25°C	3.4	6.9	8.6	ns
				Full range	3.4		9.2	ns
t_{PLZ}	Disable time from the low level	1OE1 or 2OE1	Any Y	25°C	4.1	7.5	9.4	ns
				Full range	4.1		10.2	ns

† Full range is T_A = –40°C to 85°C.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	T_A†	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level	1A and 2A	Any Y	25°C	4.2	5.5	9	ns
				Full range	4.2		9.9	
t_{PHL}	Propagation delay time, high-to-low level	1A and 2A	Any Y	25°C	4.2	7	9.3	ns
				Full range	4.2		10.1	
t_{PLH}	Propagation delay time, low-to-high level	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	25°C	4.6	7.3	9.6	ns
				Full range	4.6		10.7	
t_{PHL}	Propagation delay time, high-to-low level	$1\overline{OE1}$, $1\overline{OE2}$, and $2\overline{OE1}$, $2\overline{OE2}$	Any Y	25°C	4.8	7.7	10.2	ns
				Full range	4.8		11	
t_{PZH}	Enable time to the high level	1OE2 or 2OE2	Any Y	25°C	4.3	7.2	9.4	ns
				Full range	4.3		4	
t_{PZL}	Enable time to the low level	1OE1 or 2OE1	Any Y	25°C	5.3	9	12.2	ns
				Full range	5.3		13.5	
t_{PHZ}	Disable time from the high level	1OE2 or 2OE2	Any Y	25°C	3	5.4	7.5	ns
				Full range	3		8	
t_{PLZ}	Disable time from the low level	1OE1 or 2OE1	Any Y	25°C	3.7	5.7	7.5	ns
				Full range	3.7		8.2	

† Full range is T_A = –40°C to 85°C.

switching characteristics, V_{CC} = 5 V ± 0.25 V, T_A = 25°C to 70°C (see Note 3 and Figures 1 and 2)

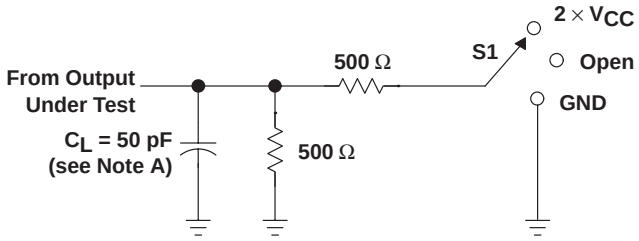
PARAMETER		FROM (INPUT)	TO (OUTPUT)	CDC209		CDC209-7		UNIT
				MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high level	1A and 2A	Any Y	6	8.5	6	8.5	ns
t_{PHL}	Propagation delay time, high-to-low level			6	9.3	6	9.3	
$t_{sk(o)}$	output skew time	1A and 2A	Any Y		1		0.7	ns

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

operating characteristics, V_{CC} = 5 V, T_A = 25°C

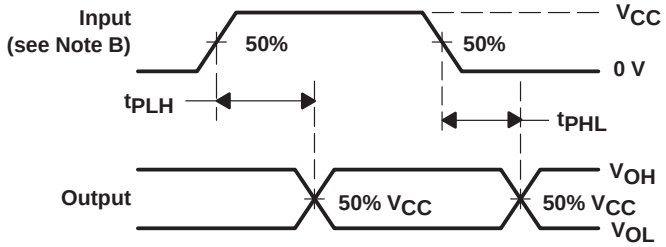
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per bank	Outputs enabled	C_L = 50 pF,	f = 1 MHz		95		pF
		Outputs disabled				10		

PARAMETER MEASUREMENT INFORMATION

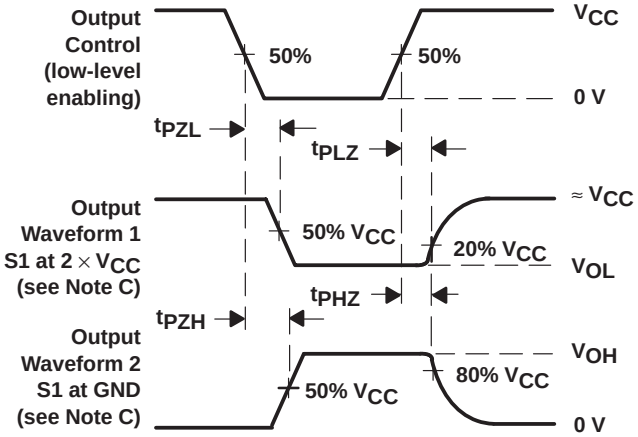


LOAD CIRCUIT FOR OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

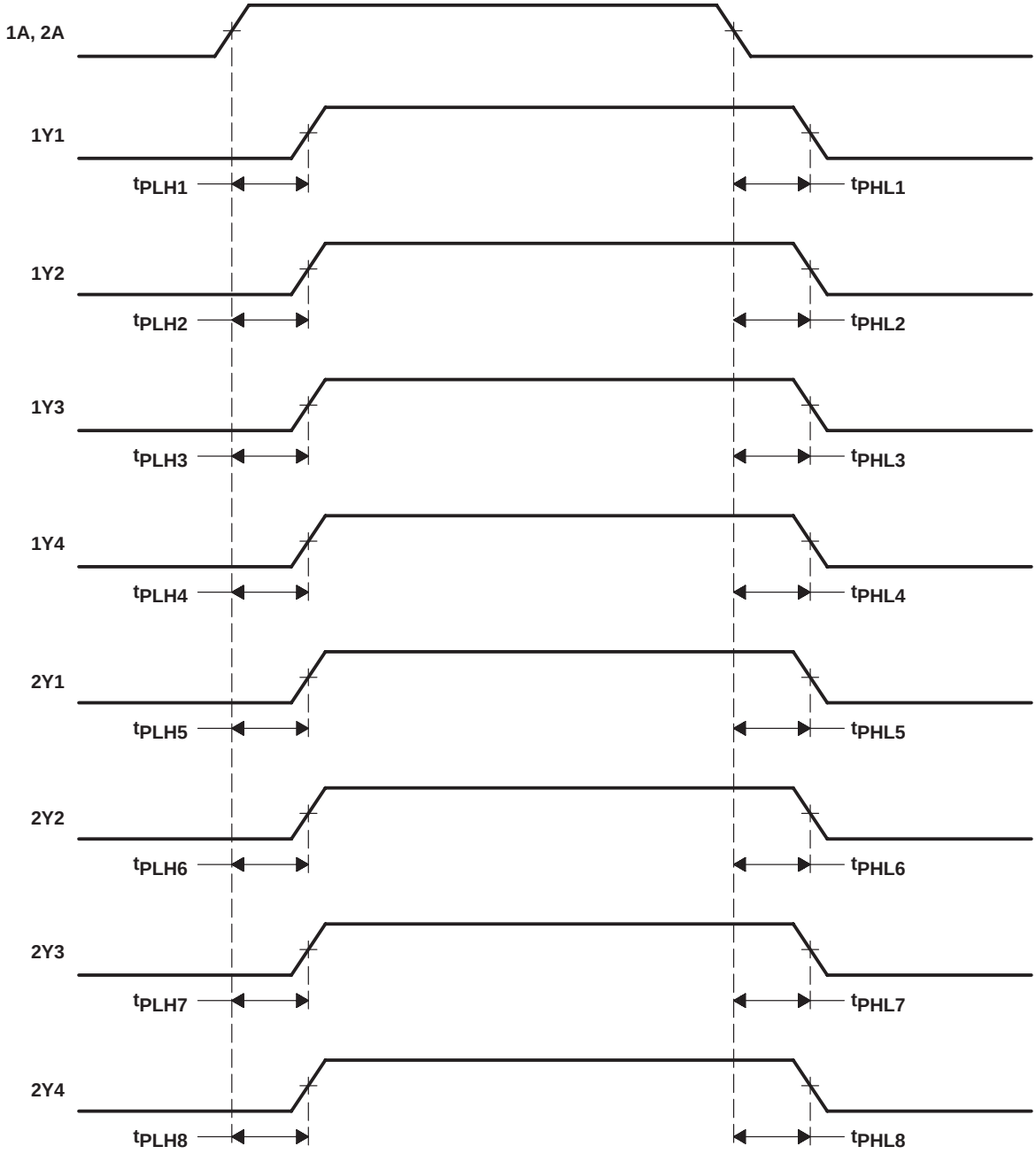


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns. For testing pulse duration: t_r = t_f = 1 to 3 ns. Pulse polarity can be either high-to-low-to-high or low-to-high-to-low.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



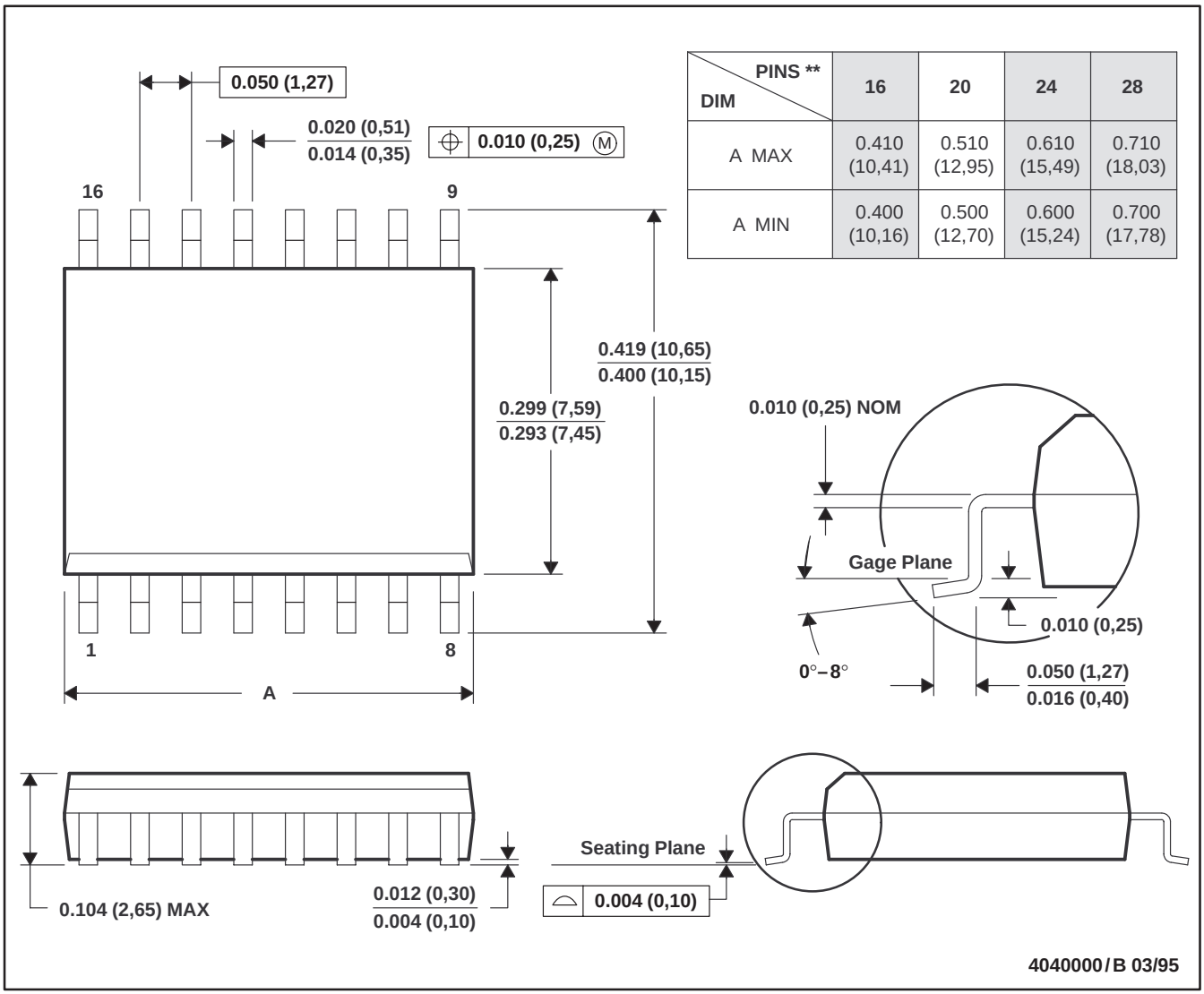
NOTE D: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 8)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

MECHANICAL INFORMATION

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

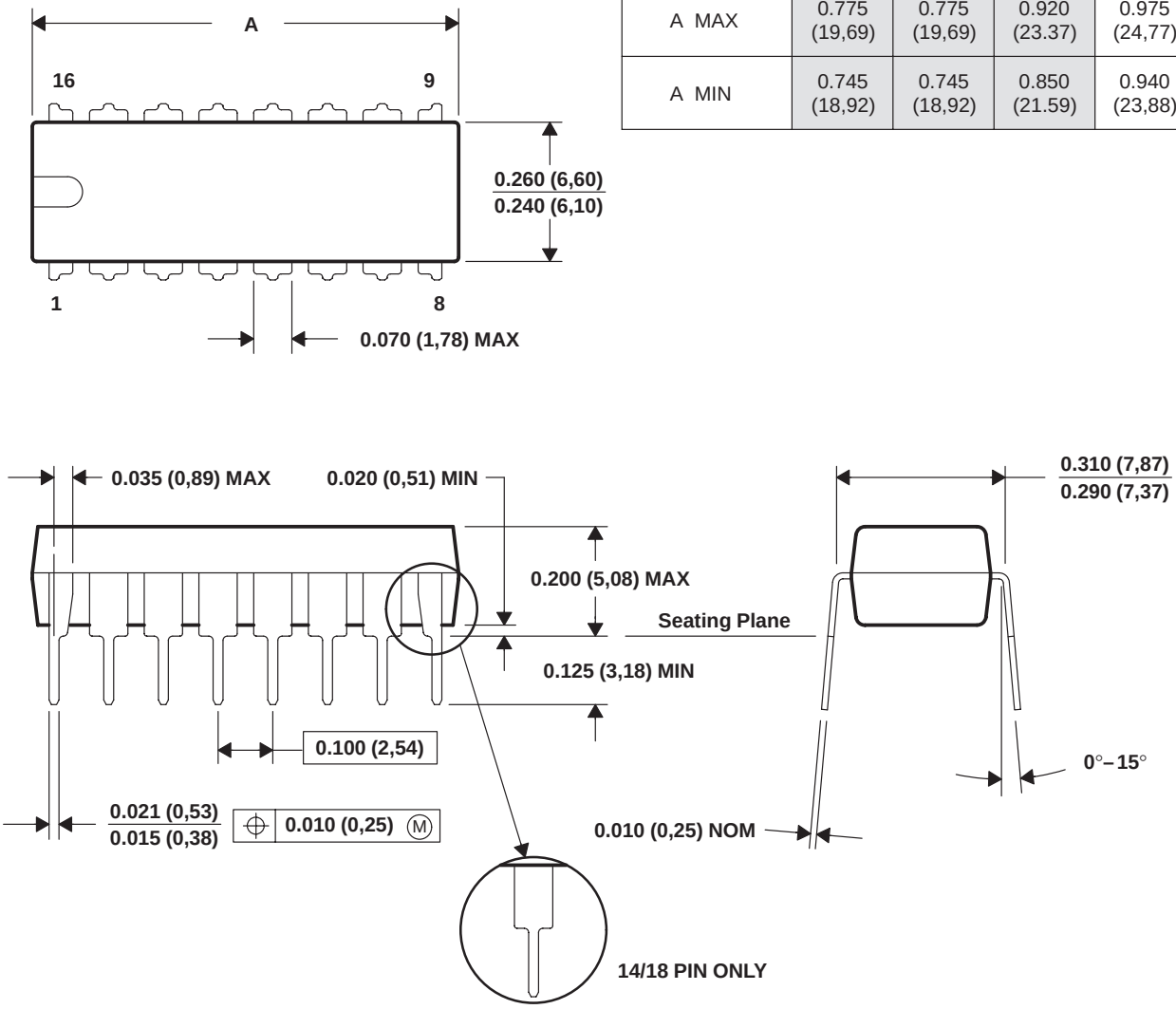
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL INFORMATION

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20 pin package is shorter then MS-001.)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CDC209-7DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
CDC209-7DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
CDC209DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
CDC209DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
CDC209DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
CDC209N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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