Texas Instruments Voltage-Level-Translation Devices

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ABSTRACT

In electronic systems design, there is a need to provide an interface between different voltage levels. Texas Instruments offers four split-rail bus transceivers with dual voltage-supply inputs. These transceivers allow translation between 3.3-V LVTTL/LVCMOS and 5-V CMOS, 2.5-V CMOS and 5-V CMOS, and 2.5-V CMOS and 3.3-V LVTTL/LVCMOS. These devices are the SN74LVCC3245A, SN74LVC4245A, SN74LVCC4245A, and SN74ALVC164245. This application report discusses the use of these devices to achieve successful voltage translation.

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Introduction

The simultaneous use of different supply-voltage levels has led to the need for voltage translation. In some cases, the logic devices are compatible with the different voltage levels, while in other cases they are not. To have switching compatibility between a driver and a receiver, the output of the driver must be compliant with the input of the receiver. V_{OL} of the driver should be equal to, or less than, V_{IL} of the receiver. To establish a high-level signal at the receiver, V_{OH} of the driver should be greater than, or equal to, V_{IH} (see Figure 1).

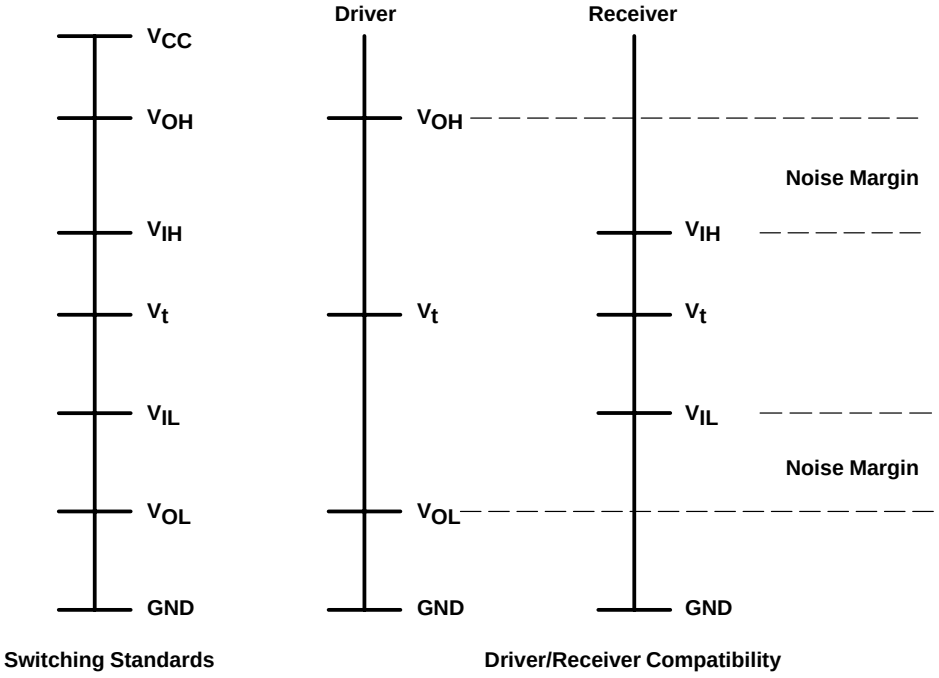


Figure 1. Switching Standards

While translating from 3.3-V LVTTL/LVCMOS to 5-V CMOS, V_{IH} for 5-V CMOS is 3.5 V, whereas V_{OH} for 3.3-V LVTTL is 2.4 V (see Figure 2).

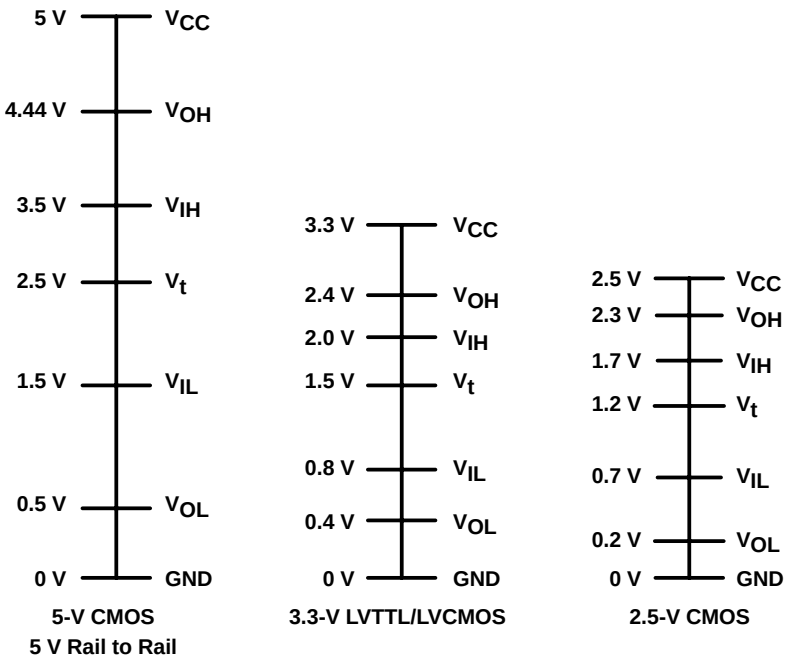


Figure 2. Comparison of Switching Standards

Thus, standard 3.3-V devices cannot achieve this type of translation. Texas Instruments split-rail devices have two separate voltage supplies, one at each port. These devices allow for translation between 3.3-V LVTTL/LVCMOS to 5-V CMOS, 2.5-V CMOS to 5-V CMOS, 2.5-V CMOS to 3.3-V LVTTL/LVCMOS, and vice versa.

Device Description

Dual-Supply Bus Transceivers

The SN74LVC4245A (see Figure 3) is an 8-bit (octal) noninverting bus transceiver that has two power-supply rails. The A port is set at 5 V, while the B port is set at 3.3 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa. The data is transmitted from the A bus to the B bus, or the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. If the buses must be isolated, the device can be disabled using the output-enable ($\overline{OE}$) input.

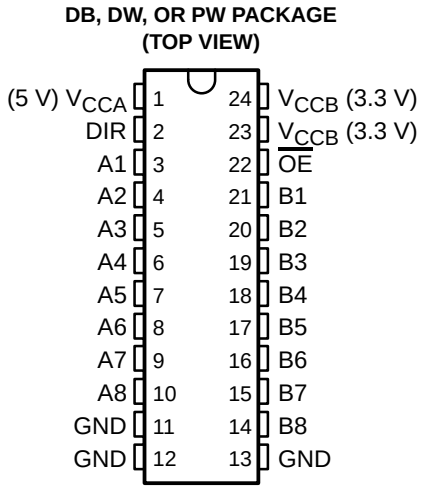


Figure 3. SN74LVC4245A Pinout

The SN74ALVC164245 (see Figure 4) is a 16-bit (dual-octal) noninverting bus transceiver. Its operation is similar to the SN74LVC4245A. The only functional difference is that, in the case of the SN74ALVC164245, V_{CCA} is set to 3.3 V, and V_{CCB} is set to 5 V, the opposite of the SN74LVC4245A configuration.

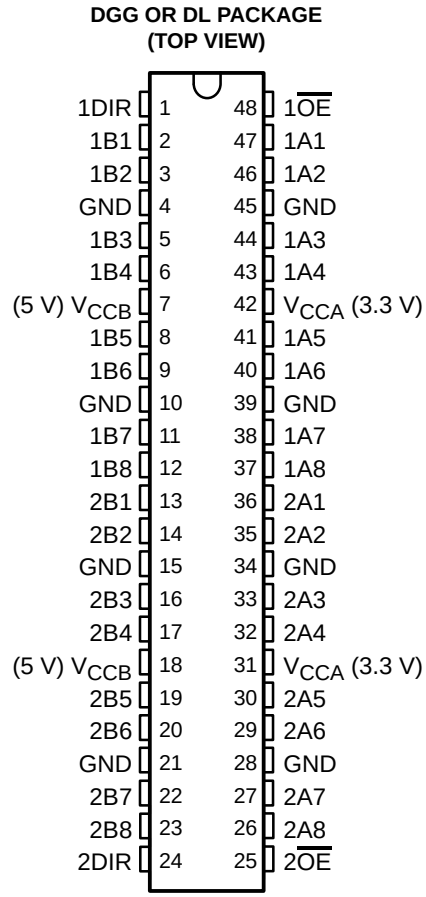


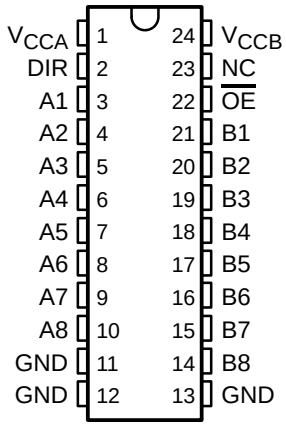
Figure 4. SN74ALVC164245 Pinout

V_{CCA} is the control side for these two devices. Therefore, the control inputs, DIR (direction) and $\overline{OE}$ (output enable), should be driven by V_{CCA} CMOS logic. For the SN74LVC4245A, DIR and $\overline{OE}$ should be driven by 5-V CMOS logic. For the SN74ALVC16425, DIR and $\overline{OE}$ should be driven by 3.3-V CMOS logic.

Configurable-Output Bus Transceivers

The SN74LVCC3245A and SN74LVCC4245A are 8-bit (octal) dual-supply bus transceivers with configurable output voltages. This means the data on the B bus follow the value of V_{CCB}. In the SN74LVCC3245A, V_{CCA} operates between 2.3 V and 3.6 V, while V_{CCB} accepts voltages from 3 V to 5.5 V. This device allows translation from 3.3 V to 5 V, 2.5 V to 3.3 V, or 2.5 V to 5 V, and vice versa. The SN74LVCC4245A operates slightly differently. V_{CCA} accepts a 5-V supply level, and V_{CCB} accepts voltages from 3 V to 5 V. Therefore, this device translates only between 3.3 V and 5 V. SN74LVCC3245A and SN74LVCC4245A are shown in Figure 5 and Figure 6, respectively.

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

Figure 5. SN74LVCC3245A Pinout

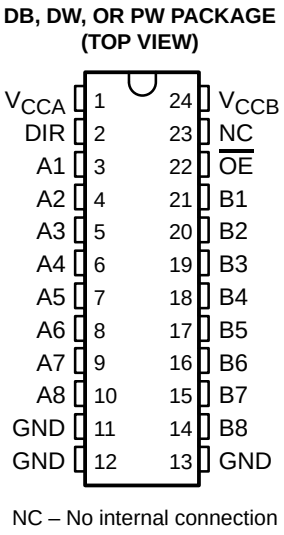


Figure 6. SN74LVCC4245A Pinout

V_{CCA} is the control side for these two devices. Therefore, the control inputs should be driven by V_{CCA} CMOS logic. For the SN74LVCC4245A, DIR and $\overline{OE}$ should be driven by 5-V CMOS logic, and for the SN74LVCC3245A, DIR and $\overline{OE}$ should be driven by 3.3-V CMOS logic.

Table 1 details possible voltage-translation combinations.

Table 1. Possible Voltage-Translation Combinations

DEVICE	SUPPLY VOLTAGE	POSSIBLE VOLTAGE-TRANSLATION COMBINATIONS (TO/FROM)	
		A PORT	B PORT
SN74LVC4245A	$4.5\ V \le V_{CCA} \le 5.5\ V$ $2.7\ V \le V_{CCB} \le 3.6\ V$	5-V CMOS	3.3-V LVTTL/LVCMOS
SN74ALVC164245A	$2.7\ V \le V_{CCA} \le 3.6\ V$ $4.5\ V \le V_{CCB} \le 5.5\ V$	3.3-V LVTTL/LVCMOS	5-V CMOS
SN74LVCC3245A	$2.3\ V \le V_{CCA} \le 3.6\ V$ $3\ V \le V_{CCB} \le 5.5\ V$	2.5-V CMOS	3.3-V LVTTL/LVCMOS
		2.5-V CMOS	5-V CMOS
		3.3-V LVTTL/LVCMOS	5-V CMOS
		3.3-V LVTTL/LVCMOS	3.3-V LVTTL/LVCMOS
SN74LVCC4245A	$4.5\ V \le V_{CCA} \le 5.5\ V$ $2.7\ V \le V_{CCB} \le 5.5\ V$	5-V CMOS	3.3-V LVTTL/LVCMOS
		5-V CMOS	5-V CMOS

Features and Benefits

Table 2 summarizes the features and corresponding benefits of these level-translation devices.

Table 2. Features and Benefits of Level-Translation Devices

FEATURES	DEVICES	BENEFITS
Two separate power-supply rails: V_{CCB} at the B port takes 3.3 V, V_{CCA} at the A port takes 5 V.	SN74LVC4245A SN74LVCC4245A	Allows 3.3-V to 5-V level translation, and vice versa
Two separate power-supply rails: V_{CCB} at the B port takes 5 V, V_{CCA} at the A port takes 3.3 V.	SN74ALVC164245	Allows 3.3-V to 5-V level translation, and vice versa
Two separate power-supply rails: V_{CCB} at the B port takes 5 V, V_{CCA} at the A port takes 2.5 V to 3.3 V.	SN74LVCC3245A	Allow 3.3-V to 5-V, 2.5-V to 3.3-V, and 2.5-V to 5-V level translations, and vice versa
Output enable can be used to disable the device.	SN74LVC4245A SN74LVCC4245A SN74ALVC164245 SN74LVCC3245A	Buses are isolated effectively without false signaling, when necessary.
B port is configurable, which means B port is designed to track V_{CCB}.	SN74LVCC4245A SN74LVCC3245A	Some real-time applications, such as PCMCIA, need full-rail data signals to maximize interface capability, which can be accomplished by tying V_{CCB} of the device to the PCMCIA card voltage supply.

Power-Up Considerations

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

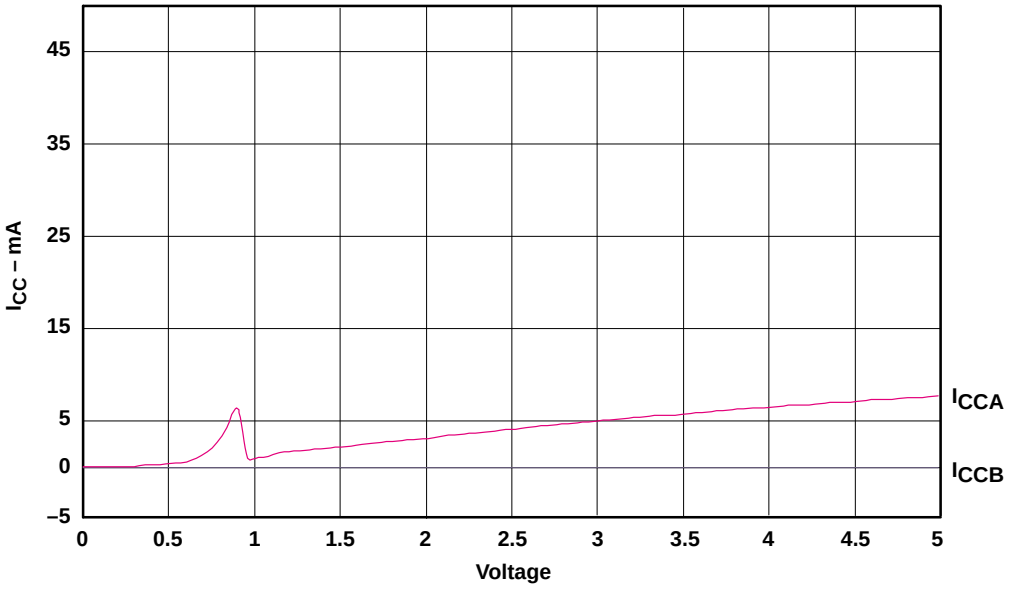
1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

Table 3 gives a brief summary about the power-up sequence of the devices.

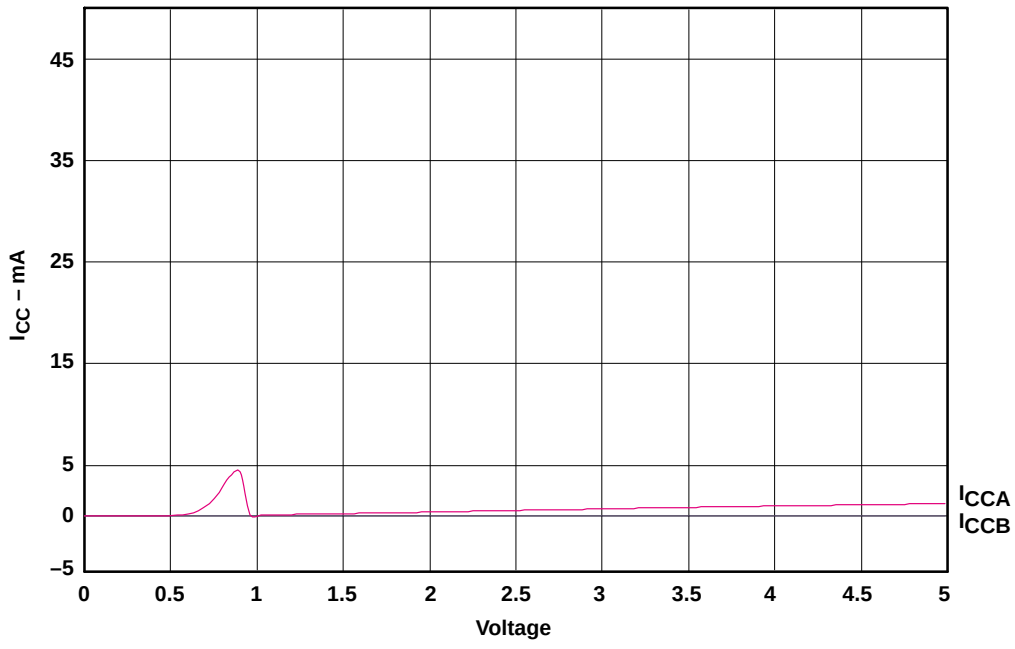
Table 3. Power-Up Sequence for Level-Translation Devices

DEVICE	V_{CCA}	V_{CCB}	$\overline{OE}$
SN74LVC4245A	5 V (power up first)	3.3 V (power up second)	Tied to V_{CCA} with a pullup resistor
SN74LVCC4245A	5 V (power up first)	3.3 V (power up second)	Tied to V_{CCA} with a pullup resistor
SN74LVCC3245A	3.3 V (power up first)	5 V (power up second)	Tied to V_{CCA} with a pullup resistor
SN74ALVC164245	3.3 V (power up first)	5 V (power up second)	Tied to V_{CCA} with a pullup resistor

The power-up sequence was tested in the laboratory for all four of these devices. Figures 7–10 show the I_{CCA} and I_{CCB} for the SN74LVC4245A, SN74LVCC4245A, SN74LVCC3245A, and SN74ALVC164245 devices during power up. V_{CCA} was powered up first, then V_{CCB} was applied. $\overline{OE}$ was tied to V_{CCA} with a 1-kΩ pullup resistor. Figures 7(a)–10(a) show the I_{CC} with DIR high, and Figures 7(b)–10(b) show the I_{CC} with DIR low. If the device is powered up in the correct manner, it draws a reasonable amount of current and ensures the proper functioning of the device.

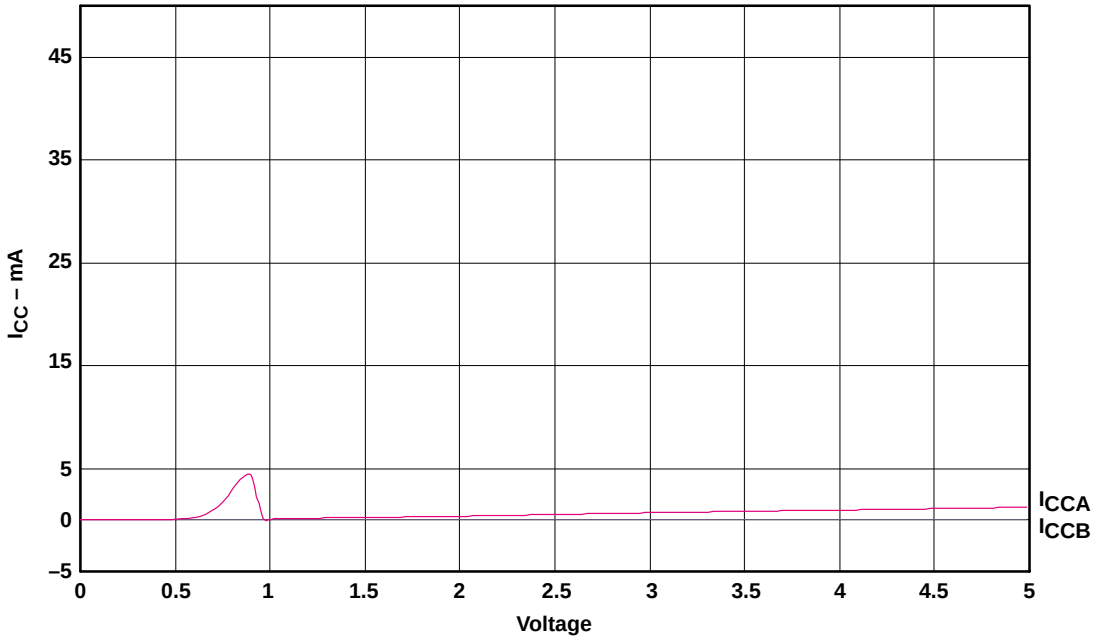


a) SN74LVC4245A POWER UP WITH DIR HIGH

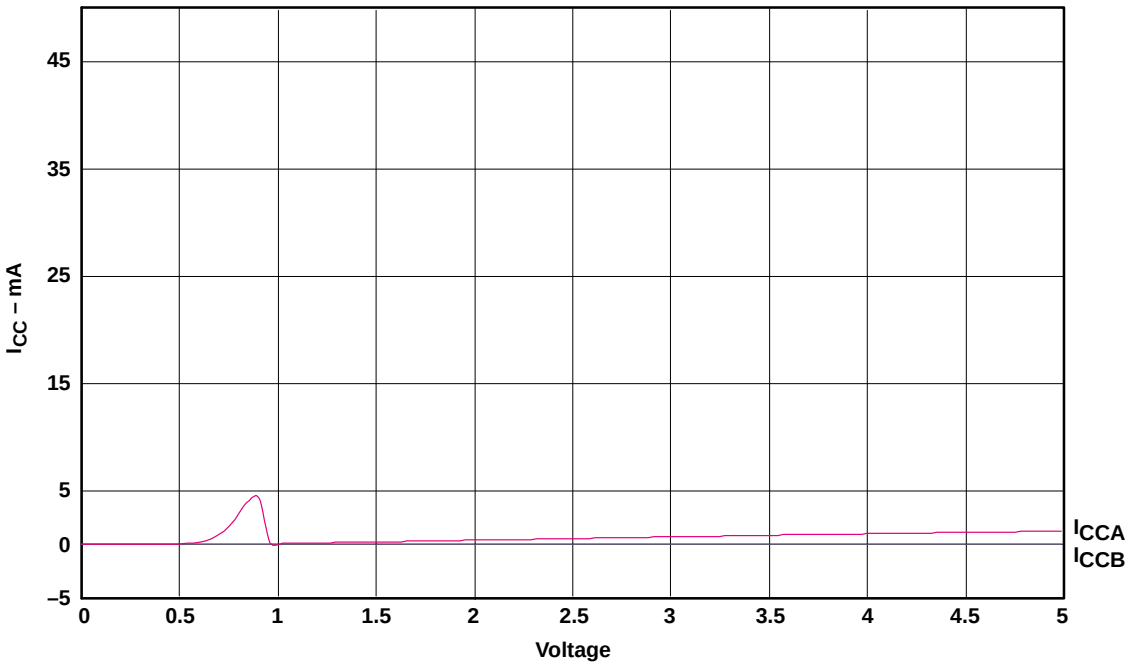


b) SN74LVC4245A POWER UP WITH DIR LOW

Figure 7. SN74LVC4245A I_{CCA} and I_{CCB}

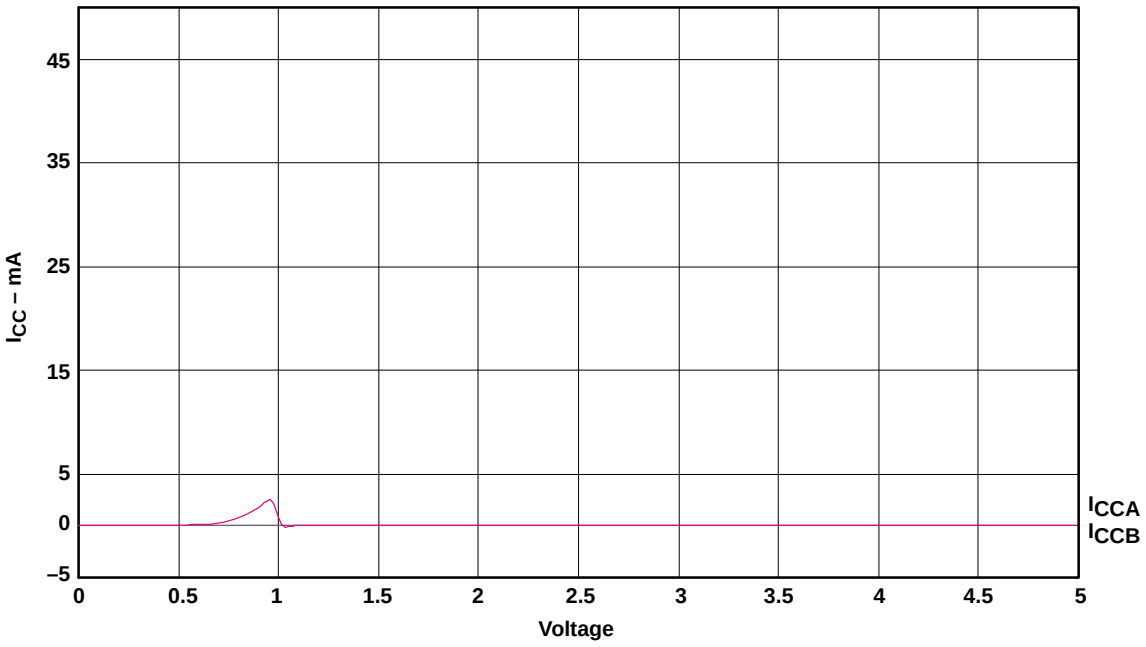


a) SN74LVCC4245A POWER UP WITH DIR HIGH

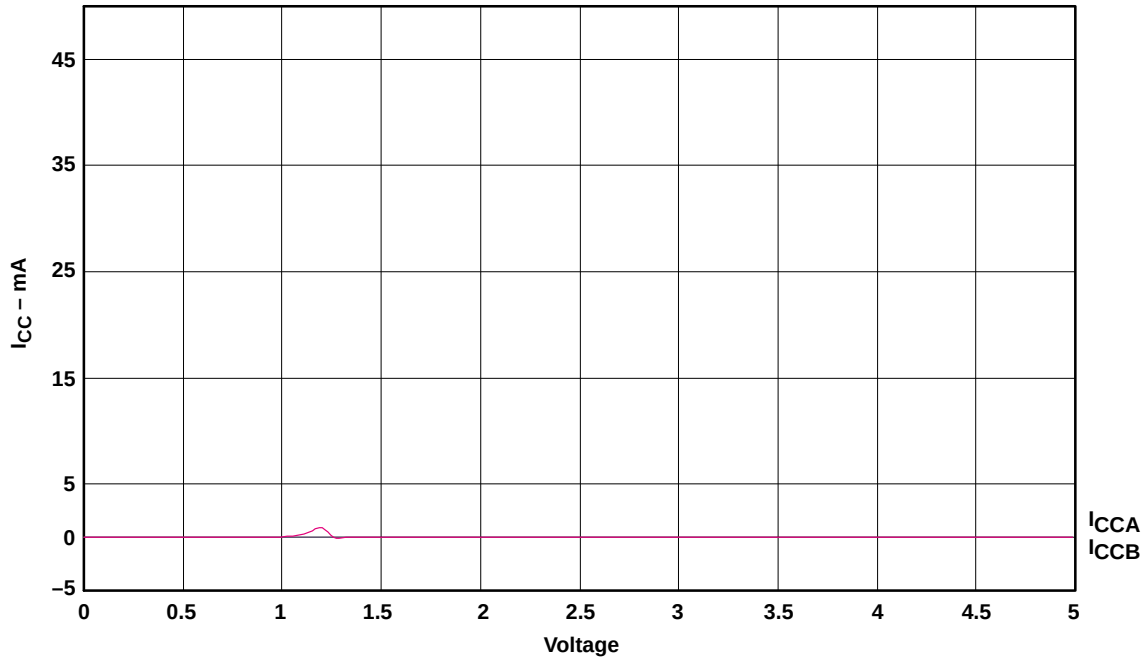


b) SN74LVCC4245A POWER UP WITH DIR LOW

Figure 8. SN74LVCC4245A I_{CCA} and I_{CCB}

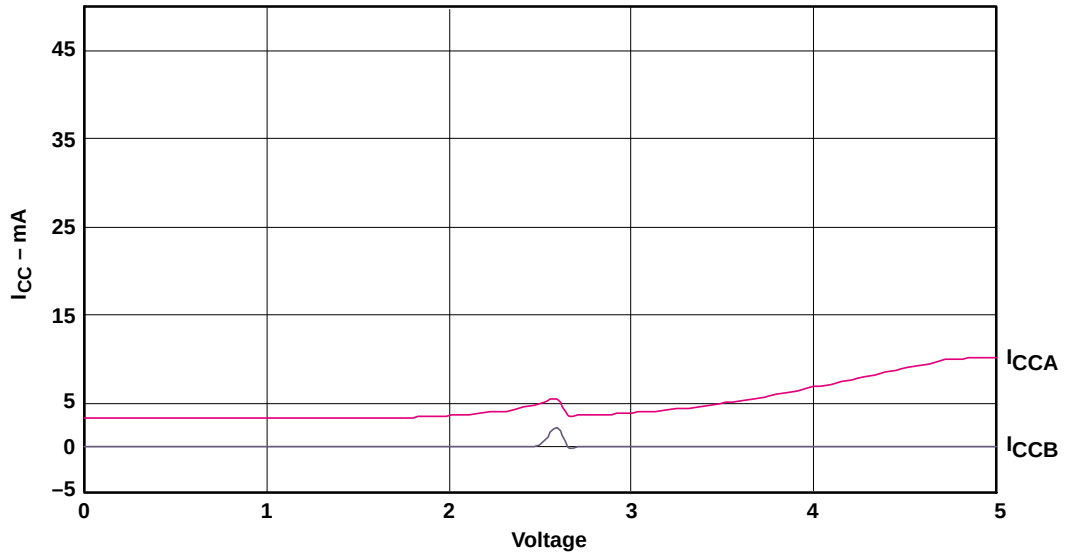


a) SN74LVCC3245A POWER UP WITH DIR HIGH

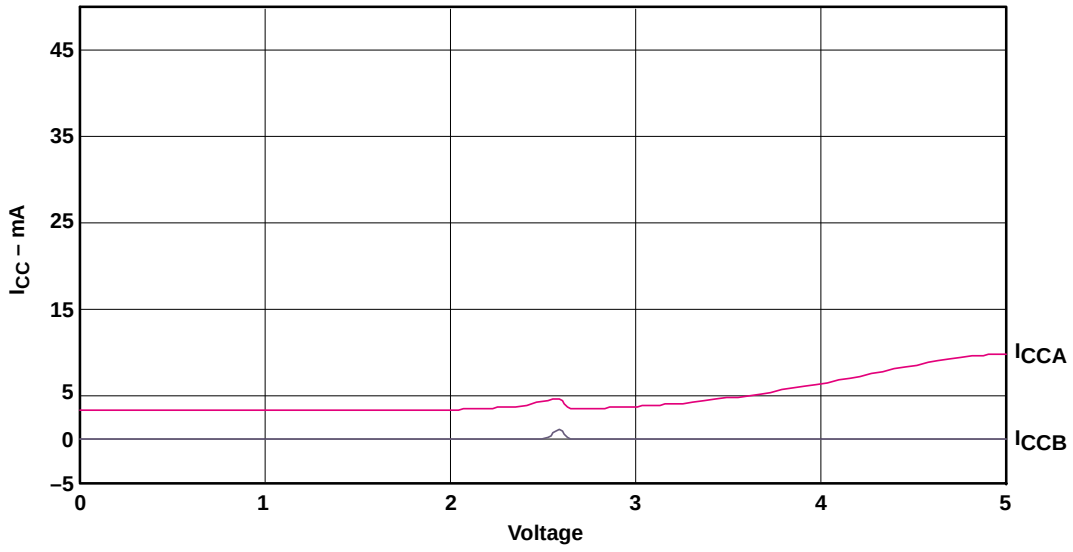


b) SN74LVCC3245A POWER UP WITH DIR LOW

Figure 9. SN74LVCC3245A I_{CCA} and I_{CCB}



a) SN74ALVC164245 POWER UP WITH DIR HIGH



b) SN74ALVC164245 POWER UP WITH DIR LOW

Figure 10. SN74ALVC164245 I_{CCA} and I_{CCB}

Conclusion

Texas Instruments offers four split-rail devices, SN74LVC4245A, SN74LVCC4245A, SN74LVCC3245A, and SN74ALVC164245 that can be used for 3.3-V to 5-V, 2.5-V to 3.3-V, and 2.5-V to 5-V translation, and vice versa. These devices are available in octal and Widebus™ configurations, which give the opportunity for designers to choose the optimal part for their applications. These devices have strict power-sequencing requirements that prevent excessive current flow or possible damage to the devices. These stringent requirements sometimes are difficult to meet from a system timing standpoint and may offer little flexibility for partial system power down or other advanced power-saving design techniques. Careful selection of these devices and adoption of an appropriate power-up sequencing technique can lead to a successful mixed-voltage design.

Glossary

CMOS	Complementary metal-oxide semiconductor
LVCMOS	Low-voltage CMOS
LVTTL	Low-voltage TTL (3.3-V power supply and interface levels)
V_{CC}	Supply voltage
V_{IH}	High-level input voltage
V_{IL}	Low-level input voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_t	Threshold voltage

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