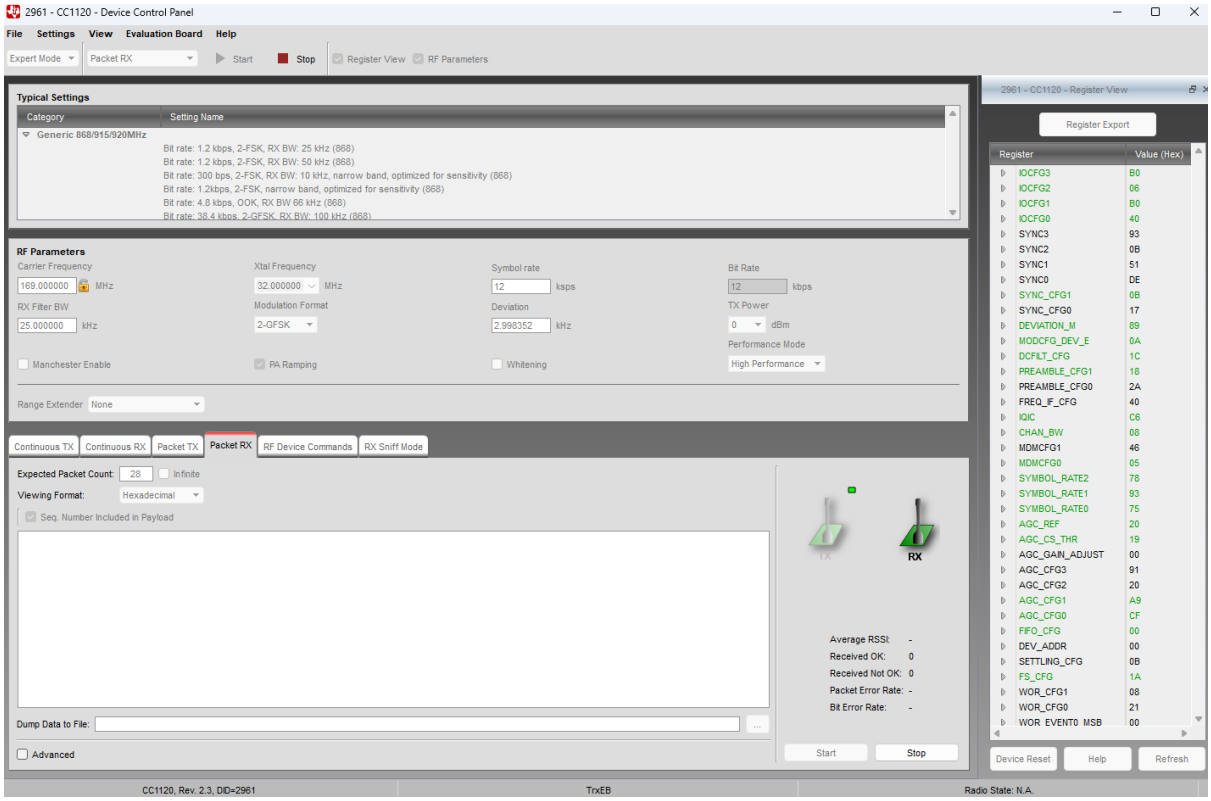
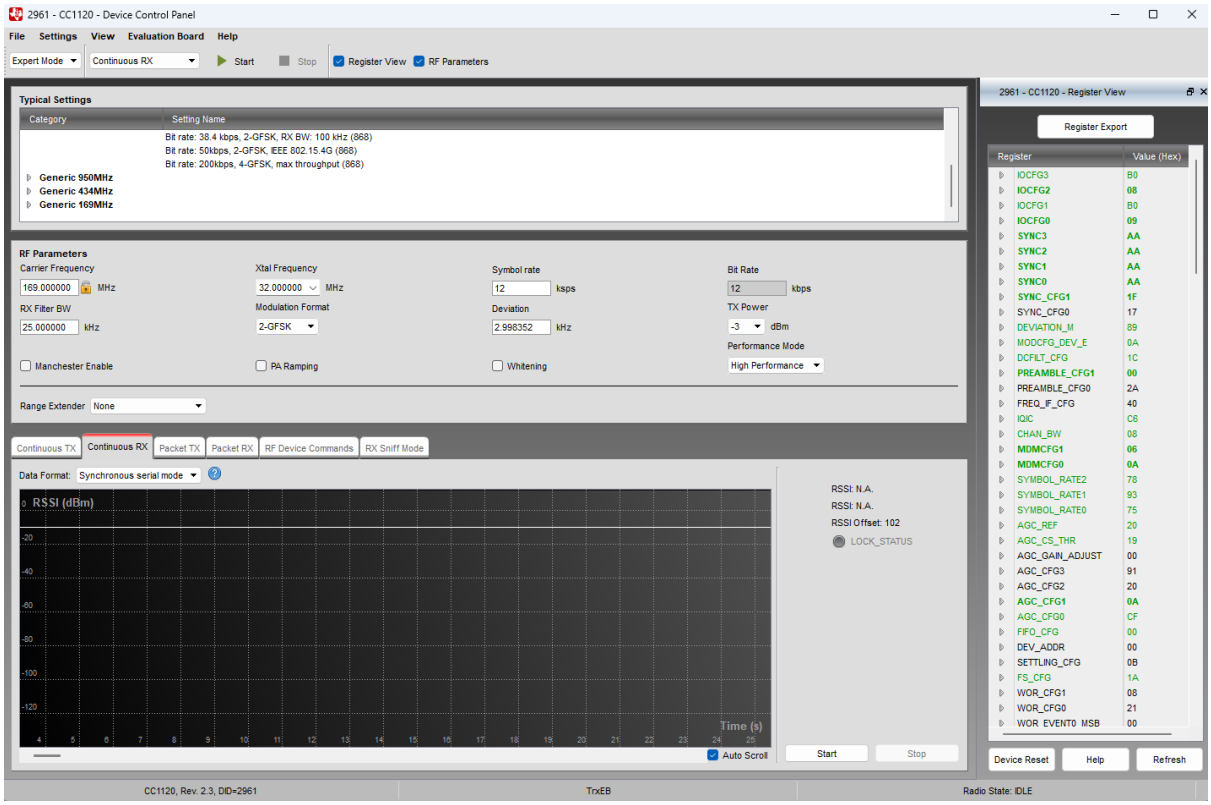
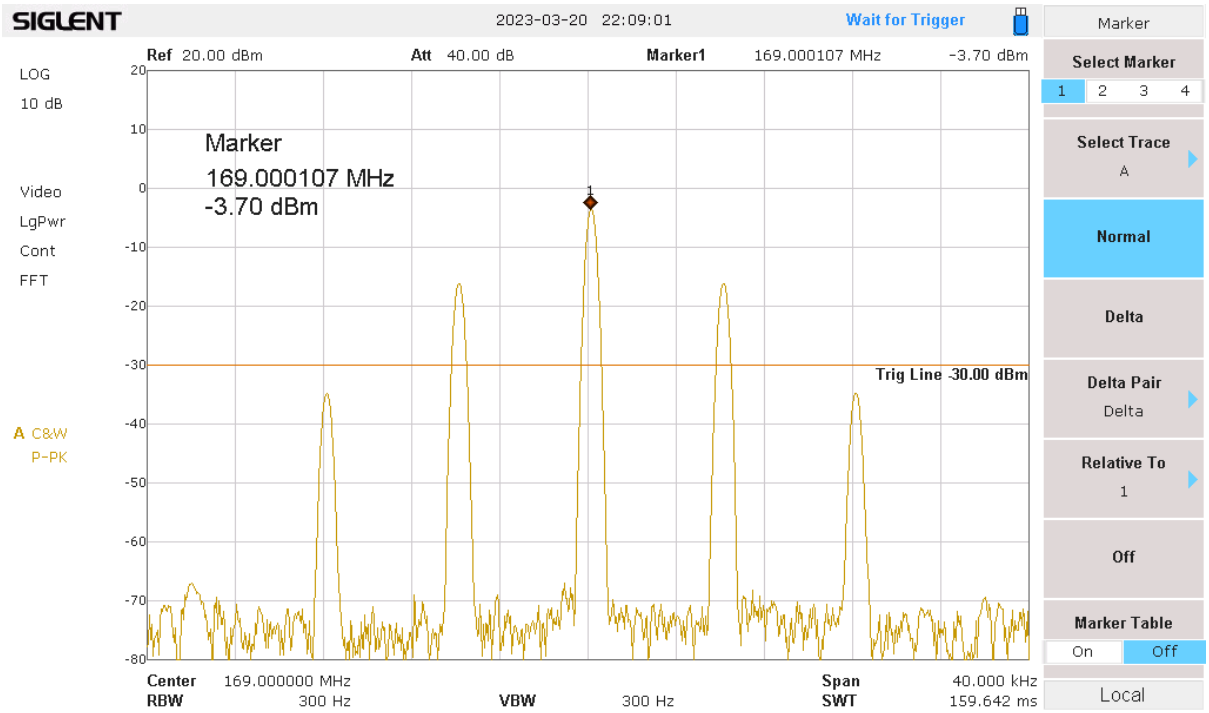

2961 - CC1120 - Device Control Panel
File Settings View Evaluation Board Help
Expert Mode
Packet RX
Start
Stop
Register View
RF Parameters
Typical Settings
Category
Setting Name
Generic 868/915/920MHz
Bit rate: 1.2 kbps, 2-FSK, RX BW: 25 kHz (868)
Bit rate: 1.2 kbps, 2-FSK, RX BW: 50 kHz (868)
Bit rate: 300 bps, 2-FSK, RX BW: 10 kHz, narrow band, optimized for sensitivity (868)
Bit rate: 1.2kbps, 2-FSK, narrow band, optimized for sensitivity (868)
Bit rate: 4.8 kbps, OOK, RX BW 66 kHz (868)
Bit rate: 38.4 kbps, 2-GFSK, RX BW: 100 kHz (868)
RF Parameters
Carrier Frequency
169.000000
MHz
Xtal Frequency
32.000000
MHz
Symbol rate
12
ksps
Bit Rate
12
kbps
RX Filter BW
25.000000
kHz
Modulation Format
2-GFSK
Deviation
2.998352
kHz
TX Power
0
dBm
Performance Mode
High Performance
Manchester Enable
PA Ramping
Whitening
Range Extender
None
Continuous TX
Continuous RX
Packet TX
Packet RX
RF Device Commands
RX Sniff Mode
Expected Packet Count:
28
Infinite
Viewing Format:
Hexadecimal
Seq. Number Included in Payload
Dump Data to File:
Advanced
TX
RX
Average RSSI: -
Received OK: 0
Received Not OK: 0
Packet Error Rate: -
Bit Error Rate: -
Start
Stop
2961 - CC1120 - Register View
Register Export
Register
Value (Hex)
IOCFG3 B0
IOCFG2 06
IOCFG1 B0
IOCFG0 40
SYNC3 93
SYNC2 0B
SYNC1 51
SYNC0 DE
SYNC_CFG1 0B
SYNC_CFG0 17
DEVIATION_M 89
MODCFG_DEV_E 0A
DCFILT_CFG 1C
PREAMBLE_CFG1 18
PREAMBLE_CFG0 2A
FREQ_IF_CFG 40
IQIC C6
CHAN_BW 08
MDMCFG1 46
MDMCFG0 05
SYMBOL_RATE2 78
SYMBOL_RATE1 93
SYMBOL_RATE0 75
AGC_REF 20
AGC_CS_THR 19
AGC_GAIN_ADJUST 00
AGC_CFG3 91
AGC_CFG2 20
AGC_CFG1 A9
AGC_CFG0 CF
FIFO_CFG 00
DEV_ADDR 00
SETTLING_CFG 0B
FS_CFG 1A
WOR_CFG1 08
WOR_CFG0 21
WOR_EVENT0_MSB 00
Device Reset
Help
Refresh
CC1120, Rev. 2.3, DID=2961
TrxEB
Radio State: N.A.


2961 - CC1120 - Device Control Panel
File Settings View Evaluation Board Help
Expert Mode
Continuous RX
Start
Stop
Register View
RF Parameters
Typical Settings
Category
Setting Name
Bit rate: 38.4 kbps, 2-GFSK, RX BW: 100 kHz (868)
Bit rate: 50kbps, 2-GFSK, IEEE 802.15.4G (868)
Bit rate: 200kbps, 4-GFSK, max throughput (868)
Generic 950MHz
Generic 434MHz
Generic 169MHz
RF Parameters
Carrier Frequency
169.000000
MHz
Xtal Frequency
32.000000
MHz
Symbol rate
12
ksps
Bit Rate
12
kbps
RX Filter BW
25.000000
kHz
Modulation Format
2-GFSK
Deviation
2.998352
kHz
TX Power
-3
dBm
Performance Mode
High Performance
Manchester Enable
PA Ramping
Whitening
Range Extender
None
Continuous TX
Continuous RX
Packet TX
Packet RX
RF Device Commands
RX Sniff Mode
Data Format:
Synchronous serial mode
RSSI (dBm)
-20
-40
-60
-80
-100
-120
4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
Time (s)
Auto Scroll
RSSI: N.A.
RSSI: N.A.
RSSI Offset: 102
LOCK_STATUS
Start
Stop
2961 - CC1120 - Register View
Register Export
Register
Value (Hex)
IOCFG3 B0
IOCFG2 08
IOCFG1 B0
IOCFG0 09
SYNC3 AA
SYNC2 AA
SYNC1 AA
SYNC0 AA
SYNC_CFG1 1F
SYNC_CFG0 17
DEVIATION_M 89
MODCFG_DEV_E 0A
DCFILT_CFG 1C
PREAMBLE_CFG1 00
PREAMBLE_CFG0 2A
FREQ_IF_CFG 40
IQIC C6
CHAN_BW 08
MDMCFG1 06
MDMCFG0 0A
SYMBOL_RATE2 78
SYMBOL_RATE1 93
SYMBOL_RATE0 75
AGC_REF 20
AGC_CS_THR 19
AGC_GAIN_ADJUST 00
AGC_CFG3 91
AGC_CFG2 20
AGC_CFG1 0A
AGC_CFG0 CF
FIFO_CFG 00
DEV_ADDR 00
SETTLING_CFG 0B
FS_CFG 1A
WOR_CFG1 08
WOR_CFG0 21
WOR_EVENT0_MSB 00
Device Reset
Help
Refresh
CC1120, Rev. 2.3, DID=2961
TrxEB
Radio State: IDLE

SPECTRUM ANALYSER SCREEN SHOT OF THE TRANSMITTING SPECTRUM



```
void        RF_Tx_Start(void)
{
    uint8_t index;

    RF_SPI_Write(SFTX, 0x00, 0x00, 1);                      //0x3B. Flush Tx FIFO.

    SPI_TX_data[0] = TXFIFO;                                //0x7E. Burst mode.
    SPI_TX_data[1] = 0x00;                                  //FIFO address 0.
    SPI_TX_data[2] = 0x1A;                                  //Number of data bytes.

    for(index = 3; index <= 17; ++index)
    {
         SPI_TX_data[index] = 0xFF;
    }

    SPI_SpiUartClearRxBuffer();

    SPI_SpiUartPutArray(SPI_TX_data, 18);                  //Load the data to the CC1125.
    CyDelay(DELAY_1ms);

    SPI_RX_data[0] = 0xFF;

    while((SPI_RX_data[0] & 0xF0) != 0x00)
    {
        RF_SPI_Write(SIDLE, 0x00, 0x00, 1);
        SPI_RX_data[0] = SPI_SpiUartReadRxData();
    }

    RF_SPI_Write(SFSTXON, 0x00, 0x00, 1);                  //0x31. Calibrate and enable the frequency synthesiser.
    SPI_RX_data[0] = 0x00;

    while((SPI_RX_data[0] & 0xF0) != 0x20)
    {
        RF_SPI_Write(STX, 0x00, 0x00, 1);                 //0x35. Enable Tx.
        SPI_RX_data[0] = SPI_SpiUartReadRxData();
    }

}
```

```
#define IOCFG3_REG                  0x00
#define IOCFG3_VAL                  0xB0        //GPIO3 disabled. High Z.

#define IOCFG2_REG                  0x01
#define IOCFG2_VAL                  0x06        //GPIO2 asserted when sync has been sent. De asserted end of packet.

#define IOCFG1_REG                  0x02
#define IOCFG1_VAL                  0xB0        //GPIO1 disabled. High Z. Used for SPI MISO.

#define IOCFG0_REG                  0x03
#define IOCFG0_VAL                  0x02        //TXFIFO_THR. Asserted when TX FIFO is filled above or equal to 127-
FIFO_CFG.FIFO_THR.
                                                //De asserted when TX FIFO is drained below FIFO_CFG.FIFO_THR.
#define SYNC3_REG                   0x04
#define SYNC3_VAL                   0x93
#define SYNC2_REG                   0x05
#define SYNC2_VAL                   0x0B
#define SYNC1_REG                   0x06
#define SYNC1_VAL                   0x51
#define SYNC0_REG                   0x07
#define SYNC0_VAL                   0xDE
#define SYNC_CFG1_REG               0x08
#define SYNC_CFG1_VAL               0x08
#define SYNC_CFG0_REG               0x09
#define SYNC_CFG0_VAL               0x17

#define DEVIATION_M_REG             0x0A
#define DEVIATION_M_VAL             0x47        //Freq deviation 3kHz. TXCO 38.4MHz.

#define MODCFG_DEV_E_REG            0x0B
#define MODCFG_DEV_E_VAL            0x0A        //2GFSK, normal mode. DEV_E = 2.

#define DCFILT_CFG_REG              0x0C
#define DCFILT_CFG_VAL              0x1C

#define PREAMBLE_CFG1_REG           0x0D
#define PREAMBLE_CFG1_VAL           0x14        //Preamble 3 bytes. Pattern 0xAA.
```

```
#define PREAMBLE_CFG0_REG           0x0E
#define PREAMBLE_CFG0_VAL           0x2A

#define FREQ_IF_CFG_REG             0x0F
#define FREQ_IF_CFG_VAL             0x40

#define IQIC_REG                    0x10
#define IQIC_VAL                    0xC6

#define CHAN_BW_REG                 0x11
#define CHAN_BW_VAL                 0x0A        //Decimation factor 20, Rx filter BW 56.8kHz.

#define MDMCFG1_REG                 0x12
#define MDMCFG1_VAL                 0x46        //NRZ. Use FIFOs for data transfer.

#define MDMCFG0_REG                 0x13
#define MDMCFG0_VAL                 0x05        //Transparent mode disabled.

#define SYMBOL_RATE2_REG            0x14
#define SYMBOL_RATE2_VAL            0x74        //12ksps. SRATE_E = 7. TXCO 38.4MHz.

#define SYMBOL_RATE1_REG            0x15
#define SYMBOL_RATE1_VAL            0x7A        //12ksps. TXCO 38.4MHz.

#define SYMBOL_RATE0_REG            0x16
#define SYMBOL_RATE0_VAL            0xE1        //12ksps. TXCO 38.4MHz.

#define AGC_REF_REG                 0x17
#define AGC_REF_VAL                 0x20

#define AGC_CS_THR_REG              0x18
#define AGC_CS_THR_VAL              0x19

#define AGC_GAIN_ADJUST_REG         0x19
#define AGC_GAIN_ADJUST_VAL         0x00

#define AGC_CFG3_REG                0x1A
#define AGC_CFG3_VAL                0x91
```

```
#define AGC_CFG2_REG                0x1B
#define AGC_CFG2_VAL                0x20

#define AGC_CFG1_REG                0x1C
#define AGC_CFG1_VAL                0xA9

#define AGC_CFG0_REG                0x1D
#define AGC_CFG0_VAL                0xCF

#define FIFO_CFG_REG                0x1E
#define FIFO_CFG_VAL                0x00        //GPIO 0 is asserted when TX FIFO is filled equal or greater than
127-FIFO_CFG_VAL.
                                                //GPIO 0 is de asserted when TX FIFO is drained below FIFO_CFG_VAL.
#define DEV_ADDR_REG                0x1F
#define DEV_ADDR_VAL                0x00

#define SETTLING_CFG_REG            0x20
#define SETTLING_CFG_VAL            0x0B        //Auto calibration performed when going from IDLE to TX or IDLE to
FSTXON.

#define FS_CFG_REG                  0x21
#define FS_CFG_VAL                  0x1A         //164MHz to 192MHz. LO divider = 20.
//#define FS_CFG_VAL                  0x18         //205MHz to 240MHz. LO divider = 16.

#define WOR_CFG1_REG                0x22
#define WOR_CFG1_VAL                0x08

#define WOR_CFG0_REG                0x23
#define WOR_CFG0_VAL                0x21

#define WOR_EVENT0_MSB_REG          0x24
#define WOR_EVENT0_MSB_VAL          0x00

#define WOR_EVENT0_LSB_REG          0x25
#define WOR_EVENT0_LSB_VAL          0x00

#define PKT_CFG2_REG                0x26
#define PKT_CFG2_VAL                0x04        //Normal mode.
```

```
#define PKT_CFG1_REG                0x27
#define PKT_CFG1_VAL                0x05        //CRC calculation enabled. Data whitening disabled. No address
check.

#define PKT_CFG0_REG                0x28
#define PKT_CFG0_VARIABLE_VAL       0x20        //Variable packet length. Up to 255 bytes. Packet length is first
byte after the sync word.
//#define PKT_CFG0_INFINITE_VAL       0x40        //Infinite packet length.

#define RFEND_CFG1_REG              0x29
#define RFEND_CFG1_VAL              0x0F

#define RFEND_CFG0_REG              0x2A
#define RFEND_CFG0_VAL              0x00

#define PA_CFG2_REG                 0x2B        //RF power.
#define PA_CFG2_VAL                 0x3B        //-4dBm.

#define PA_CFG1_REG                 0x2C
#define PA_CFG1_VAL                 0x56        //PA ramp up.

#define PA_CFG0_REG                 0x2D
#define PA_CFG0_VAL                 0x7D        //Tx upsampler factor = 32.

#define PKT_LEN_REG                 0x2E
#define PKT_LEN_VAL                 0xFF        //Max number of data bytes that can be transmited.

#define IF_MIX_CFG_REG              0x00        //Extended register.
#define IF_MIX_CFG_VAL              0x00

#define FREQOFF_CFG_REG             0x01        //Extended register.
#define FREQOFF_CFG_VAL             0x22

#define TOC_CFG_REG                 0x02        //Extended register.
#define TOC_CFG_VAL                 0x0B

#define MARC_SPARE_REG              0x03        //Extended register.
#define MARC_SPARE_VAL              0x00
```

```
#define ECG_CFG_REG                 0x04        //Extended register.
#define ECG_CFG_VAL                 0x00

#define CFM_DATA_CFG_REG            0x05        //Extended register.
#define CFM_DATA_CFG_VAL            0x00

#define EXT_CTRL_REG                0x06        //Extended register.
#define EXT_CTRL_VAL                0x01

#define RCCAL_FINE_REG              0x07        //Extended register.
#define RCCAL_FINE_VAL              0x00

#define RCCAL_COURSE_REG            0x08        //Extended register.
#define RCCAL_COURSE_VAL            0x00

#define RCCAL_OFFSET_REG            0x09        //Extended register.
#define RCCAL_OFFSET_VAL            0x00

#define FREQOFF1_REG                0x0A        //Extended register.
#define FREQOFF1_VAL                0x00

#define FREQOFF0_REG                0x0B        //Extended register.
#define FREQOFF0_VAL                0x00

#define FREQ2_REG                   0x0C        //Extended register.
//#define FREQ2_VAL                 0x5F        //229MHz. TXCO 38.4MHz.
#define FREQ2_VAL                   0x58        //169MHz. TXCO 38.4MHz.

#define FREQ1_REG                   0x0D        //Extended register.
//#define FREQ1_VAL                 0x6A        //229MHz. TXCO 38.4MHz.
#define FREQ1_VAL                   0x05        //169MHz. TXCO 38.4MHz.

#define FREQ0_REG                   0x0E        //Extended register.
//#define FREQ0_VAL                 0xAA        //229MHz. TXCO 38.4MHz.
#define FREQ0_VAL                   0x55        //169MHz. TXCO 38.4MHz.

#define IF_ADC2_REG                 0x0F        //Extended register.
#define IF_ADC2_VAL                 0x02
```

```
#define IF_ADC1_REG                0x10        //Extended register.
#define IF_ADC1_VAL                0xA6

#define IF_ADC0_REG                0x11        //Extended register.
#define IF_ADC0_VAL                0x05

#define FS_DIG1_REG                0x12        //Extended register.
#define FS_DIG1_VAL                0x00

#define FS_DIG0_REG                0x13        //Extended register.
#define FS_DIG0_VAL                0x5F

#define FS_CAL3_REG                0x14        //Extended register.
#define FS_CAL3_VAL                0x00

#define FS_CAL2_REG                0x15        //Extended register.
#define FS_CAL2_VAL                0x20

#define FS_CAL1_REG                0x16        //Extended register.
#define FS_CAL1_VAL                0x00

#define FS_CAL0_REG                0x17        //Extended register.
#define FS_CAL0_VAL                0x0E

#define FS_CHP_REG                 0x18        //Extended register.
#define FS_CHP_VAL                 0x28
#define FS_CHP_INDEX               2

#define FS_DIVTWO_REG              0x19        //Extended register.
#define FS_DIVTWO_VAL              0x03

#define FS_DSM1_REG                0x1A        //Extended register.
#define FS_DSM1_VAL                0x00

#define FS_DSM0_REG                0x1B        //Extended register.
#define FS_DSM0_VAL                0x33

#define FS_DVC1_REG                0x1C        //Extended register.
#define FS_DVC1_VAL                0xFF
```

```
#define FS_DVC0_REG                 0x1D        //Extended register.
#define FS_DVC0_VAL                 0x17

#define FS_PFD_REG                  0x1F        //Extended register.
#define FS_PFD_VAL                  0x50

#define FS_PRE_REG                  0x20        //Extended register.
#define FS_PRE_VAL                  0x6E

#define FS_REG_DIV_CML_REG          0x21        //Extended register.
#define FS_REG_DIV_CML_VAL          0x14

#define FS_SPARE_REG                0x22        //Extended register.
#define FS_SPARE_VAL                0xAC

#define FS_VCO4_REG                 0x23        //Extended register.
#define FS_VCO4_VAL                 0x14
#define FS_VCO4_INDEX               1

#define FS_VCO3_REG                 0x24        //Extended register.
#define FS_VCO3_VAL                 0x00

#define FS_VCO2_REG                 0x25        //Extended register.
#define FS_VCO2_VAL                 0x00
#define FS_VCO2_INDEX               0

#define FS_VCO1_REG                 0x26        //Extended register.
#define FS_VCO1_VAL                 0x00

#define FS_VCO0_REG                 0x27        //Extended register.
#define FS_VCO0_VAL                 0x81

#define GBIAS6_REG                  0x28        //Extended register.
#define GBIAS6_VAL                  0x00

#define GBIAS5_REG                  0x29        //Extended register.
#define GBIAS5_VAL                  0x02
```

```
#define GBIAS4_REG                  0x2A        //Extended register.
#define GBIAS4_VAL                  0x00

#define GBIAS3_REG                  0x2B        //Extended register.
#define GBIAS3_VAL                  0x00

#define GBIAS2_REG                  0x2C        //Extended register.
#define GBIAS2_VAL                  0x10

#define GBIAS1_REG                  0x2D        //Extended register.
#define GBIAS1_VAL                  0x00

#define GBIAS0_REG                  0x2E        //Extended register.
#define GBIAS0_VAL                  0x00

#define IFAMP_REG                   0x2F        //Extended register.
#define IFAMP_VAL                   0x01

#define LNA_REG                     0x30        //Extended register.
#define LNA_VAL                     0x01

#define RXMIX_REG                   0x31        //Extended register.
#define RXMIX_VAL                   0x01

#define XOSC5_REG                   0x32        //Extended register.
#define XOSC5_VAL                   0x0E

#define XOSC4_REG                   0x33        //Extended register.
#define XOSC4_VAL                   0xA0

#define XOSC3_REG                   0x34        //Extended register.
#define XOSC3_VAL                   0xC7

#define XOSC2_REG                   0x35        //Extended register.
#define XOSC2_VAL                   0x05        //XOSC always ON.

#define XOSC1_REG                   0x36        //Extended register.
#define XOSC1_VAL                   0x07
```

```
#define ANALOG_SPARE_REG            0x38        //Extended register.
#define ANALOG_SPARE_VAL            0x00

#define PA_CFG3_REG                 0x39        //Extended register.
#define PA_CFG3_VAL                 0x00

#define BIST_REG                    0x68        //Extended register.
#define BIST_VAL                    0x00

#define DCFILTOFFSET_I1_REG         0x69        //Extended register.
#define DCFILTOFFSET_I1_VAL         0x00

#define DCFILTOFFSET_I0_REG         0x6A        //Extended register.
#define DCFILTOFFSET_I0_VAL         0x00

#define DCFILTOFFSET_Q1_REG         0x6B        //Extended register.
#define DCFILTOFFSET_Q1_VAL         0x00

#define DCFILTOFFSET_Q0_REG         0x6C        //Extended register.
#define DCFILTOFFSET_Q0_VAL         0x00

#define IQIE_I1_REG                 0x6D        //Extended register.
#define IQIE_I1_VAL                 0x00

#define IQIE_I0_REG                 0x6E        //Extended register.
#define IQIE_I0_VAL                 0x00

#define IQIE_Q1_REG                 0x6F        //Extended register.
#define IQIE_Q1_VAL                 0x00

#define IQIE_Q0_REG                 0x70        //Extended register.
#define IQIE_Q0_VAL                 0x00

#define MARCSTATE_REG               0x73        //Extended register.

#define AGC_GAIN2_REG               0x7A        //Extended register.
#define AGC_GAIN2_VAL               0xD1
```

```
#define AGC_GAIN1_REG               0x7B        //Extended register.
#define AGC_GAIN1_VAL               0x00

#define AGC_GAIN0_REG               0x7C        //Extended register.
#define AGC_GAIN0_VAL               0x3F

#define CFM_TX_DATA_IN_REG          0x7E        //Extended register.
#define CFM_TX_DATA_IN_VAL          0x00

#define RNDGEN_REG                  0x80        //Extended register.
#define RNDGEN_VAL                  0x7F        //Random number generator disabled.

#define FSCAL_CTRL_REG              0x8D        //Extended register.
#define FSCAL_CTRL_VAL              0x01

#define SERIAL_STATUS_REG           0x91        //Extended register.
#define SERIAL_STATUS_VAL           0x00

#define PA_IFAMP_TEST_REG           0x96        //Extended register.
#define PA_IFAMP_TEST_VAL           0x00

#define FSRF_TEST_REG               0x97        //Extended register.
#define FSRF_TEST_VAL               0x00

#define PRE_TEST_REG                0x98        //Extended register.
#define PRE_TEST_VAL                0x00

#define PRE_OVR_REG                 0x99        //Extended register.
#define PRE_OVR_VAL                 0x00

#define ADC_TEST_REG                0x9A        //Extended register.
#define ADC_TEST_VAL                0x00

#define DVC_TEST_REG                0x9B        //Extended register.
#define DVC_TEST_VAL                0x0B
```

```
#define ATEST_REG                   0x9C        //Extended register.
#define ATEST_VAL                   0x40

#define ATEST_LVDS_REG              0x9D        //Extended register.
#define ATEST_LVDS_VAL              0x00

#define ATEST_MODE_REG              0x9E        //Extended register.
#define ATEST_MODE_VAL              0x00

#define XOSC_TEST_1_REG             0x9F        //Extended register.
#define XOSC_TEST_1_VAL             0x00

#define XOSC_TEST_0_REG             0xA0        //Extended register.
#define XOSC_TEST_0_VAL             0x00

#define RXFIRST_REG                 0xD2        //Extended register.
#define RXFIRST_VAL                 0x00

#define TXFIRST_REG                 0xD3        //Extended register.
#define TXFIRST_VAL                 0x00

#define RXLAST_REG                  0xD4        //Extended register.
#define RXLAST_VAL                  0x00

#define TXLAST_REG                  0xD5        //Extended register.
#define TXLAST_VAL                  0x00
```