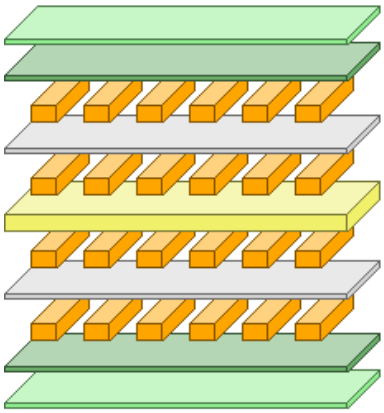
Stackup:

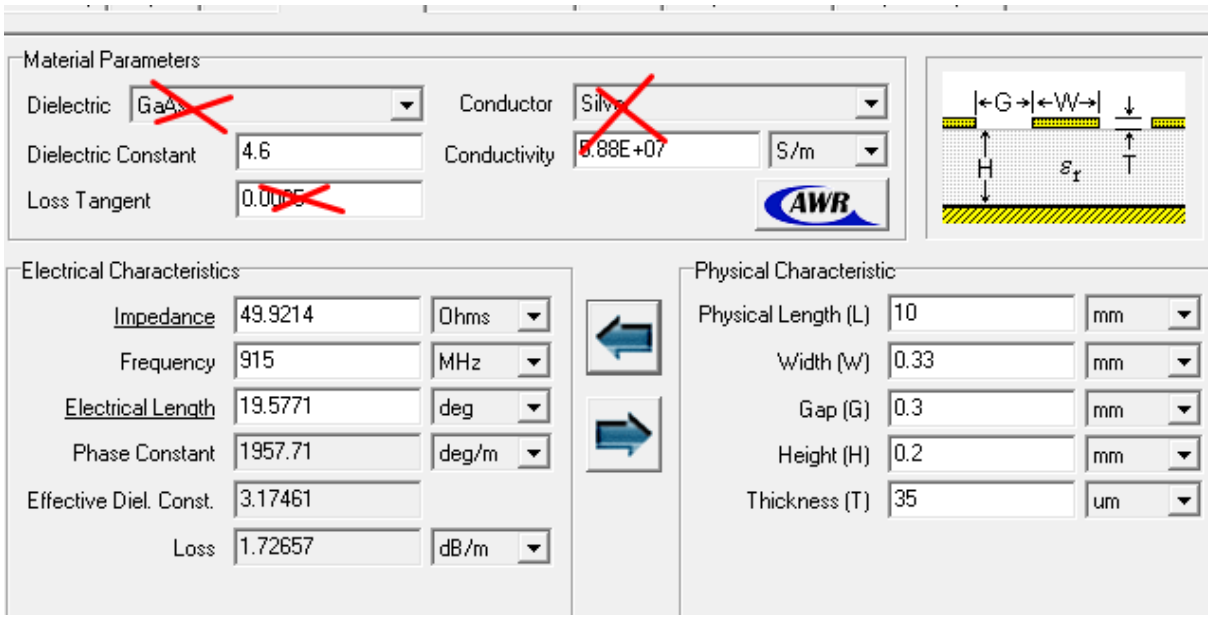


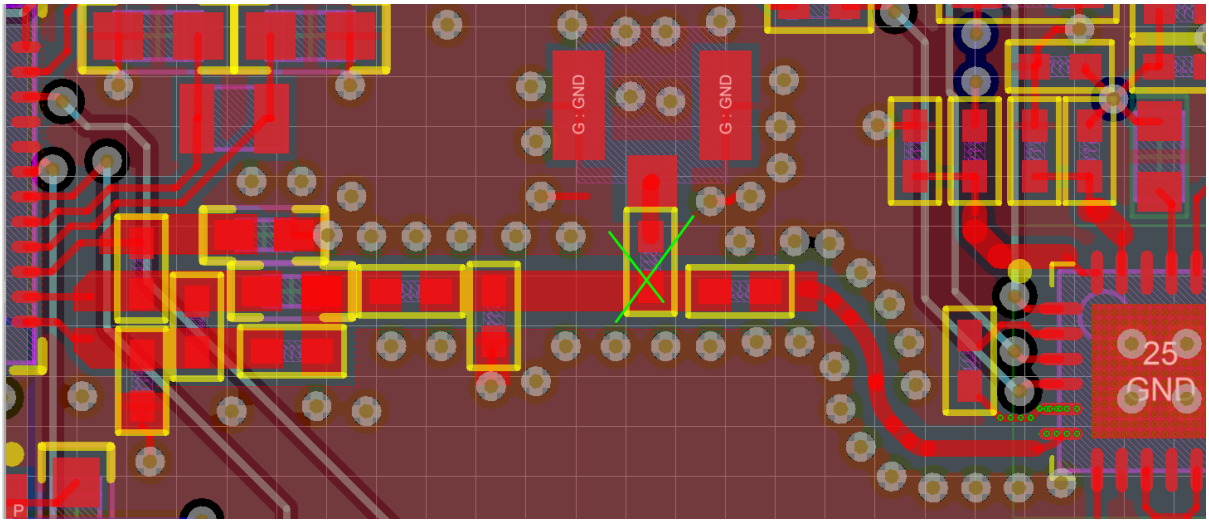
Layer Name	Type	Material	Thickness (mm)	Dielectric Material
Top Overlay	Overlay			
Top Solder	Solder Mask/Co...	Surface Material	0.0254	Solder Resist
Top Layer	Signal	Copper	0.035	
Dielectric 1	Dielectric	Prepreg	0.2	
Signal Layer 1	Signal	Copper	0.035	
Dielectric 3	Dielectric	Core	1	FR4
Signal Layer 2	Signal	Copper	0.035	
Dielectric 2	Dielectric	Prepreg	0.2	
Bottom Layer	Signal	Copper	0.035	
Bottom Solder	Solder Mask/Co...	Surface Material	0.0254	Solder Resist
Bottom Overlay	Overlay			

Total Thickness: 1.5908mm Add Layer Delete Layer Move Up Move Down

CPW calculation:

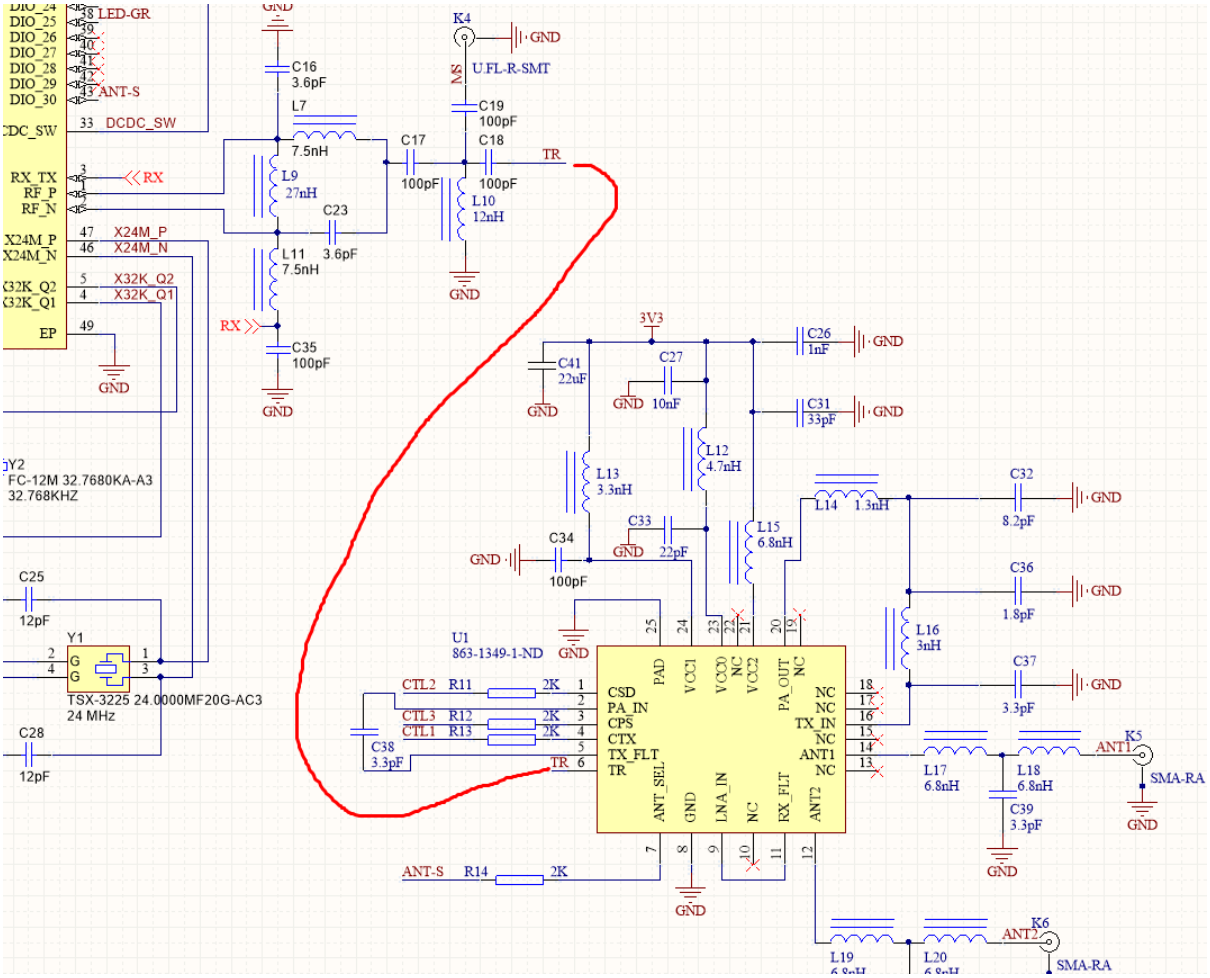
(TXLINE 2003)



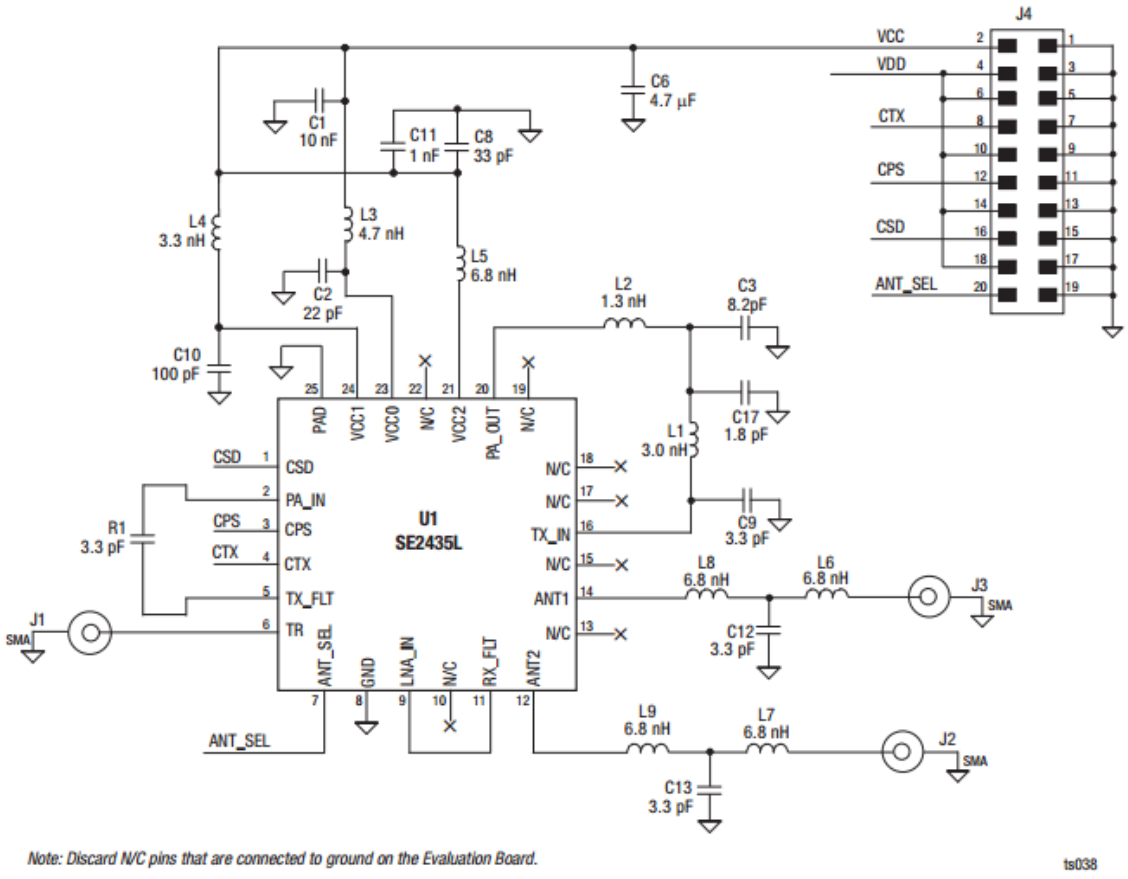


(solid ground plane on second layer; “light blue line is layer 3)

The 100 pF blocking cap is NC in the board design.



Skyworks reference schematic:



Note: Discard N/C pins that are connected to ground on the Evaluation Board.

ts038

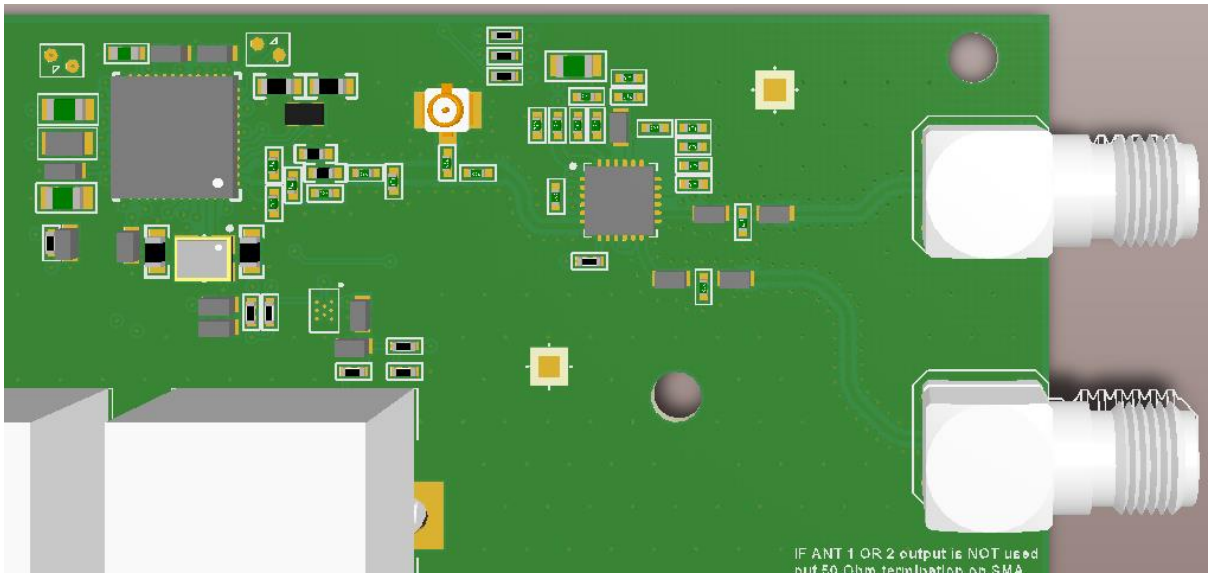
Figure 10. Evaluation Board Schematic for 915 MHz Application and FCC Conducted Harmonics Rejection Compliant

I verified the PA settings (CTX; CPS; CSD; ANT_SEL) levels before transmitting with a multimeter.

Table 6. SE2435L Electrical Specifications: Mode Control Logic (T_A = +25)

Mode	CPS	CSD	CTX	ANT_SEL
Sleep (all off)	0	0	0	X
Receive or transmit bypass	0	1	0	X
Receive LNA mode	1	1	0	X
Transmit	X	1	1	X
ANT1 port enabled	X	X	X	0
ANT2 port enabled	X	X	X	1

Note 1: "1" = 1.6 to Vcc, "0" = 0 to 0.3 V, "X" = don't care.


IF ANT 1 OR 2 output is NOT used