

Revision History

Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A

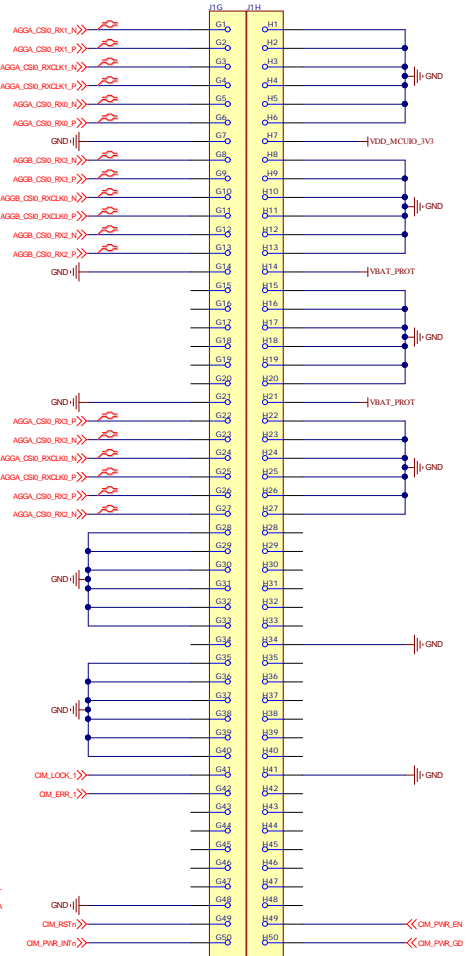
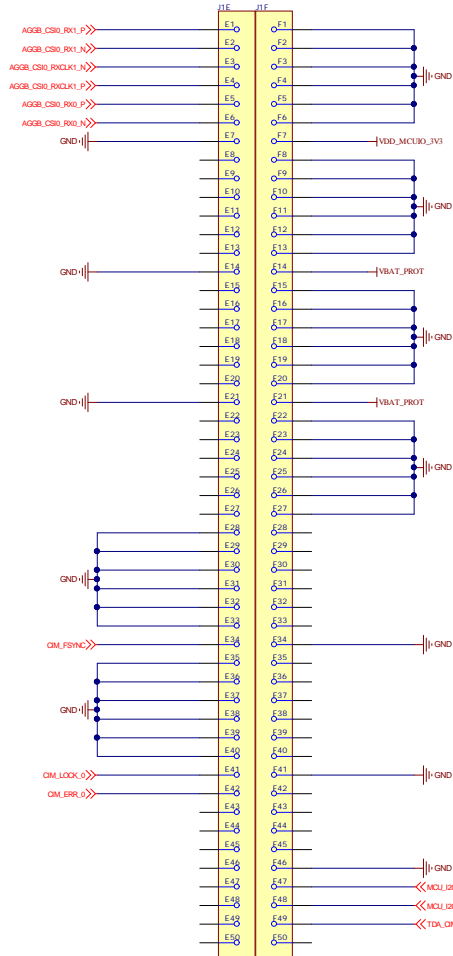
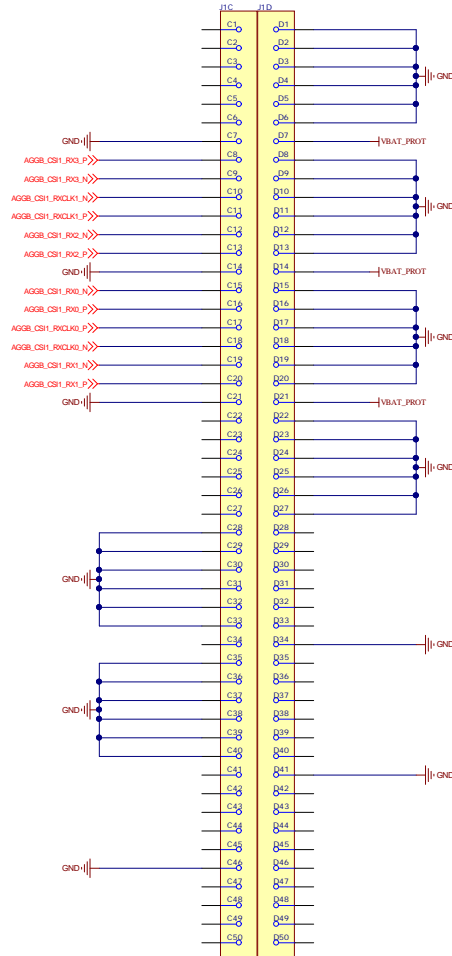
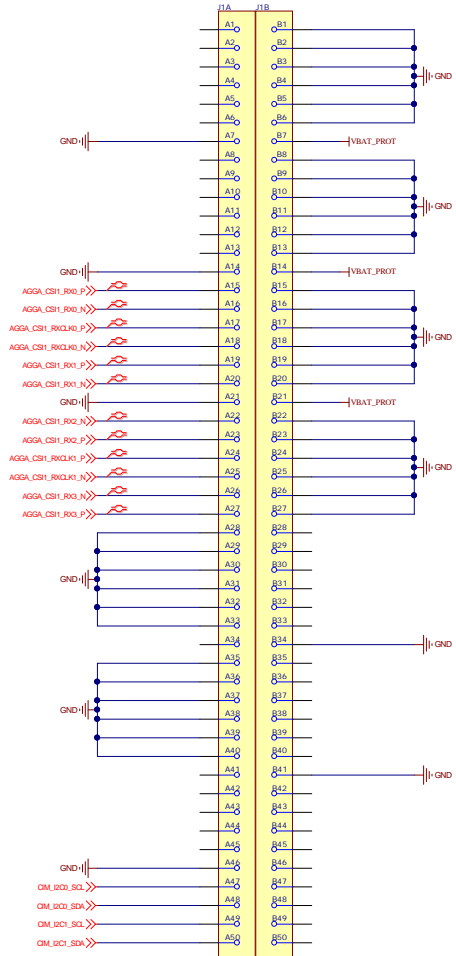
Place Block Diagram here (if appropriate) or delete this text box.
 If using a block diagram from another tool, save the picture as a .bmp
 file.
 Then, use menu Place|Drawing Tools|Graphic to insert the
 .png/.svg/.bmp file on the schematic.

Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 7/11/2019
TID #: N/A	Project Title: Qualcomm 9702 Daughter Card	
Number: Qualcomm 9702 Daughter Card	Sheet Title:	
SVN Rev.: Not in version control	Assembly Variant: 001	Sheet: 1 of 10
Drawn By:	File: CoverSheet_SchDoc	Size: B
Engineer: Mustafa Shuva	Contact: http://www.ti.com/support	

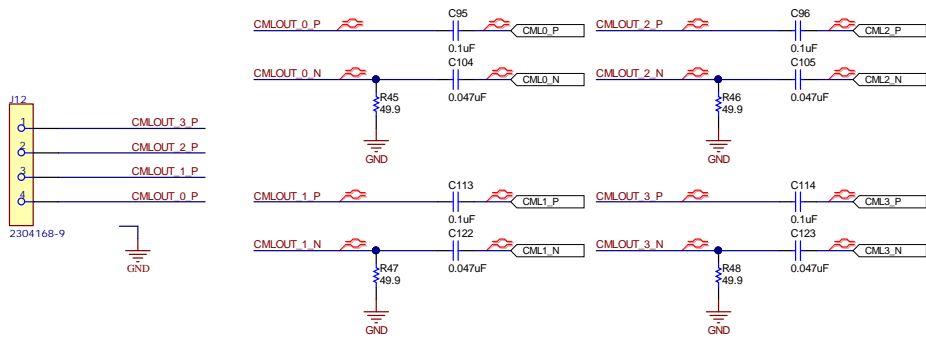
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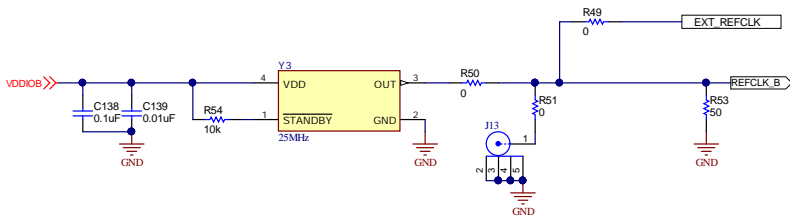
NVIDIA Interface Connector



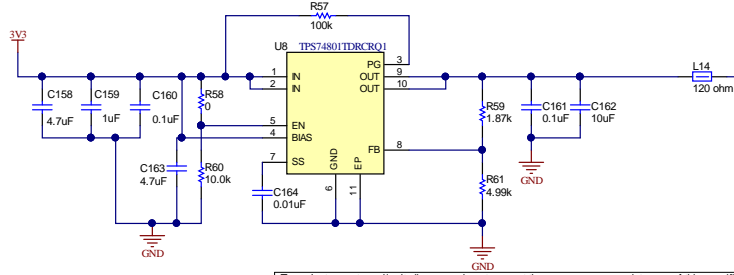
CMLOUT Connection



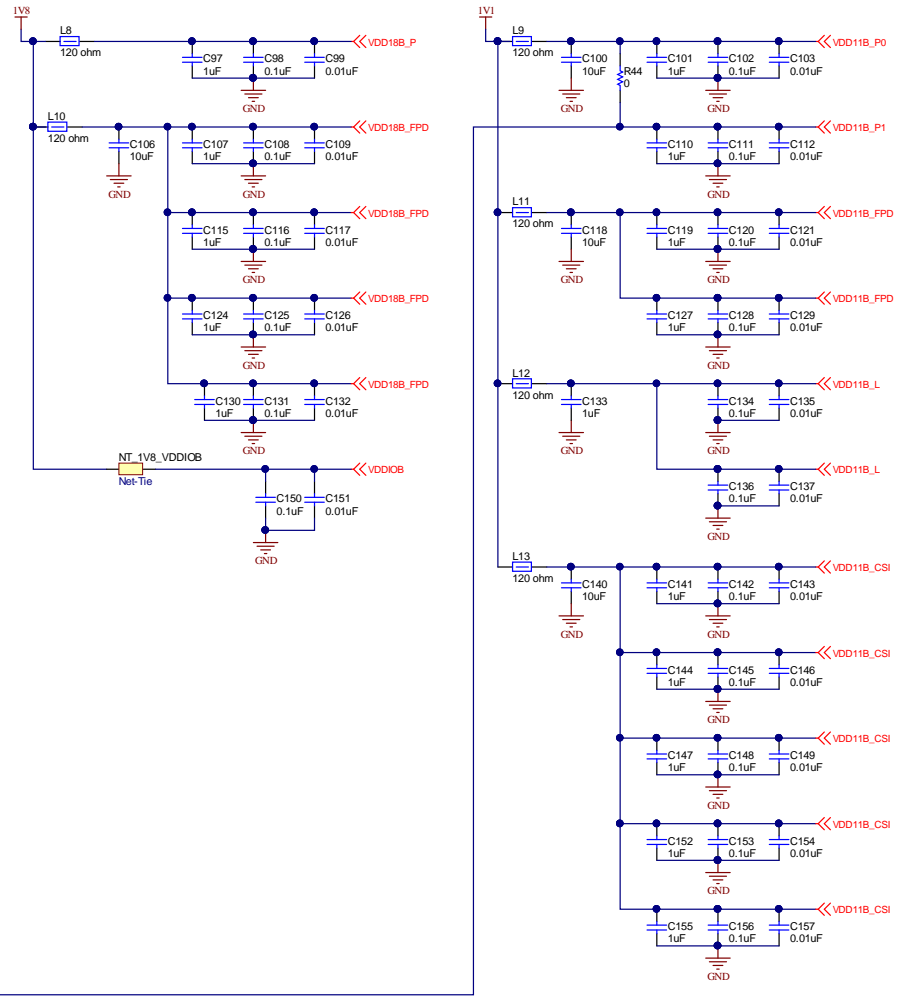
External Clock



1V1@1.5A POWER SUPPLY



Power Filtering

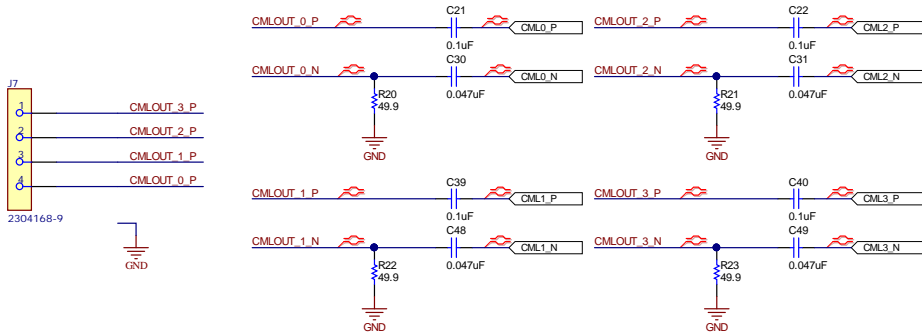


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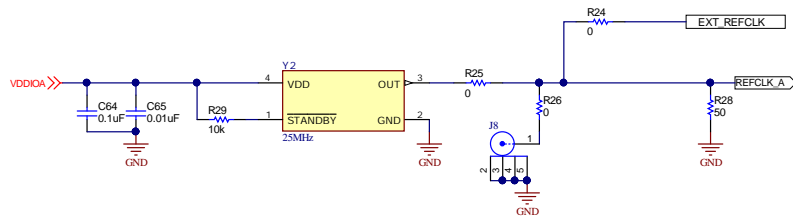
Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 7/23/2020
TID #: N/A	Project Title: Qualcomm 9702 Daughter Card	
Number: Qualcomm 9702 Daughter Card	Sheet Title:	
SVN Rev.: Not in version control	Assembly Variant: 001	Sheet: 2 of 3
Drawn By:	File: VNE-9702 DaughterCard_9702B_Filtering_CML_ISR68B.Doc	http://www.ti.com
Engineer: Mostafa Shuva	Contact: http://www.ti.com/support	© Texas Instruments 2018



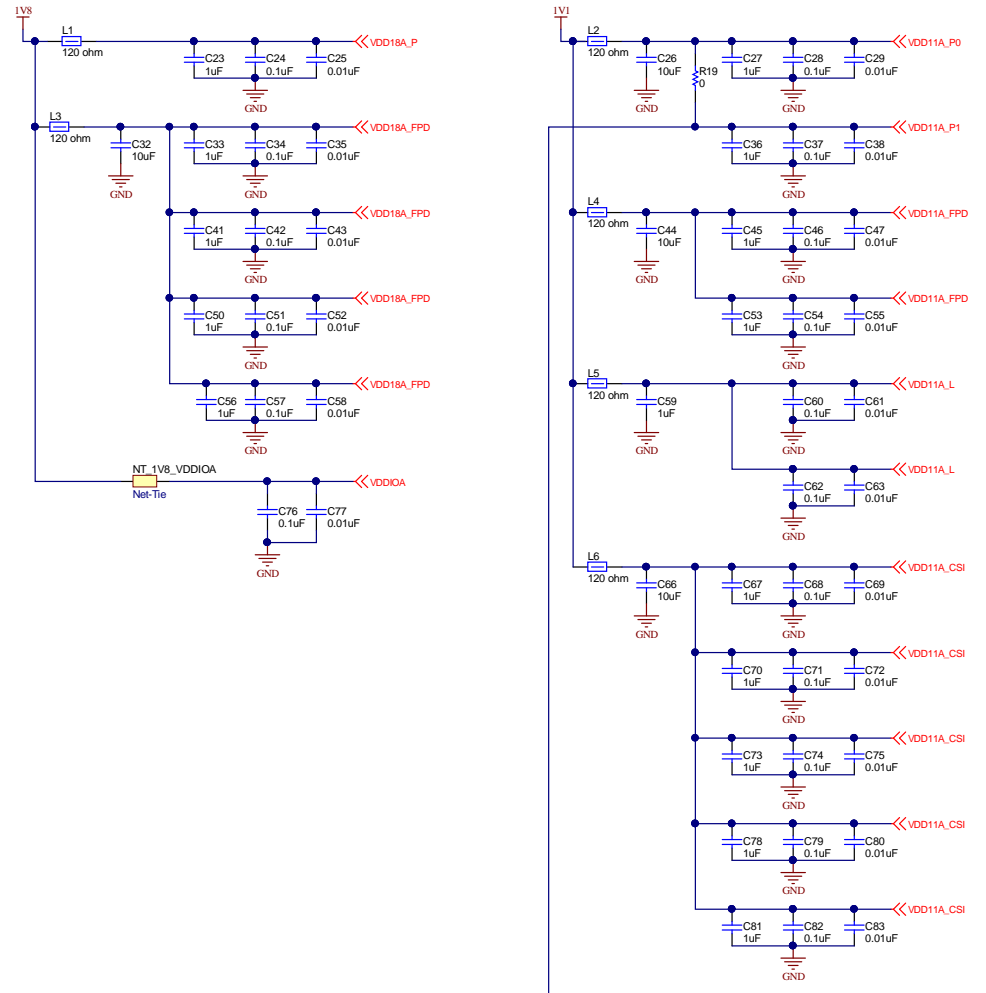
CMLOUT Connection



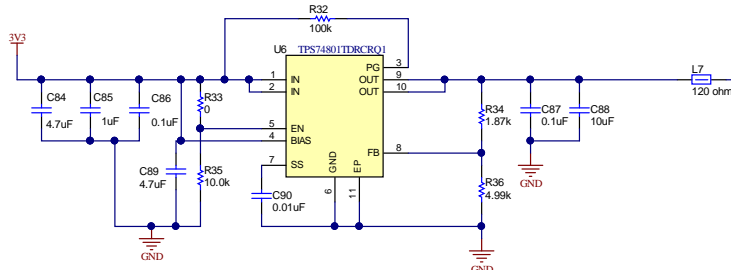
External Clock



Power Filtering



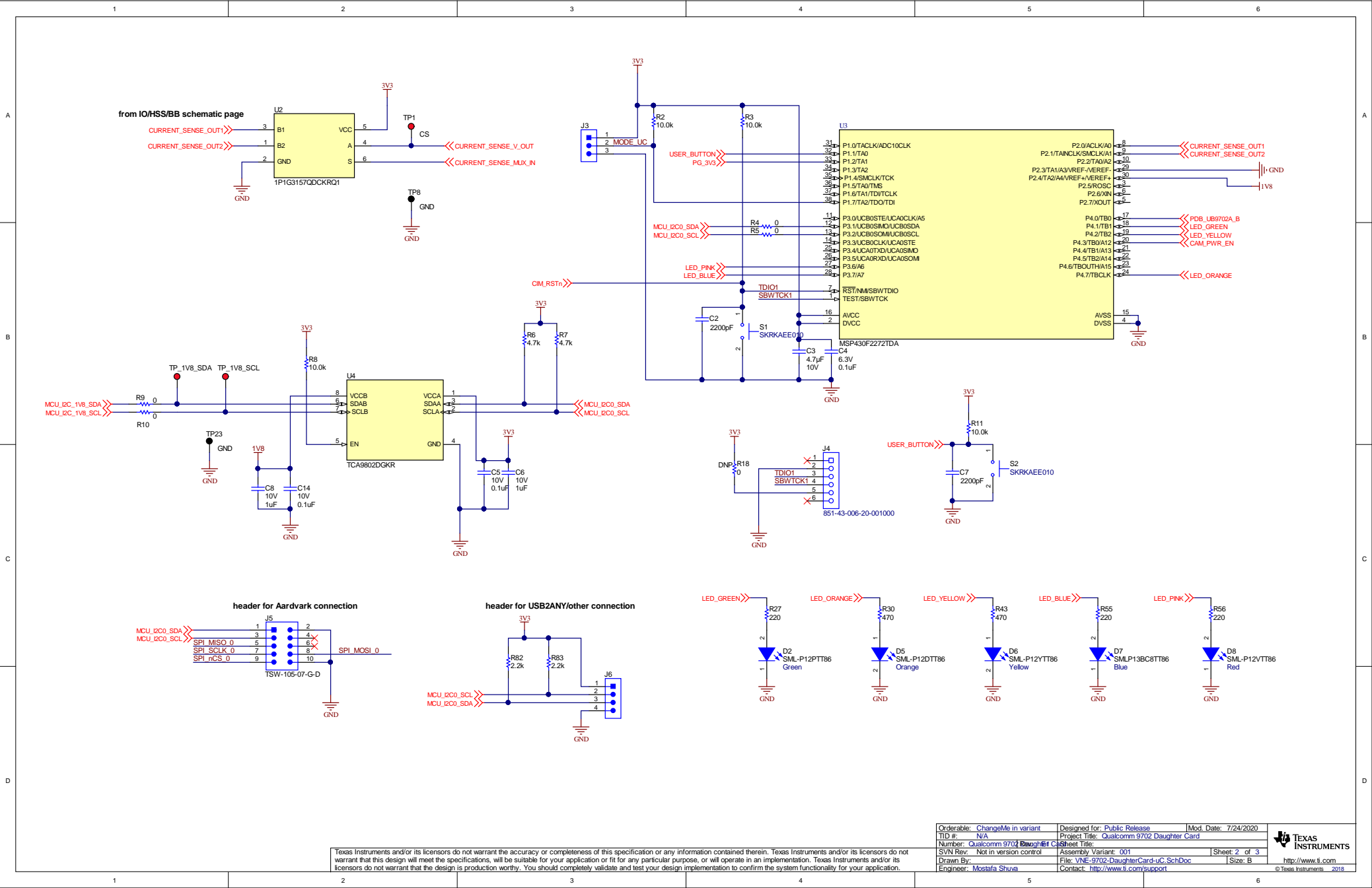
1V1@1.5A POWER SUPPLY



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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 7/23/2020
TID #: N/A	Project Title: Qualcomm 9702 Daughter Card	
Number: Qualcomm 9702 Daughter Card	Sheet Title:	
SVN Rev.: Not in version control	Assembly Variant: 001	Sheet: 2 of 3
Drawn By:	File: VNE-9702 DaughterCard_9702A_Filtering_CML_IS0648.DOC	http://www.ti.com
Engineer: Mustafa Shuja	Contact: http://www.ti.com/support	© Texas Instruments 2018



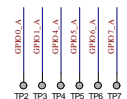
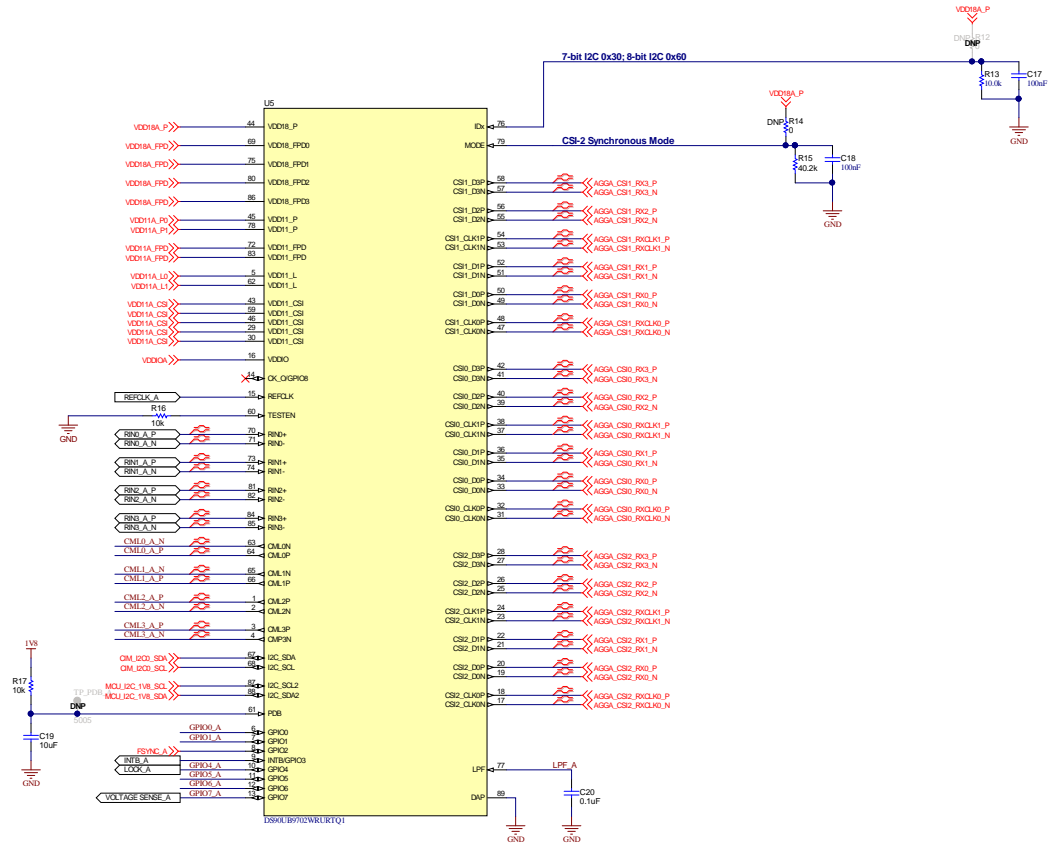
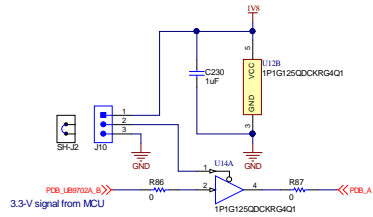
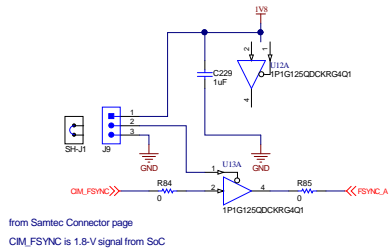


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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 7/24/2020
TID #: N/A	Project Title: Qualcomm 9702 Daughter Card	
Number: Qualcomm 9702 Daughter Card	Sheet Title:	
SVN Rev.: Not in version control	Assembly Variant: 001	Sheet 2 of 3
Drawn By:	File: VNE-9702-DaughterCard-uC_SchDoc	Size: B
Engineer: Mustafa Shuja	Contact: http://www.ti.com/support	

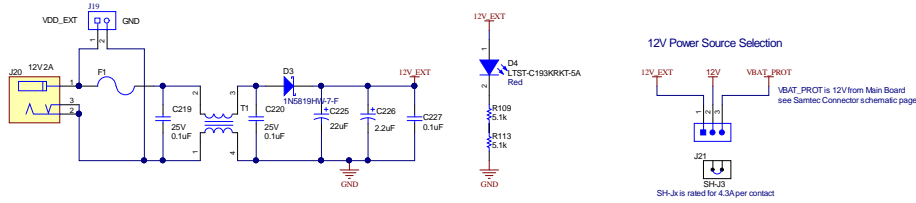


9702_A

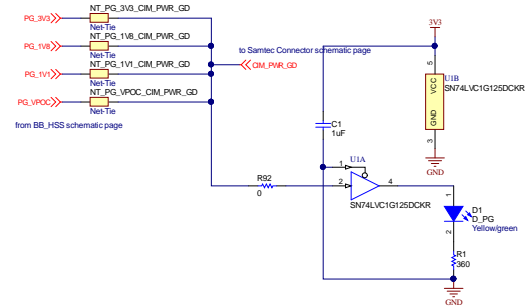


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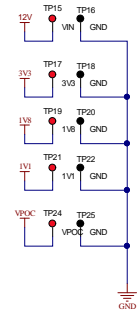
External Power Supply Input



PG & STATUS LEDs

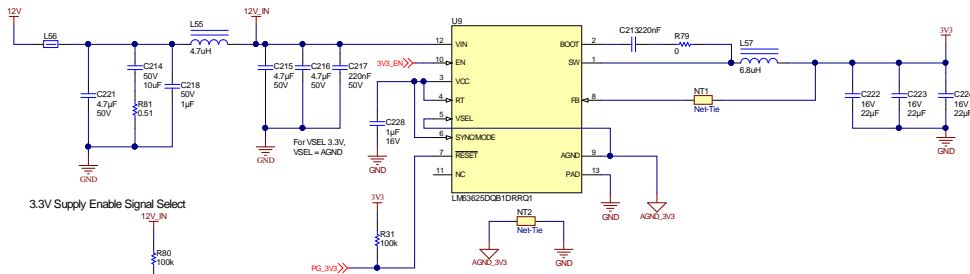


POWER SUPPLY TEST POINTS

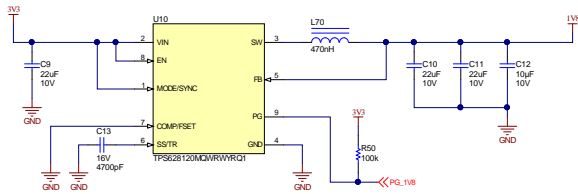


VSYS - 3.3 V @ 2.5A POWER SUPPLY

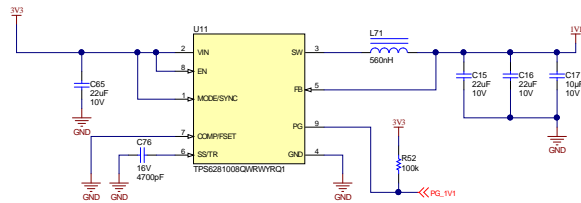
EMI Filter for LM63625-Q1 @ 400 kHz



1V8 @ 2A POWER SUPPLY

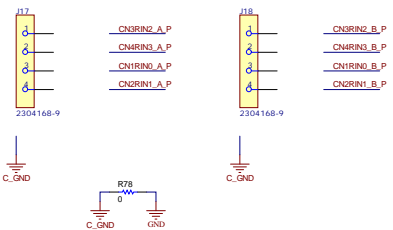
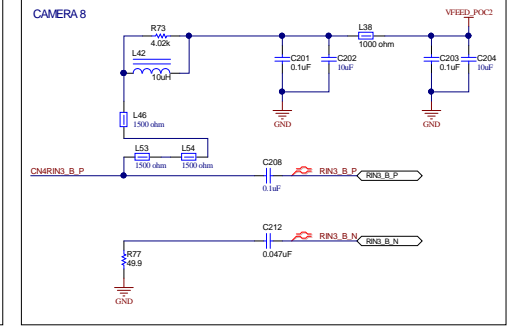
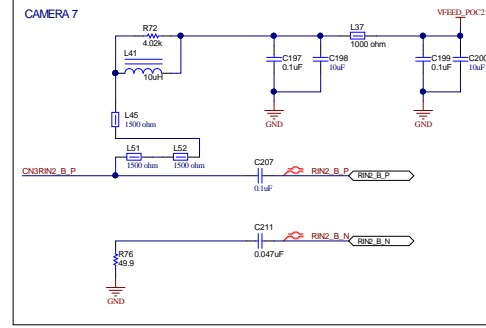
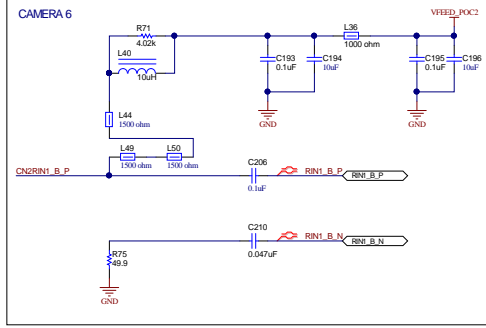
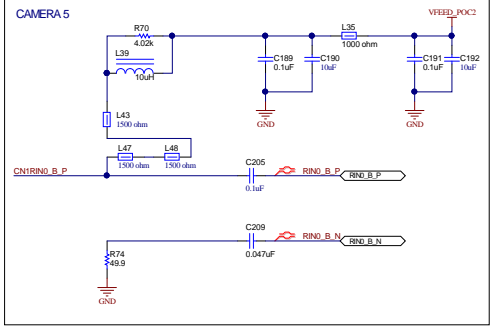
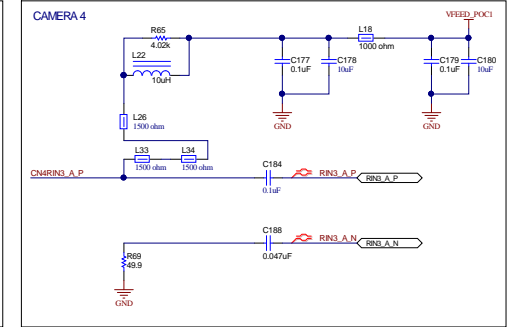
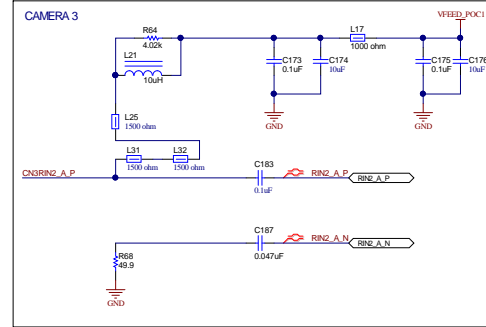
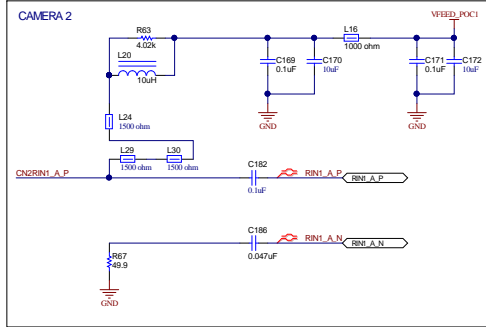
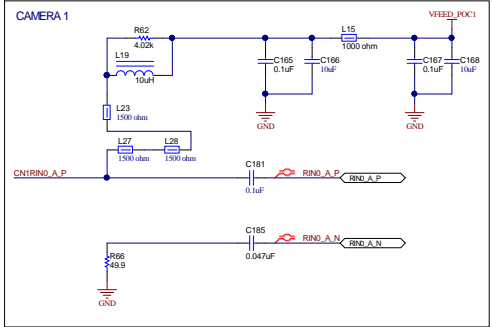


1V1 @ 4A POWER SUPPLY



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Power over Coax



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DNP
FD1

DNP
FD2

DNP
FD3

PCB Number: Qualcomm 9702 Daughter Card
PCB Rev: Rev1

PCB
LOGO
Texas Instruments



PCB
LOGO
FCC disclaimer

PCB
LOGO
WEEE logo

Variant/Label Table

Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1
PCB Label
THF-14-423-10
Size: 0.65" x 0.20"

ZZ1
Label Assembly Note
This Assembly Note is for PCB labels only

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

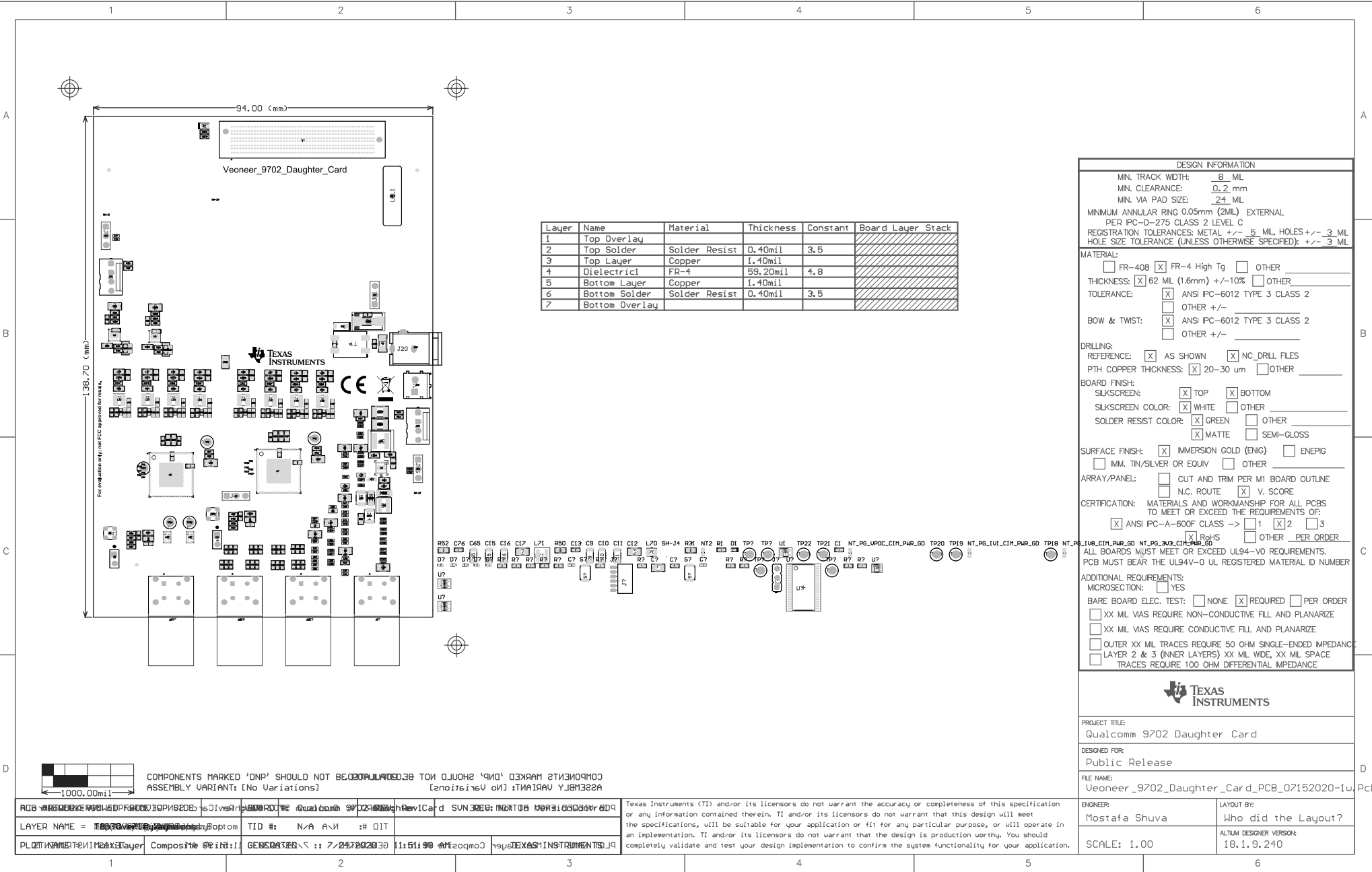
ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Orderable: ChangeMe in variant	Designed for: Public Release	Mod. Date: 9/25/2019
TID #: N/A	Project Title: Qualcomm 9702 Daughter Card	
Number: Qualcomm 9702 Daughter Card	Sheet Title:	Sheet: 8 of 8
SVN Rev.: Not in version control	Assembly Variant: 001	Size: B
Drawn By:	File: Hardware_SchDoc	http://www.ti.com
Engineer: Mustafa Shuva	Contact: http://www.ti.com/support	© Texas Instruments 2018



Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
 Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
 Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
 Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4	59.20mil	4.8	
5	Bottom Layer	Copper	1.40mil		
6	Bottom Solder	Solder Resist	0.40mil	3.5	
7	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8_MIL
 MIN. CLEARANCE: 0.2 mm
 MIN. VIA PAD SIZE: 24_MIL
 MINIMUM ANNUAL RING 0.05mm (2MIL) EXTERNAL
 PER IPC-D-275 CLASS 2 LEVEL C
 REGISTRATION TOLERANCES: METAL +/- 5_MIL, HOLES +/- 3_MIL
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3_MIL

MATERIAL:
 FR-408 FR-4 High Tg OTHER
 THICKNESS: 62 MIL (1.6mm) +/-10% OTHER
 TOLERANCE: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-
 BOW & TWIST: ANSI IPC-6012 TYPE 3 CLASS 2
 OTHER +/-

DRILLING:
 REFERENCE: AS SHOWN NC_DRILL FILES
 PTH COPPER THICKNESS: 20-30 um OTHER

BOARD FINISH:
 SILKSREEN: TOP BOTTOM
 SILKSREEN COLOR: WHITE OTHER
 SOLDER RESIST COLOR: GREEN OTHER
 MATTIE SEMI-GLOSS

SURFACE FINISH: IMMERSION GOLD (ENG) ENERP
 MM. TIN/SILVER OR EQUIV OTHER

ARRAY/PANEL: CUT AND TRM PER M1 BOARD OUTLINE
 N.C. ROUTE V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs
 TO MEET OR EXCEED THE REQUIREMENTS OF:
 ANSI IPC-A-600F CLASS -> 1 2 3
 RoHS OTHER PER ORDER

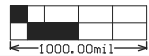
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
 MICROSECTION: YES
 BARE BOARD ELEC. TEST: NONE REQUIRED PER ORDER
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: Qualcomm 9702 Daughter Card
 DESIGNED FOR: Public Release
 FILE NAME: Veoneer_9702_Daughter_Card_PCB_07152020-1u

ENGINEER: Mostafa Shuva
 LAYOUT BY: Who did the Layout?
 SCALE: 1.00
 ALTUM DESIGNER VERSION: 18.1.9.240



COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED OR PRODUCED.
 ASSEMBLY VARIANT: [No Variations]

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