捷騰光電 solteamopto

JSA-1502

Color Light Sensor

Data Sheet

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Contents

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Color Light Sensor

JSA-1502

1. Description

JSA-1502 is a color-based light to digital converter which combines photodiodes, current amplifiers, analog circuit and digital signal processor. JSA-1502 provides red, green, blue, white and infrared light sensing. Each channel is parallel output at the same time, so it has excellent performance of illuminance & correlated color temperature under different light conditions such as white LED, CWF, TL84, D65, illuminant A and horizon. It can work from dark to direct sunlight, the selectable detect range is about 70dB. JSA-1502 has programmable interrupt function with high / low threshold.

2. Features

- I2C interface (Fast Speed Mode at 400kHz/s)
- Supply voltage range from 2.4V to 3.6V
- Operating temperature from -40°C to +85°C
- Package level trimming.
- Power on reset & brown out reset.
- Waiting time function for reducing power consumption.
- R, G, B, W and IR five channel parallel output.
- Fluorescent light flicker immunity.
- Selectable analog gain.
- Selectable resolution (up to 16-bit).
- High sensitivity in low illumination.
- Wide detect range in high illumination.
- High accuracy of LUX & CCT.

3. Applications

- Handset device
  - ■ Mobile phone, tablet, color matcher
- Consumer device
  - ■ LCD TV, digital camera, toy
- Computing device
  - ■ Laptop, LCD monitor
- Smart lighting
  - ■ Ceiling light, panel light

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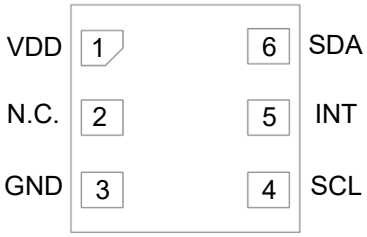
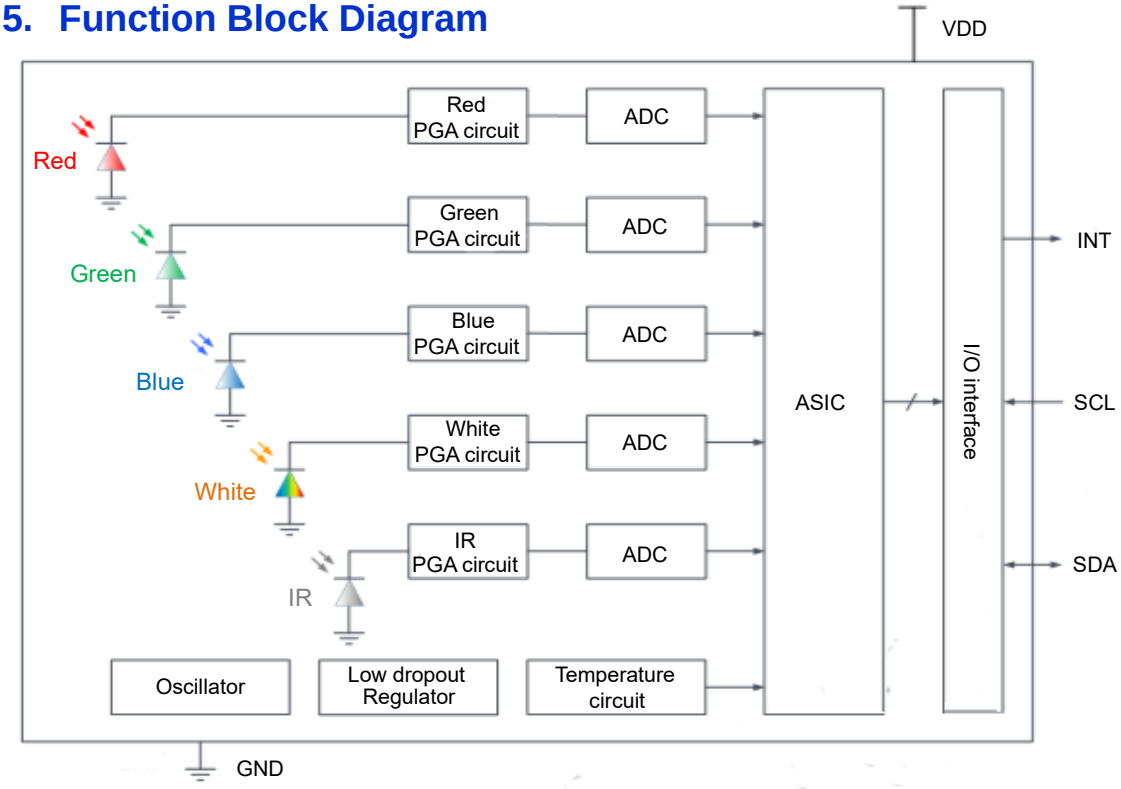
4. Pin Configuration



Pin Number	Pin Name	Description
1	VDD	Positive supply: 2.4V to 3.6V
2	N.C.	No connect
3	GND	Ground
4	SCL	I^2C serial clock signal
5	INT	Interrupt pin
6	SDA	I^2C serial data signal

5. Function Block Diagram



6. Ordering Information

Part Number	Slave Address	Package Size	Quantity
JSA-1502	0x38	2.0 x 2.0 x 0.6 (mm)	3000 per reel

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7. Absolute Maximum Ratings

Parameter	Rating	Unit
V_{DD} Supply Voltage	+4.5	V
I^2C Bus Pin Voltage (SCL, SDA)	-0.2 to +4.5	V
I^2C Bus Pin Current (SCL, SDA)	+10	mA
ESD Rating (HBM)	2	kV
Operating Temperature	-40 to +85	°C
Storage Temperature	-45 to +100	°C
CAUTION: Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.		

8. Electrical Characteristics (Ta = +25°C)

Parameter	Descriptions	Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage		2.4	3.0	3.6	V
V_{BUS}	I^2C bus supply Voltage	$V_{BUS} \leqq V_{DD}$	1.62	1.8	V_{DD}	V
V_{DD_slew}	V_{DD} power slew rate		0.5	--	--	V/ms
I_{PD1}	Shutdown current	V_{DD} = 3.3V, Ev=0, Sleep mode, *Note 1	--	1.5	--	uA
I_{PD2}	Shutdown current	V_{DD} = 3.3V, Ev=0, Sleep mode, I^2C inactive	--	2.5	--	uA
I_{DD}	Active current	V_{DD} = 3.3V, *Note 2	--	210	--	uA
T_{boot}	Device boot time	V_{DD} = 3.3V, *Note 3	--	20	--	ms

*Notes:

1. Brown out reset circuit disable.
2. The testing condition WTIME=6, INT_TIME=64T, CLSCONV=1.
3. The Device Boot Time (T_{boot}) is the delay time that the host can send the first I^2C command after the VDD ready.

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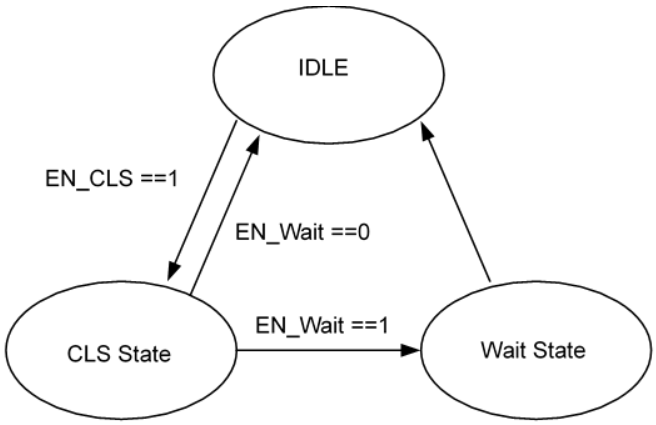
9. Optical Characteristics (V_{DD} = 3.3V, Ta = +25°C)

Descriptions		Condition	Min	Typ	Max	Unit
Full scale ADC counts value			--	--	65535	Count
Full scale ADC counts per step			--	--	1023	Count
Dark ADC Count		PGA_CLS=192; INT_TIME=64T CLSCONV=1	--	1	3	Count
CCT		Corrected color temperature accuracy	--	±5	--	%
ADC number of integration unit			1	--	16	Unit
ADC number of integration steps			1	--	64	Step
ADC integration time step size			--	2.06	--	ms
Sensing Gain Relative to x1 setting			--	4	--	
			--	8	--	
			--	32	--	
			--	96	--	
			--	192	--	
Wait time unit		W_{unit}	--	10	--	ms
Wait time number		W_{TIME}	1	--	256	W_{unit}
Sensitivity	RCH	PGA_CLA=96 INT_TIME=64T CLSCONV=1 White LED 4500K Ev = 500 Lux	4576	5200	5824	Count
	GCH		7463	8480	9498	
	BCH		2570	2920	3271	
	WCH		12743	14480	16218	

9.1 State Machine

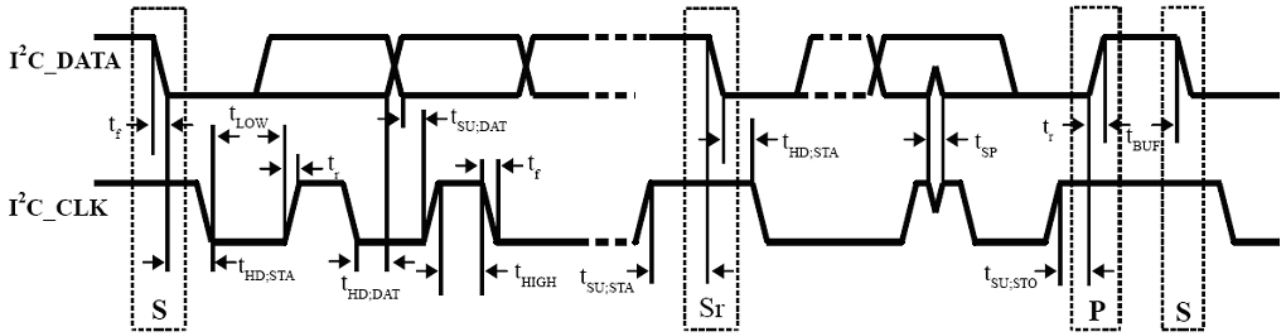
There are two operation mode CLS. The state machine is shown below:



10. I²C Electrical Specifications (V_{DD} = 3.3V, Ta = +25°C)

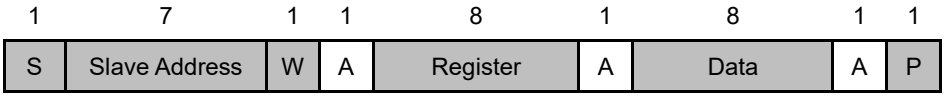
Parameter	Description	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	100	--	400	KHz
V_{IL}	I²C Bus Input Low Voltage	--	--	0.5	V
V_{IH}	I²C Bus Input High Voltage	1.4	--	--	V
$R_{pull-up}$	SDA and SCL system bus pull-up reistor	--	10	--	KΩ
t_{BUF}	Bus free time between a STOP and START condition	1.3	--	--	μs
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6	--	--	μs
t_{LOW}	LOW period of the SCL clock	1.3	--	--	μs
t_{HIGH}	HIGH period of the SCL clock	0.6	--	--	μs
$t_{SU;STA}$	Set-up time for a repeated START condition	0.6	--	--	μs
$t_{SU;STO}$	Set-up time for STOP condition	0.6	--	--	μs
t_r	Rise time of both SDA and SCL signCLS	20 x VDD/5.5	--	300	ns
t_f	Fall time of both SDA and SCL signCLS	20 x VDD/5.5	--	300	ns
$t_{HD;DAT}$	Data hold time	50	--	--	ns
$t_{SU;DAT}$	Data setup time	100	--	--	ns
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	0	--	50	ns

11. I²C Timing Diagram

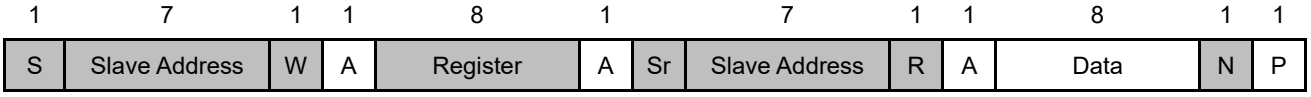


12. I²C Protocol

I²C Write



I²C Read



A	Acknowledge (0 for an ACK)	N	Non-Acknowledge(1 for an NACK)
S	Start condition	Sr	Repeated start condition
P	Stop condition		
W	Write (0 for writing)	R	Read (1 for read)
■	Master to Slave	□	Slave to Master

12.1 I²C Slave Address and R/W bit

This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). A '0' indicates a transmission (WRITE), a '1' indicates a request for data (READ).The slave address of this device is 0x38.

12.2 I²C Bus Clear

In the unlikely event where the clock (SCL) is stuck LOW, the preferential procedure is to reset the bus using the HW reset signal if your I²C devices have HW reset inputs. If theI²C devices do not have HW reset inputs, cycle power to the devices to activate the mandatory Internal Power-On Reset (POR) circuit. If the data line (SDA) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it sometime within those nine clocks.

12.3 I²C General Call Software Reset

Following a General Call, (0000 0000), sending 0000 0110 (06h) as the second byte causes software reset. This feature is optional and not all devices will respond to this command. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address. Precautions must be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

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13. Register Description

The JSA-1502 is operated over the I²C bus with registers that contain configuration, status, and result information. All registers are 8 bits long.

13.1 Overall

Address	Name	Type	Default value	Description
0x00	SYSM_CTRL	RW	0x00	CLS operation mode control, waiting mode control, SW reset
0x01	INT_CTRL	RW	0x03	Interrupt pin control, interrupt persist control
0x02	INT_FLAG	RW	0x80	Interrupt flag, error flag, power on reset (POR) flag
0x03	WAIT_TIME	RW	0x00	Waiting time setting
0x04	CLS_GAIN	RW	0x81	CLS analog gain setting
0x05	CLS_TIME	RW	0x03	CLS integrated time setting
0x0B	PERSISTENCE	RW	0x01	CLS persistence setting
0x0C	CLS_THRES_LL	RW	0x00	CLS lower interrupt threshold - LSB
0x0D	CLS_THRES_LH	RW	0x00	CLS lower interrupt threshold - MSB
0x0E	CLS_THRES_HL	RW	0xFF	CLS higher interrupt threshold - LSB
0x0F	CLS_THRES_HH	RW	0xFF	CLS higher interrupt threshold - MSB
0x16	INT_SOURCE	RW	0x08	CLS interrupt source
0x17	ERROR_FLAG	R	0x00	Error flag
0x1C	RCH_DATA_L	R	0x00	RCH output data - LSB
0x1D	RCH_DATA_H	R	0x00	RCH output data - MSB
0x1E	GCH_DATA_L	R	0x00	GCH output data - LSB
0x1F	GCH_DATA_H	R	0x00	GCH output data - MSB
0x20	BCH_DATA_L	R	0x00	BCH output data - LSB
0x21	BCH_DATA_H	R	0x00	BCH output data – MSB
0x22	WCH_DATA_L	R	0x00	WCH output data - LSB
0x23	WCH_DATA_H	R	0x00	WCH output data - MSB
0x24	IRCH_DATA_L	R	0x00	IRCH output data - LSB
0x25	IRCH_DATA_H	R	0x00	IRCH output data - MSB

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13.2 Register 0x00 – SYSM_CTRL

0x00	SYSM_CTRL, System Control (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	SWRST	EN_ WAIT	EN_ FRST	0	0	0	EN_IR	EN_ CLS

SWRST：Software reset. Reset all register to default value.

0: (Default)

1: Reset will be triggered.

EN_WAIT：Waiting time will be inserted between two measurements.

0: Disable waiting function. (Default)

1: Enable waiting function.

EN_FRST：

0: Enable (Brown out Reset circuit enable). (Default)

1: Disable (Brown out Reset circuit disable).

EN_IR：Enables IR function.

0: Disable IR function. (Default)

1: Enable IR function.

EN_CLS： Enables CLS function.

0: Disable CLS function. (Default)

1: Enable CLS function.

13.3 Register 0x01 – INT_CTRL

0x01	Interrupt Pin Control (Default = 0x03)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	CLS_ SYNC	0	0	1	EN_ CINT

CLS_SYNC： Measurement is pended when CLS interrupt is triggered. Until clear the interrupt then start the next measurement.

0: Disable pending CLS function. (Default)

1: Enable pending CLS function.

EN_CINT：The CLS interrupt (INT_CLS) flag can trigger the INT pin to low.

0: Disable INT_CLS effect INT pin.

1: Enable INT_CLS effect INT pin. (Default)

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13.4 Register 0x02 – INT_FLAG

0x02	INT_FLAG, System Control (Default = 0x80)							
BIT	7	6	5	4	3	2	1	0
R/W	INT_POR	DATA_FLAG	0	0	0	0	0	INT_CLS

INT_POR：Power-On-Reset Interrupt flag trigger the INT pin when the flag sets to one. Write zero to clear the flag.

0:

1: This bit will be set to one when it satisfies one of the following conditions:

- Power On
- VDD < 1.4V
- SWRST

DATA_FLAG： It shows if any data is invalid after completion of each conversion cycle. This bit is read-only.

0: Data valid.

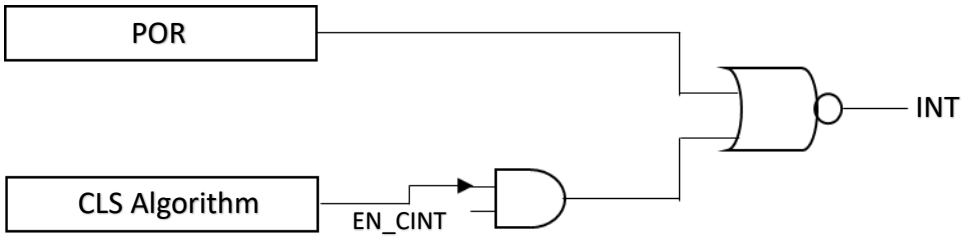
1: Data invalid.

INT_CLS：CLS Interrupt flag. Its correlation with CH0/1 data and CLS high/low threshold. Write zero to clear the flag.

0: CLS interrupt not triggered or be cleared.

1: CLS interrupt triggered.

Interrupt Behavior :



CLS Interrupt Algorithm

Correlative register:

The CLS Interrupt (**INT_CLS**, register 0x02, bit0).

The CLS Persistence (**PRS_CLS**, register 0x0B, bit0 to bit3).

The CLS Data (**W channel data**, register 0x22 to 0x23).

The CLS Low Threshold (**CLS_THRES_L**, register 0x0C to 0x0D).

The CLS High Threshold (**CLS_THRES_H**, register 0x0E to 0x0F).

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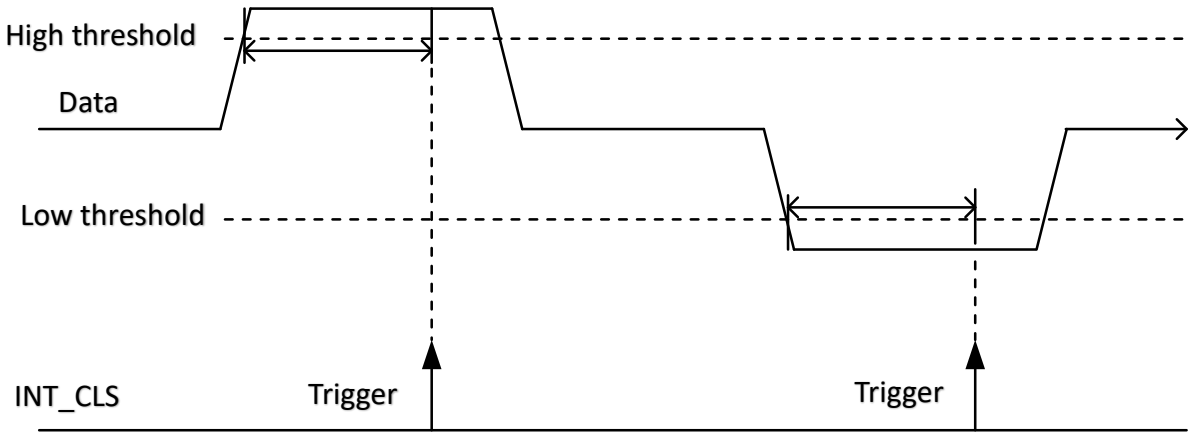
INT_CLS triggered condition:

1. Rule of active interrupt: **DATA**>**CLS_THRES_H** or **DATA**<**CLS_THRES_L.**
2. If the **DATA** meets the rule, the **interrupt** count increases one.
   If the **DATA** fails in the rule, the interrupt count will be clear.
3. When the **interrupt** count equal to **PRS_CLS setting**, **INT_CLS** will be triggered and reset the interrupt counter.
4. If **PRS_CLS** is set to zero, **threshold** will be ignored and **DATA** will meets the active interrupt rule forcibly.



13.5 Register 0x03 – WAIT_TIME

0x03	WAIT_TIME, waiting time (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	WTIME							

WTIME： This register controls the time unit of waiting state which is inserted between any two measurements. It is 10ms per time unit.

0x00: 1 time unit.

0x01: 2 time unit.

……

0x7f : 256 time unit.

13.6 Register 0x04 – CLS_GAIN

0x04	CLS_GAIN, CLS analog gain (Default = 0x81)							
BIT	7	6	5	4	3	2	1	0
R/W	DIOD_SEL	0	0	PGA_CLS				

DIOD_SEL：CLS sensor area select.

0: x1

1: x2 (Default)

PGA_CLS：CLS sensing gain.

0x01: x1 (Default)

0x02: x4

0x04: x8

0x08: x32

0x10: x96

0x20: x192

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13.7 Register 0x05 – CLS_TIME

0x05	CLS_TIME, CLS integrated time (Default = 0x03)							
BIT	7	6	5	4	3	2	1	0
R/W	INT_CYC				0	0	CYC_TIME	

INT_CYC：This register controls the integrated cycles.

0x0: 1 (Default)

0x1: 2

……

0xf : 16

CYC_TIME：This register controls the integrated cycle time .

0x0: 1T = 2.0667 ms.

0x1: 4T = 8.2668 ms.

0x2: 16T = 33.0672 ms.

0x3: 64T = 132.2688 ms. (Default)

The integrated time of CLS function (T_{CLS}) and the resolution of output data is decided by **INT_CYC** and **CYC_TIME**.

T_{CLS}= **CYC_TIME** x (**INT_CYC** + 1) (ms)

The maximum count of **output data** is minimum of [(1024 x [**CYC_TIME***(**INT_CYC** +1)] – 1) , 65535]

13.8 Register 0x0B – PERSISTENCE

0x0B	PERSISTENCE, CLS persistence setting (Default = 0x01)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	PRS_CLS			

PRS_CLS：This register sets the numbers of similar consecutive CLS interrupt events before the interrupt pin is triggered.

0x0: Every CLS conversion is done.

0x1: 1 consecutive CLS interrupt events is asserted. (Default)

……

0xf : 15 consecutive CLS interrupt events are asserted.

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13.9 Register 0x0C to 0x0D – CLS_THRES_L

0x0C 0x0D	CLS_THRES_L, CLS low interrupt threshold (Default = 0x0000)							
BIT	7	6	5	4	3	2	1	0
R/W	CLS_THRE_LL							
R/W	CLS_THRE_LH							

This register sets the lower threshold value of CLS interrupt. The interrupt algorithm the selected CLS data and CLS threshold value.

CLS_THRE_LL：CLS lower interrupt threshold value, LSB. (Reg. 0x0C)

CLS_THRE_LH：CLS lower interrupt threshold value, MSB. (Reg. 0x0D)

13.10 Register 0x0E to 0x0F – CLS_THRES_H

0x0E 0x0F	CLS_THRES_H, CLS high interrupt threshold (Default = 0xFFFF)							
BIT	7	6	5	4	3	2	1	0
R/W	CLS_THRE_HL							
R/W	CLS_THRE_HH							

This register sets the lower threshold value of CLS interrupt. The interrupt algorithm the selected CLS data and CLS threshold value.

CLS_THRE_HL：CLS high interrupt threshold value, LSB. (Reg. 0x0E)

CLS_THRE_HH：CLS high interrupt threshold value, MSB. (Reg. 0x0F)

13.11 Register 0x16 – INT_SOURCE

0x16	INT_SOURCE, CLS interrupt source (Default = 0x08)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	INT_SRC				

INT_SRC：This register sets to select the CLS data for the CLS Interrupt algorithm

0x01: Select RCH_DATA.

0x02: Select GCH_DATA.

0x04: Select BCH_DATA.

0x08: Select WCH_DATA.

0x10: Select IRCH_DATA.

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13.12 Register 0x17 – ERROR_FLAG

0x17	ERROR_FLAG, Error flag status							
BIT	7	6	5	4	3	2	1	0
R	0	0	0	ERR_IRCH	ERR_WCH	ERR_BCH	ERR_GCH	ERR_RCH

This register indicates the CLS data status. If the CLS data is outside of measurable range, the corresponding error flag (ERR_RCH, ERR_GCH, ERR_BCH, ERR_WCH, and ERR_IRCH) will set to one. That also means the data is invalid.

13.13 Register 0x1C to 0x1D – RCH_Data

0x1C 0x1D	RCH_DATA, R channel output data.							
BIT	7	6	5	4	3	2	1	0
R	RCH_DATA_L							
R	RCH_DATA_H							

The R channel conversion result is written into RCH_DATA when CLS conversion is done.

For ensuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

13.14 Register 0x1E to 0x1F – GCH_Data

0x1E 0x1F	GCH_DATA, G channel output data.							
BIT	7	6	5	4	3	2	1	0
R	GCH _DATA_L							
R	GCH_DATA_H							

The G channel conversion result is written into GCH_DATA when CLS conversion is done.

For ensuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

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13.15 Register 0x20 to 0x21 – BCH_Data

0x20 0x21	BCH_DATA, B channel output data.							
BIT	7	6	5	4	3	2	1	0
R	BCH _DATA_L							
R	BCH_DATA_H							

The B channel conversion result is written into BCH_DATA when CLS conversion is done.

For ensuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

13.16 Register 0x22 to 0x23 – WCH_Data

0x22 0x23	WCH_DATA, W channel output data.							
BIT	7	6	5	4	3	2	1	0
R	WCH _DATA_L							
R	WCH_DATA_H							

The W channel conversion result is written into WCH_DATA when CLS conversion is done.

For ensuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

13.17 Register 0x24 to 0x25 – IRCH_Data

0x24 0x25	IRCH_DATA, IR channel output data.							
BIT	7	6	5	4	3	2	1	0
R	IRCH _DATA_L							
R	IRCH_DATA_H							

The IR channel conversion result is written into IRCH_DATA when CLS conversion is done.

For ensuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has been accessed until the high byte data has be read.

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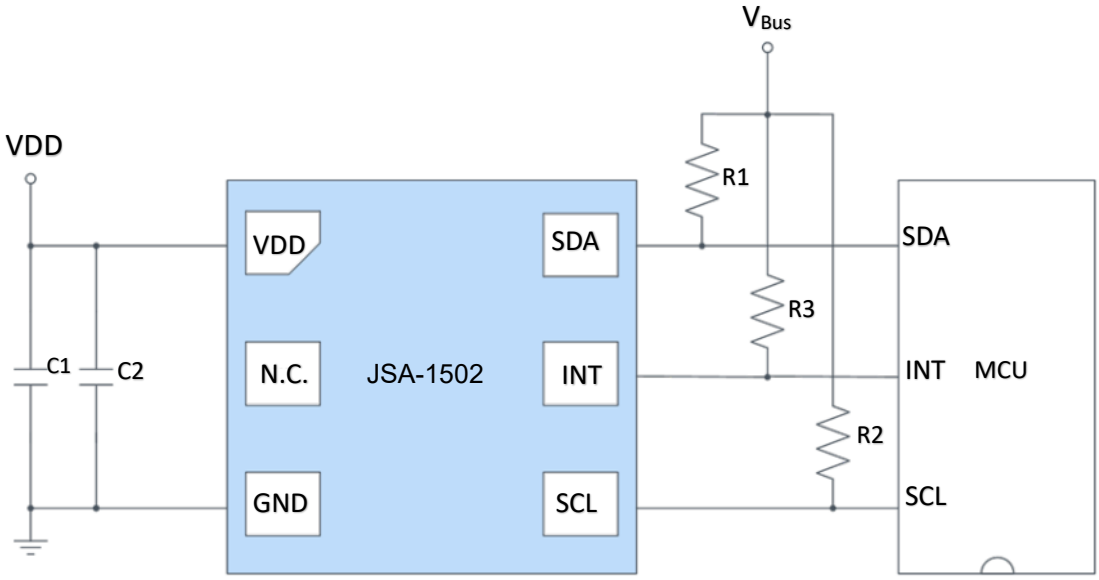
14. Application Circuit



The capacitors (C1, C2) are required for power supply. The capacitors should be placed as close as possible to the device. The high frequency AC noises can be shunted to the ground by the capacitors. The transient current caused by digital circuit switching also can be handled by the capacitors. A typical value 0.1 / 1 μF can be used.

The pull-up resistors (R1, R2) are required for I^2C communication. At fast speed mode (400kHz/s) and V_{BUS} = 3V, 1.5kΩ resistors can be used. The pull-up resistor (R3) is also required for the interrupt, a typical value between 10 kΩ and 100 kΩ can be used.

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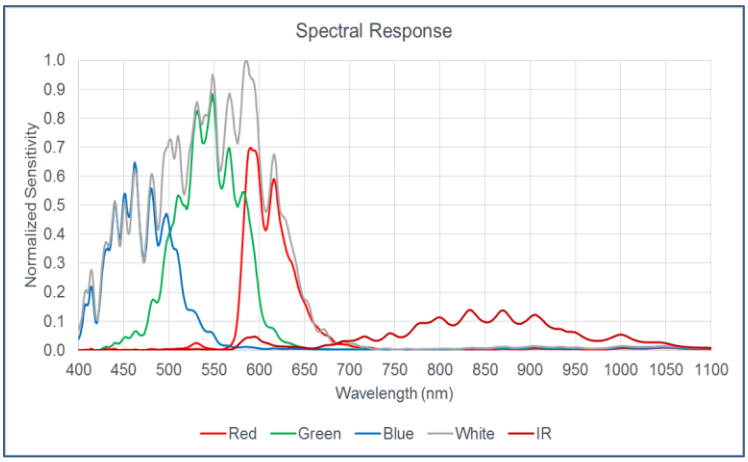
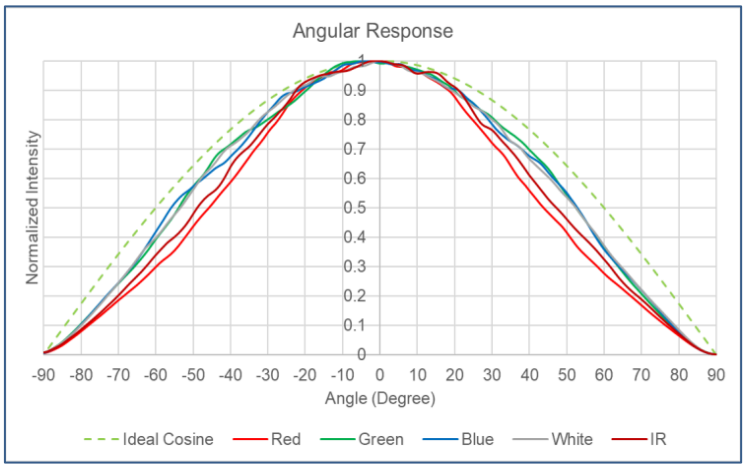
15. Typical Characteristics Curves

Unless otherwise specified, the following specifications apply over the operating ambient temperature T = 25˚C, VDD = 3.3V.

15.1 Spectral response



15.2 Angular response



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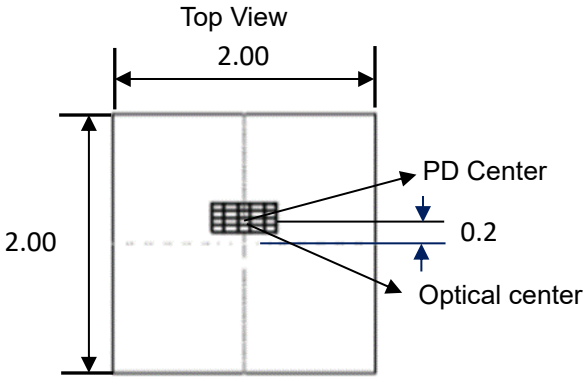
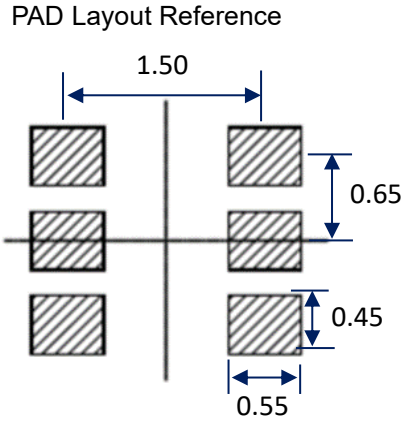
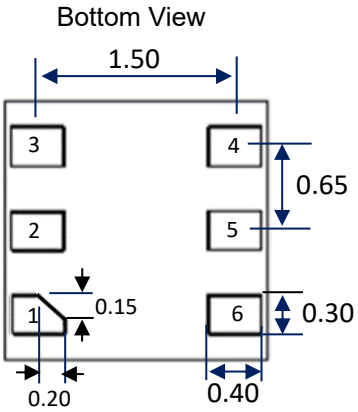
16. Package Outline







Pin Define

1. VDD
2. N.C.
3. GND
4. SCL
5. INT
6. SDA

Notes:

1. All dimensions are in millimeters.
2. All tolerances are ±0.1mm (0.004 inch) unless otherwise noted.

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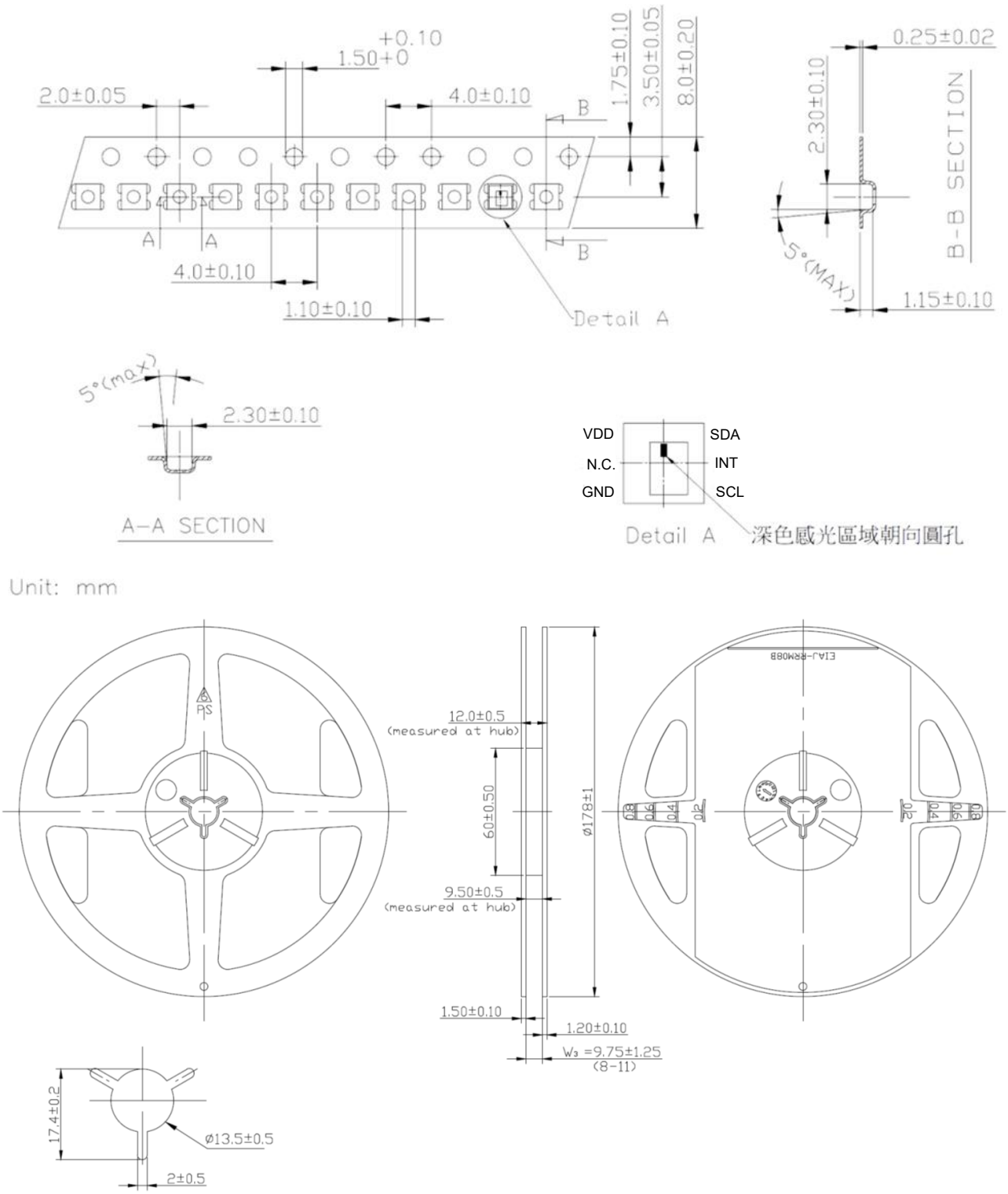
17. Tape and Reel Information



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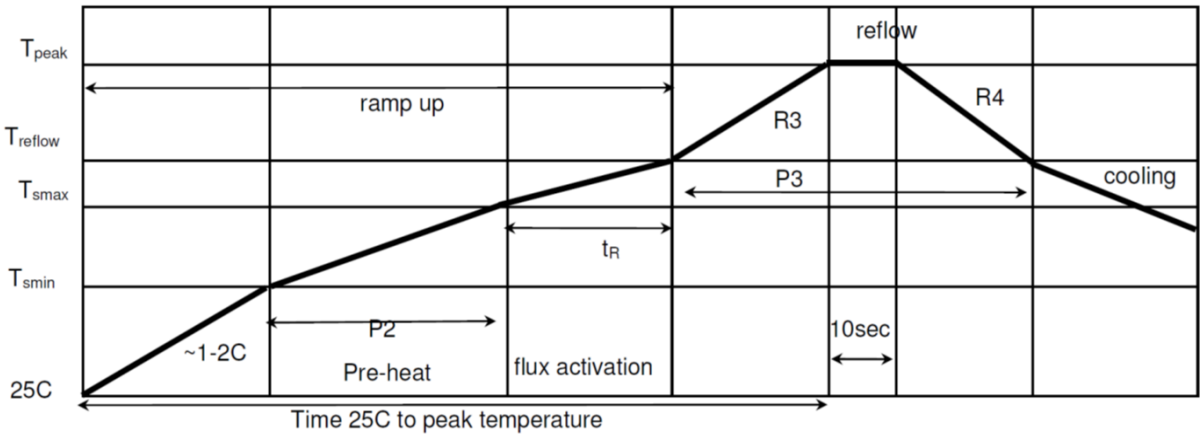
18. Recommended Reflow Profile



	Peak temperature (Tpeak)	255-260C (max) ; 10sec
Pre-Heat	Temperature min (Tsmin) Temperature max (Tsmax) P2: (Ts min to Ts max)	150C 2C/sec 150C-217C 100s to 180s 90-110s
Time maintain above	Temperature (T_{reflow}) Time (P3) R3 slope (from 217C -> peak) R4 slope (from peak -> 217C)	217C 60-90sec 2C/sec [typ] -> 2.5C/sec (max) -1.5C/sec [typ]-> -4C/sec (max)
	Time to peak temperature	480s max
	Cooling down slope (peak to 217C)	2-4C/ sec

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However, there is always a chance of failure due to unexpected factors.

Therefore, please take into account the derating characteristics and allow for sufficient safety features, such as extra margin, anti-flammability, and fail-safe measures when designing in order to prevent possible accidents that may result in bodily harm or fire caused by component failure.

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