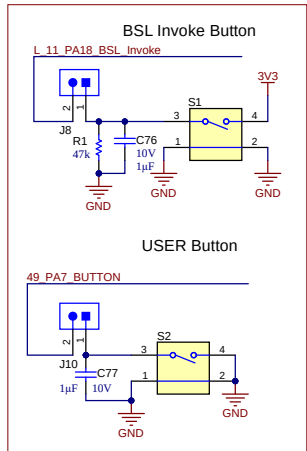
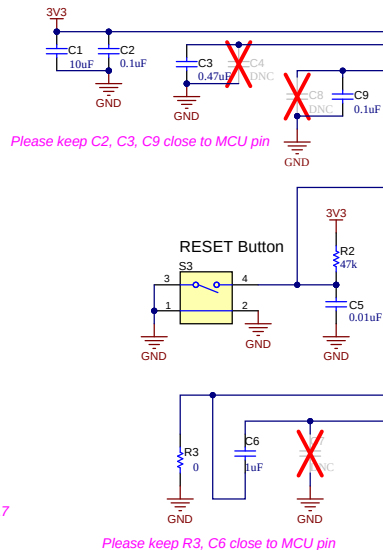




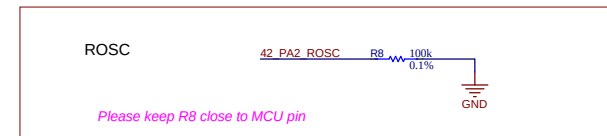
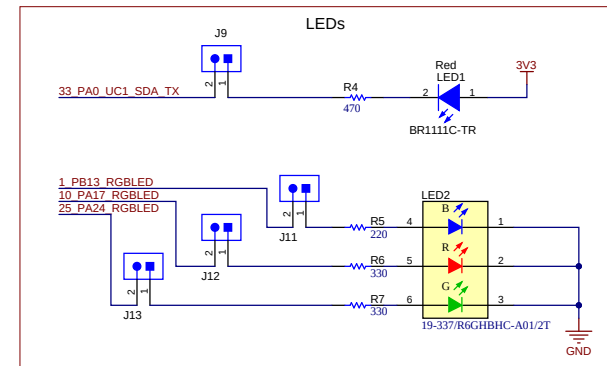
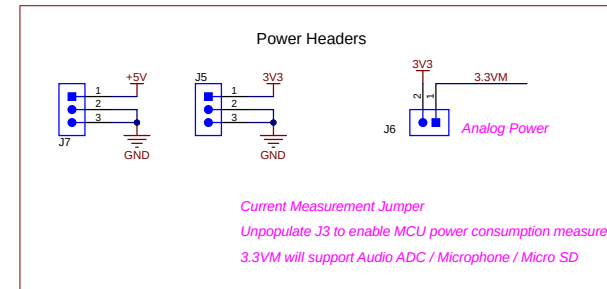
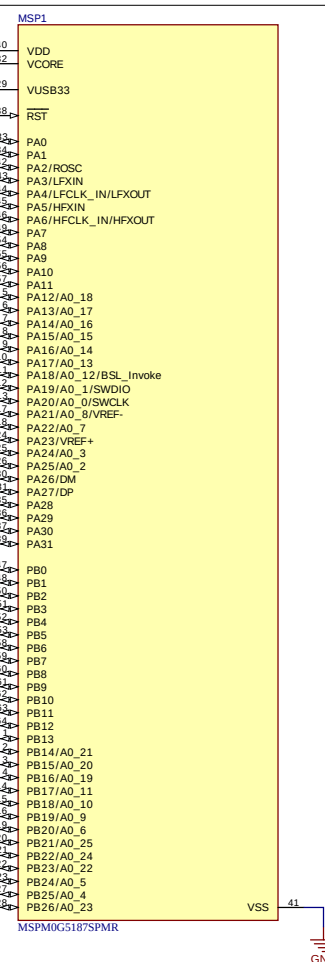
Add jumper to flexible choose the button pin, default is PA7



Low side SPI Interface - UC3

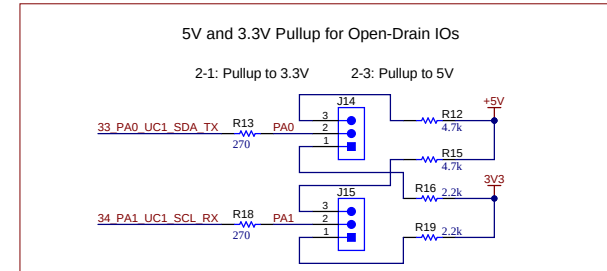
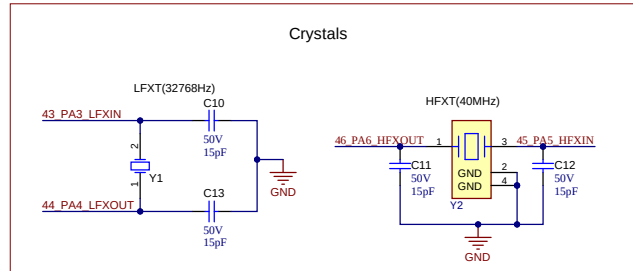
Low side Audio ADC Interface - I2S

32 VCORE	40	VDD VCORE	32
29 VUSB	29	VUSB33	29
RST	38	RST	38
33 PA0 UC1 SDA TX	33	PA0	33
34 PA1 UC1 SCL RX	34	PA1	34
42 PA2 ROSC	42	PA2/ROSC	42
43 PA3 LFXIN	43	PA3/LFXIN	43
44 PA4 LFXOUT	44	PA4/LFCLK_IN/LFXOUT	44
45 PA5 HFXIN	45	PA5/HFXIN	45
46 PA6 HFXOUT	46	PA6/HFCLK_IN/HFXOUT	46
49 PA7 BUTTON	49	PA7	49
54 PA8 UC1 SDA TX	54	PA8	54
55 PA9 UC1 SCL RX	55	PA9	55
56 PA10 UC0 SDA TX	56	PA10	56
57 PA11 UC0 SCL RX	57	PA11	57
5 PA12 I2S BCLK A0_18	5	PA12/A0_18	5
6 PA13 I2S AD0 A0_17	6	PA13/A0_17	6
7 PA14 I2S AD1 A0_16	7	PA14/A0_16	7
8 PA15 I2S WCLK A0_15	8	PA15/A0_15	8
9 PA16 I2S MCLK A0_14	9	PA16/A0_14	9
10 PA17 RGBLED	10	PA17/A0_13	10
11 PA18 BSL Invoke	11	PA18/A0_12/BSL Invoke	11
12 PA19 SWDIO	12	PA19/A0_11/SWDIO	12
13 PA20 SWCLK	13	PA20/A0_10/SWCLK	13
17 PA21 VREF-	17	PA21/A0_9/VREF-	17
18 PA22 CLKOUT	18	PA22/A0_8/VREF-	18
24 PA23 VREF+	24	PA23/A0_7	24
25 PA24 RGBLED	25	PA23/VREF+	25
26 PA25 A0_2	26	PA24/A0_3	26
30 PA26 DM	30	PA25/A0_2	30
31 PA27 DP	31	PA26/DM	31
35 PA28 TIMA0_C3	35	PA27/DP	35
36 PA29 UC2 CS3	36	PA28	36
37 PA30 UC2 CS2	37	PA29	37
39 PA31 TIMA0_C3N	39	PA30	39
		PA31	
47 PB0 TIMA0_C2	47	PB0	47
48 PB1 TIMA0_C2N	48	PB1	48
50 PB2 UC3 PICO TX	50	PB2	50
51 PB3 UC3 SCK RX	51	PB3	51
52 PB4 TIMA0_C1	52	PB4	52
53 PB5 TIMA0_C1N	53	PB5	53
58 PB6 UC3 CS0 CTS	58	PB6	58
59 PB7 UC3 POCI RTS	59	PB7	59
60 PB8 UC3 PICO TX	60	PB8	60
61 PB9 UC3 SCK RX	61	PB9	61
62 PB10 I2S WCLK	62	PB10	62
63 PB11 I2S BCLK	63	PB11	63
64 PB12 I2S AD0	64	PB12	64
1 PB13 RGBLED	1	PB13	1
2 PB14 A0_21	2	PB14/A0_21	2
3 PB15 A0_20	3	PB15/A0_20	3
4 PB16 A0_19	4	PB16/A0_19	4
14 PB17 UC2 PICO	14	PB17/A0_18	14
15 PB18 UC2 SCK	15	PB18/A0_17	15
16 PB19 UC2 POCI	16	PB19/A0_16	16
19 PB20 A0_6	19	PB20/A0_15	19
20 PB21 A0_25 COMP0 IN0+	20	PB21/A0_14	20
21 PB22 A0_24 COMP0 IN0-	21	PB22/A0_13	21
22 PB23	22	PB23/A0_12	22
23 PB24 UC2 CS1	23	PB24/A0_11	23
27 PB25 TIMA FAL0 COMP0 OUT	27	PB25/A0_10	27
28 PB26	28	PB26/A0_9	28



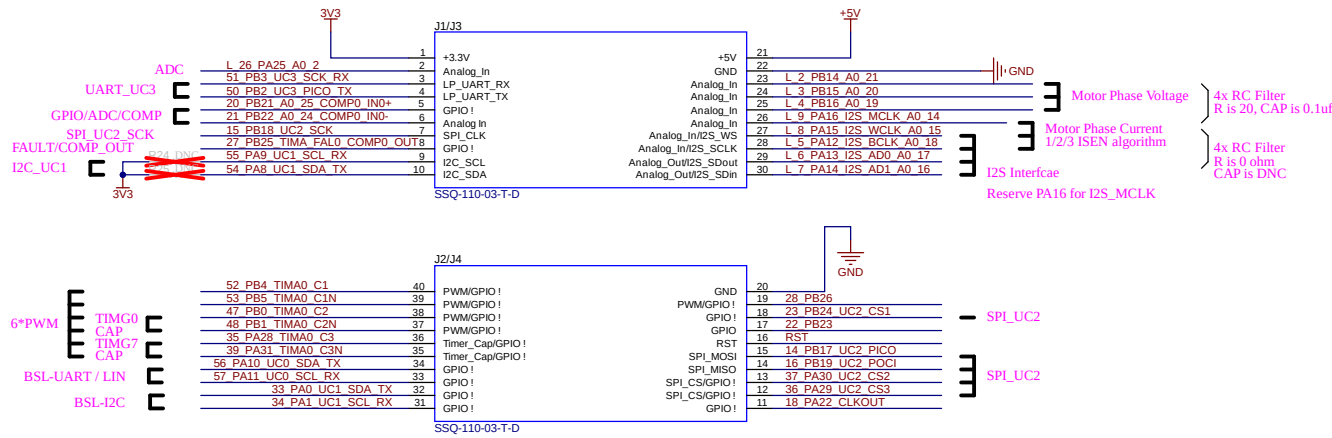
Isolation Resistors for Critical Signals

To Pin Headers	To MCU Pins
LS 42 PA2 ROSC	42 PA2 ROSC
LS 43 PA3 LFXIN	43 PA3 LFXIN
LS 44 PA4 LFXOUT	44 PA4 LFXOUT
LS 45 PA5 HFXIN	45 PA5 HFXIN
LS 46 PA6 HFXOUT	46 PA6 HFXOUT
LS 17 PA21 VREF-	17 PA21 VREF-
LS 24 PA23 VREF+	24 PA23 VREF+
L 11 PA18 BSL Invoke	11 PA18 BSL Invoke

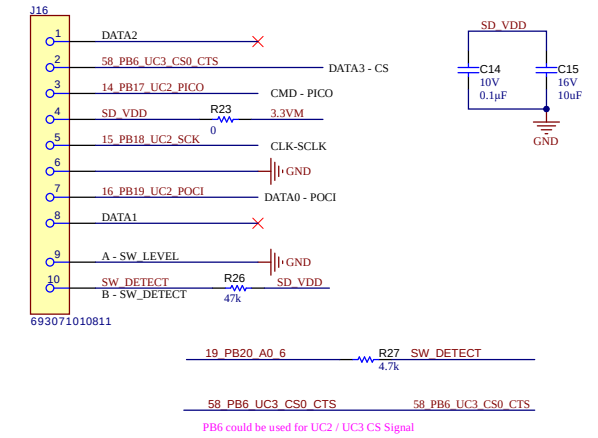


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BoosterPack Connectors

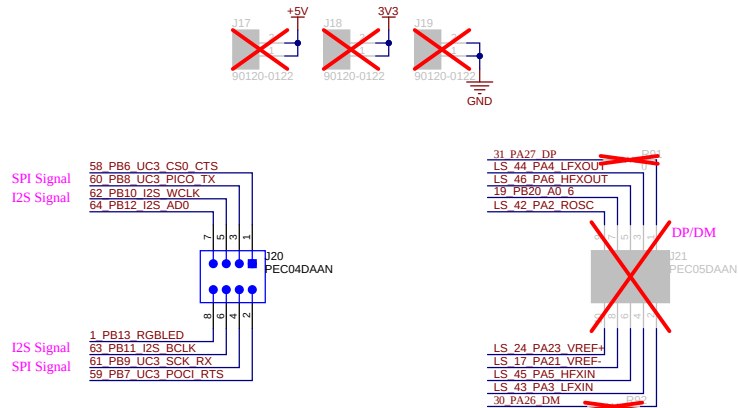


MicroSD Memory Card Interface

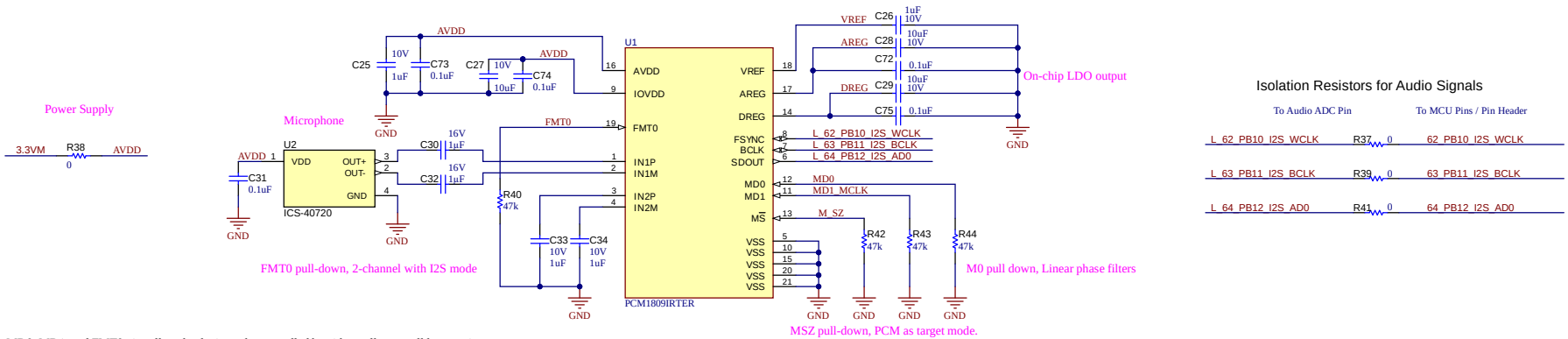


When SD plug in, the SPI interface used in BoosterPack will be occupied

Pin headers at the Low Side of the Board

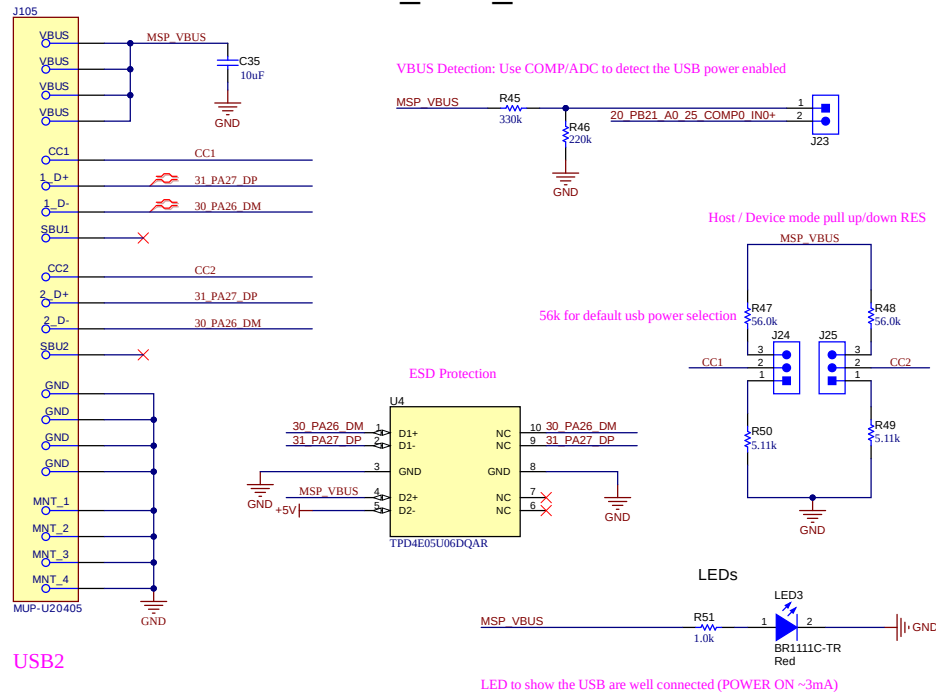


Audio ADC



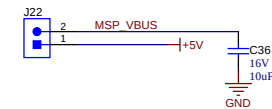
The MSZ, MD0, MD1, and FMT0 pins allow the device to be controlled by either pullup or pulldown resistors
Select fixed hardware connection to choose the PCM device mode with I2S format

A1_USB_Interface



USB HOST POWER SWITCH

Switch the 5V input from the USB interface



Connect J22 only when requires MCU work in the HOST mode

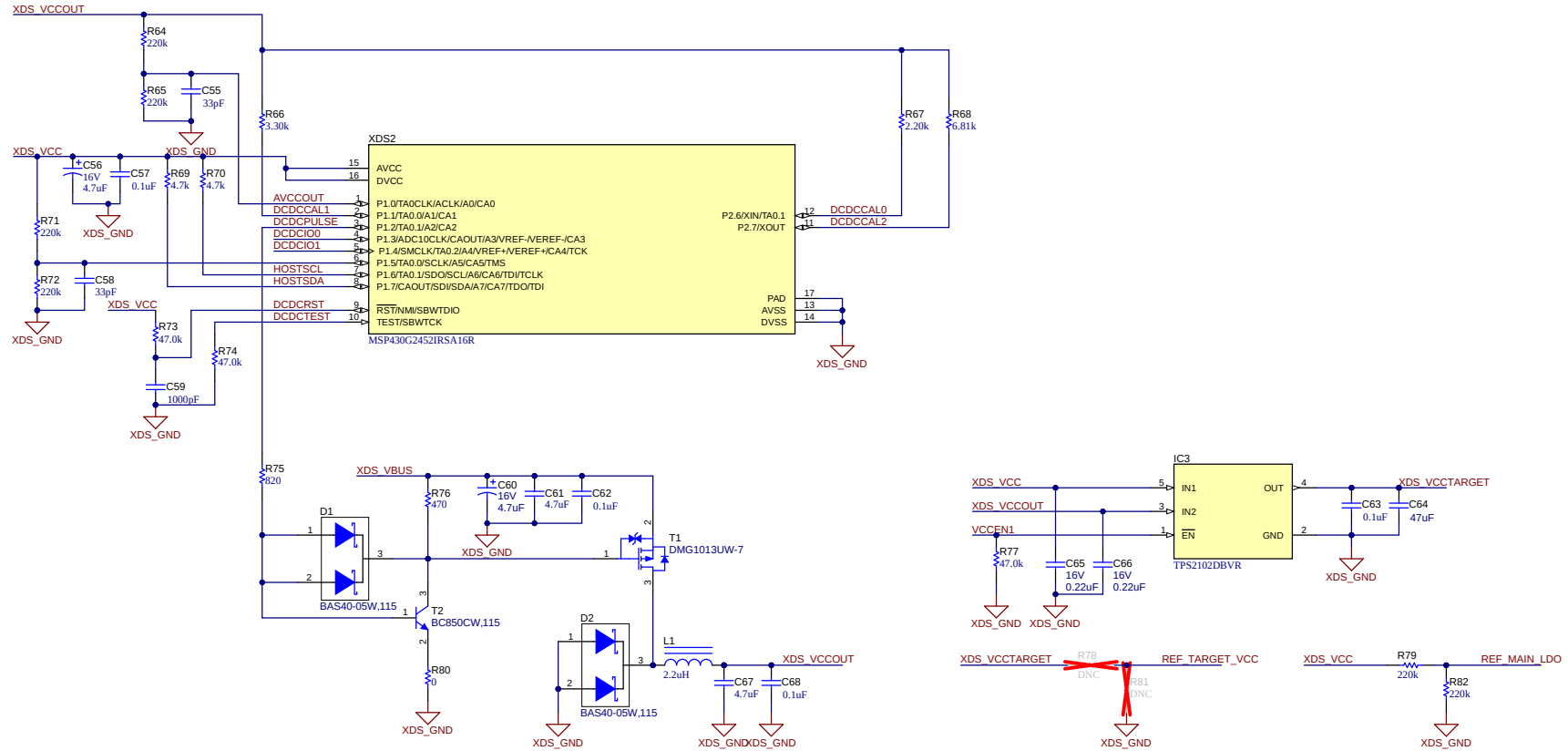
The USB VBUS can be get from +5V (From XDS110 or external 5V)

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Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/12/3
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170	Rev: A	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 3 of 8
Drawn By: Sal Ye	File: MCU170_03_MSPM0G5187_Target_Interface_340000B	http://www.ti.com
Engineer: Sal Ye	Contact: http://www.ti.com/support	© Texas Instruments, 2025

Software-controlled DCDC converter

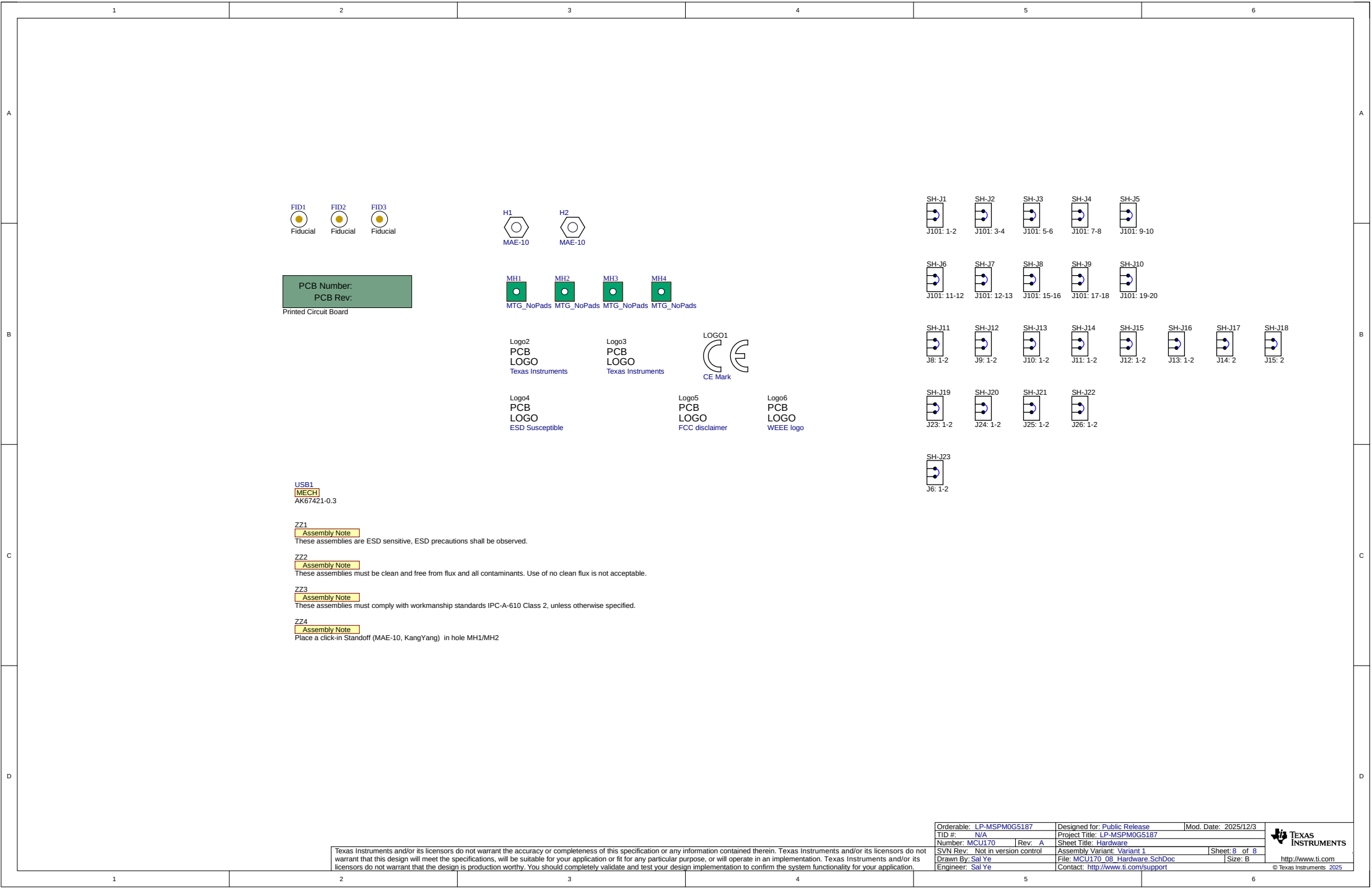
Energy measurement method protected under U.S. Patent
Application 13/329,073 and subsequent patent applications



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Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/12/3
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170	Rev: A	Sheet Title: XDS110-ET EnergyTrace
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 5 of 8
Drawn By: Sal Ye	File: MCU170_05_XDS110-ET_EnergyTrace.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

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SH-J11

J8: 1-2

SH-J12

J9: 1-2

SH-J13

J10: 1-2

SH-J14

J11: 1-2

SH-J15

J12: 1-2

SH-J16

J13: 1-2

SH-J17

J14: 2

SH-J18

J15: 2

SH-J19

J23: 1-2

SH-J20

J24: 1-2

SH-J21

J25: 1-2

SH-J22

J26: 1-2

SH-J23

J6: 1-2

Logo2

PCB

LOGO

Texas Instruments

Logo3

PCB

LOGO

Texas Instruments

Logo4

PCB

LOGO

ESD Susceptible

Logo5

PCB

LOGO

FCC disclaimer

Logo6

PCB

LOGO

WEEE logo

Logo1

CE Mark

Logo1

CE Mark

PCB Number:

PCB Rev:

Printed Circuit Board

USB1

MECH

AK67421-0.3

ZZ1

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ4

Assembly Note

Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

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Orderable: LP-MSPM0G5187

Designed for: Public Release

Mod. Date: 2025/12/3

TID #: N/A

Project Title: LP-MSPM0G5187

Number: MCU170

Rev: A

Sheet Title: Hardware

SVN Rev: Not in version control

Assembly Variant: Variant 1

Sheet: 8 of 8

Drawn By: Sal Ye

File: MCU170_08_Hardware.SchDoc

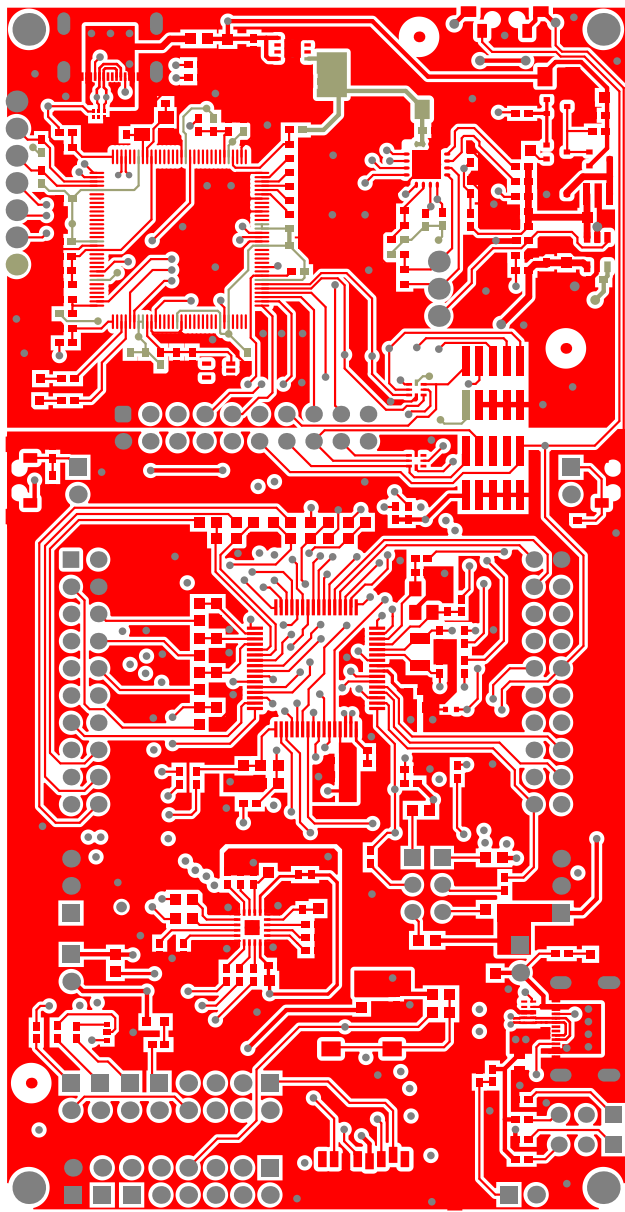
Size: B

Engineer: Sal Ye

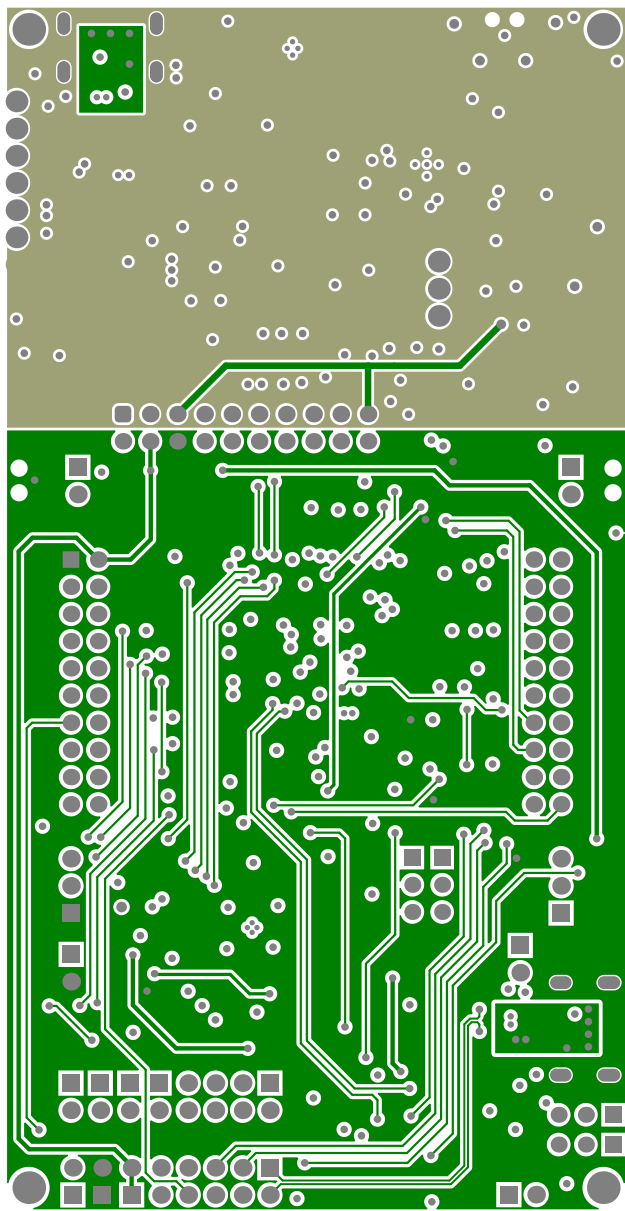
Contact: http://www.ti.com/support

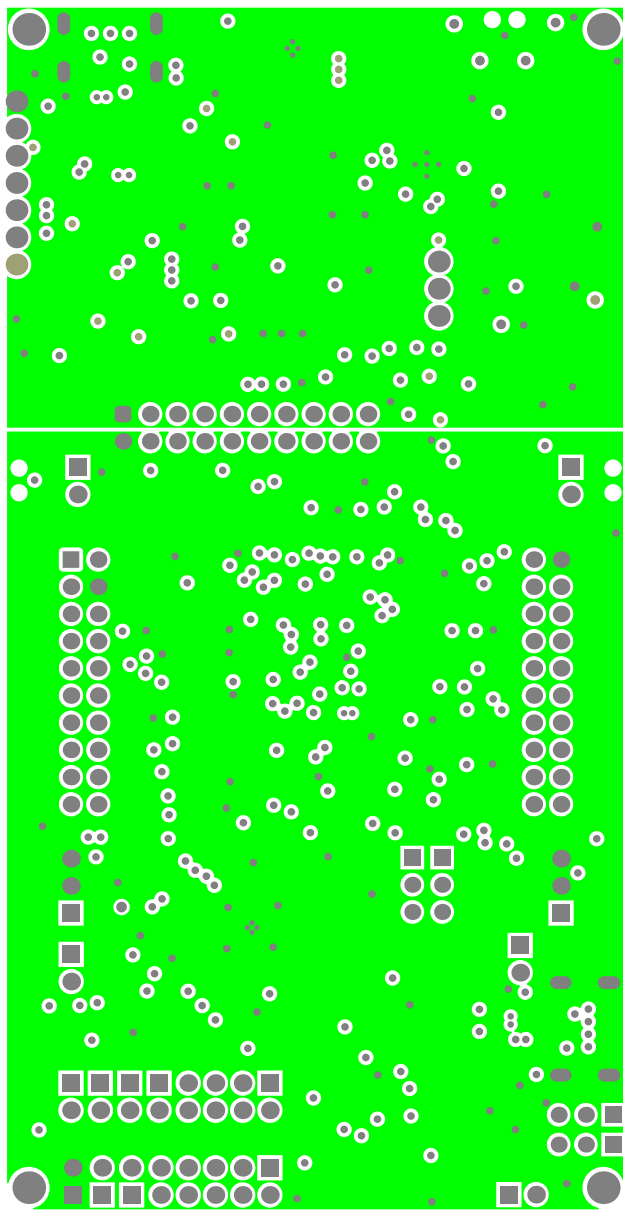
http://www.ti.com

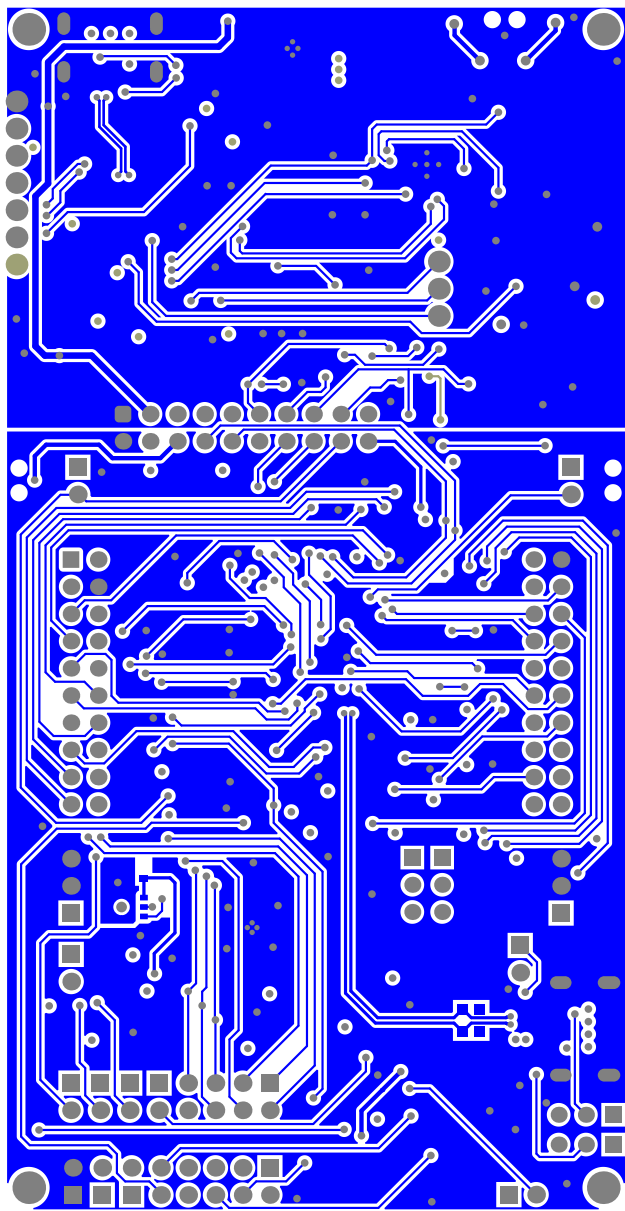
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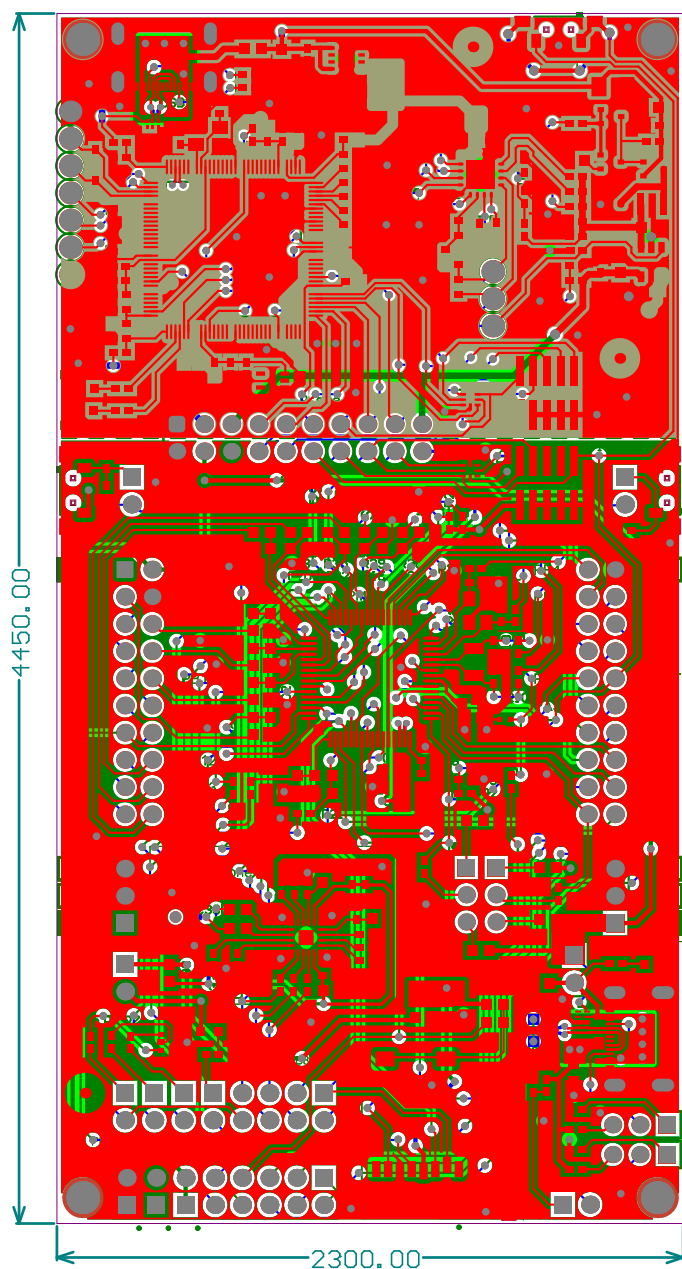
Top Layer







Bottom Layer



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance	Hole Length
□	6	35.43mil (0.900mm)	NPTH	Round	Top Layer - Bottom Layer		-
⊞	4	125.00mil (3.175mm)	NPTH	Round	Top Layer - Bottom Layer		-
⊙	13	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer		-
✱	301	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer		-
▼	8	20.00mil (0.508mm)	PTH	Round	Top Layer - Bottom Layer		-
○	1	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer		-
▽	90	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer		-
✕	40	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer		-
✱	4	55.12mil (1.400mm)	PTH	Slot	Top Layer - Bottom Layer		23.62mil (0.600mm)
□	4	55.06mil (1.500mm)	PTH	Slot	Top Layer - Bottom Layer		23.62mil (0.600mm)
471 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SH-004	0.99mil	4	
	Top Layer		1.40mil		
1	Dielectric 2	FR-4	8.40mil	4.2	
	VCC Layer		1.40mil		
2	Dielectric1	FR-4	40.00mil	4.2	
	GND Layer		1.40mil		
3	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SH-004	0.99mil	4	
	Bottom Overlay				

IMPEDANCE TABLE | MSPM0 USB 2.0 Full Speed

SIGNAL	LAYER	WIDTH	GAP	IMPEDANCE	TOL.
		(mil)	(mil)	(Differential)	
MSP_USB	TOP	9.6	6	90 Ohm	+/- 10%
	VCC	7.4	8	90 Ohm	+/- 10%
	BOTTOM	11.6	8	90 Ohm	+/- 10%