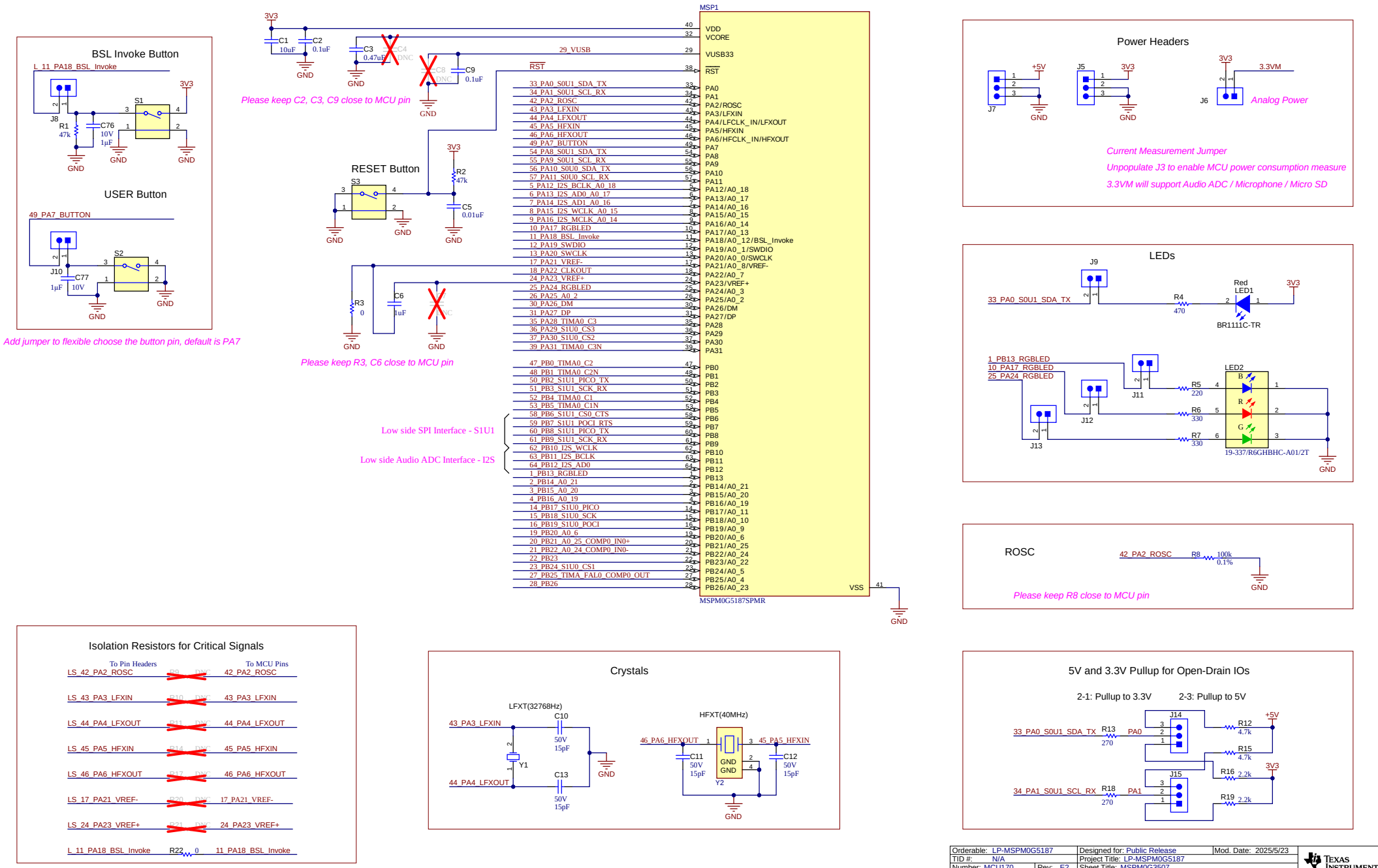


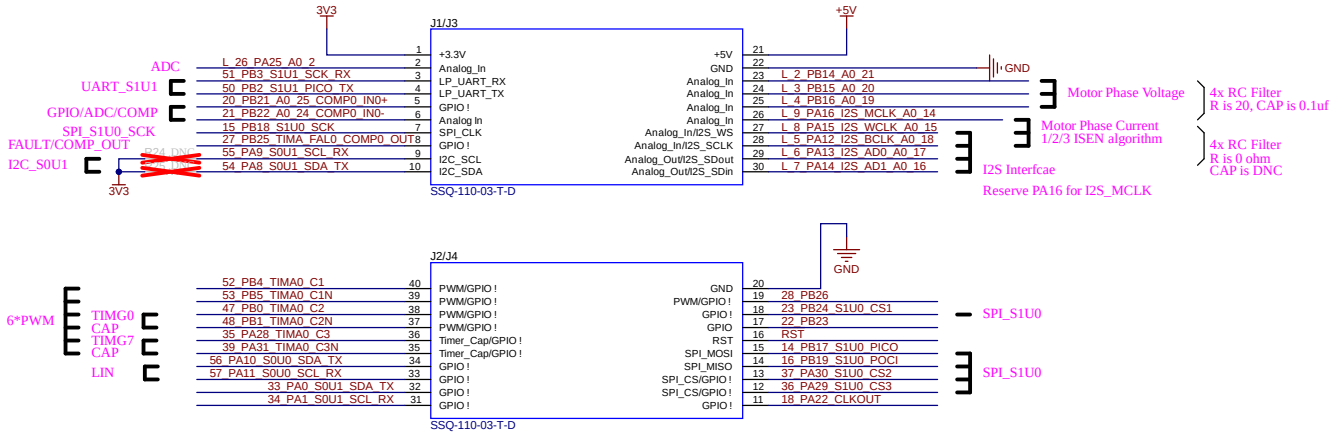
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Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/5/23
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170 Rev: E2	Sheet Title: MSPM0G3507	
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 1 of 8
Drawn By: N/A	File: MCU170_01_MSPM0G5187_Target_Device.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

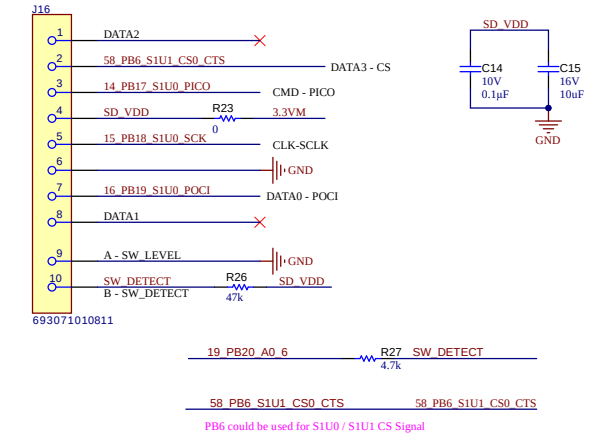
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BoosterPack Connectors

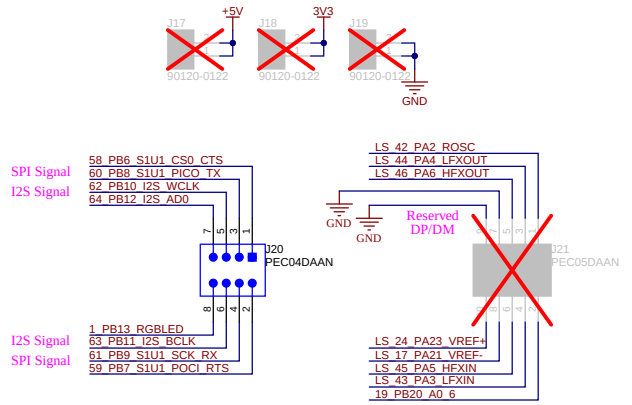


MicroSD Memory Card Interface

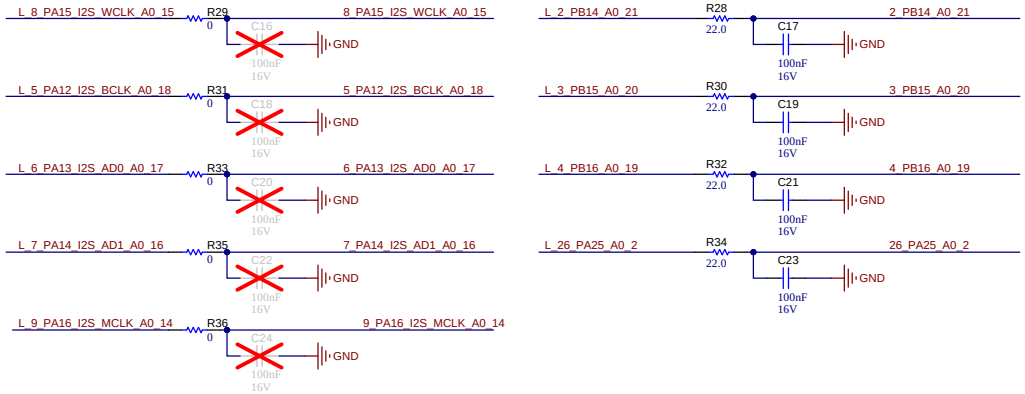


When SD plug in, the SPI interface used in BoosterPack will be occupied

Pin headers at the Low Side of the Board



RC Filter for ADC Input



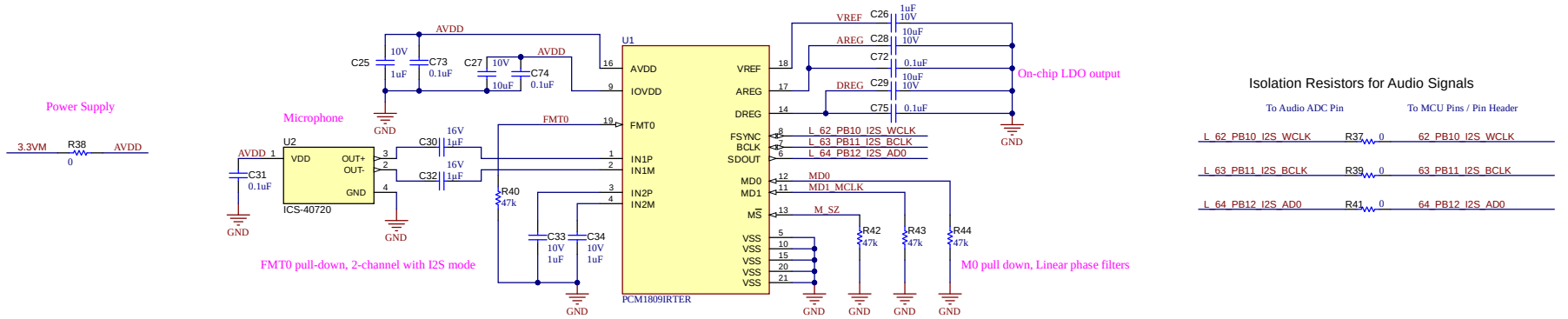
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Orderable: LP-MSPM0G5187		Designed for: Public Release	Mod. Date: 2025/5/21
TID #: N/A		Project Title: LP-MSPM0G5187	
Number: MCU170	Rev: E2	Sheet Title: BoosterPack Connectors	
SVN Rev: Not in version control		Assembly Variant: Variant 1	Sheet: 2 of 8
Drawn By: N/A		File: MCU170_02_BoosterPack_Connectors.SchDoc	Size: B
Engineer: Sal Ye		Contact: http://www.ti.com/support	

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Audio ADC



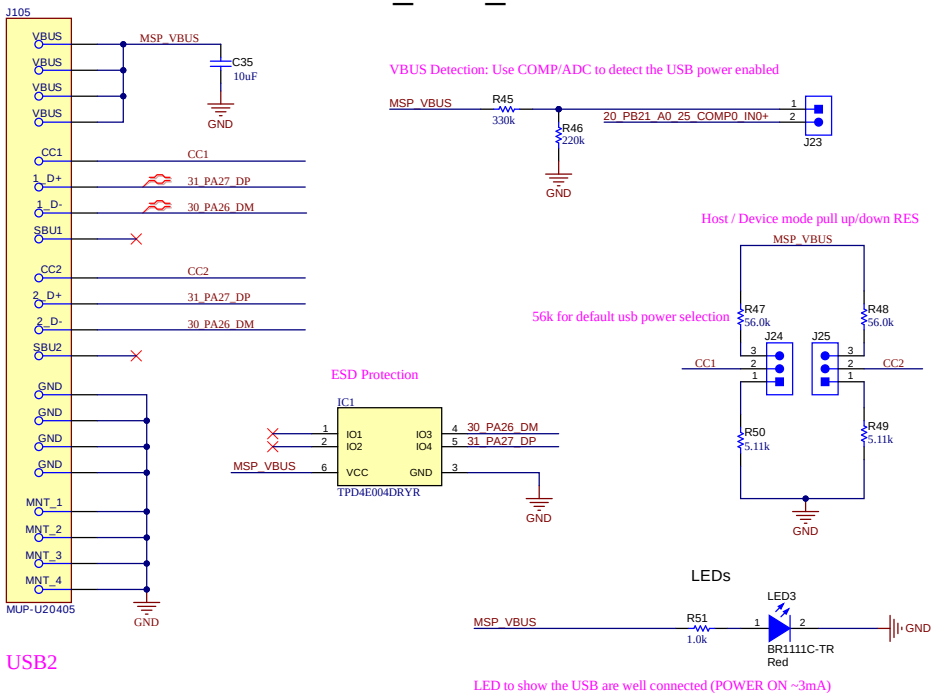
Isolation Resistors for Audio Signals

To Audio ADC Pin		To MCU Pins / Pin Header
L_62_PB10_I2S_WCLK	R37 0	62_PB10_I2S_WCLK
L_63_PB11_I2S_BCLK	R39 0	63_PB11_I2S_BCLK
L_64_PB12_I2S_AD0	R41 0	64_PB12_I2S_AD0

The MSZ, MD0, MD1, and FMT0 pins allow the device to be controlled by either pullup or pulldown resistors

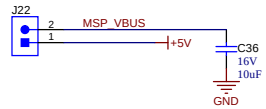
Select fixed hardware connection to choose the PCM device mode with I2S format

A1_USB_Interface



USB HOST POWER SWITCH

Switch the 5V input from the USB interface



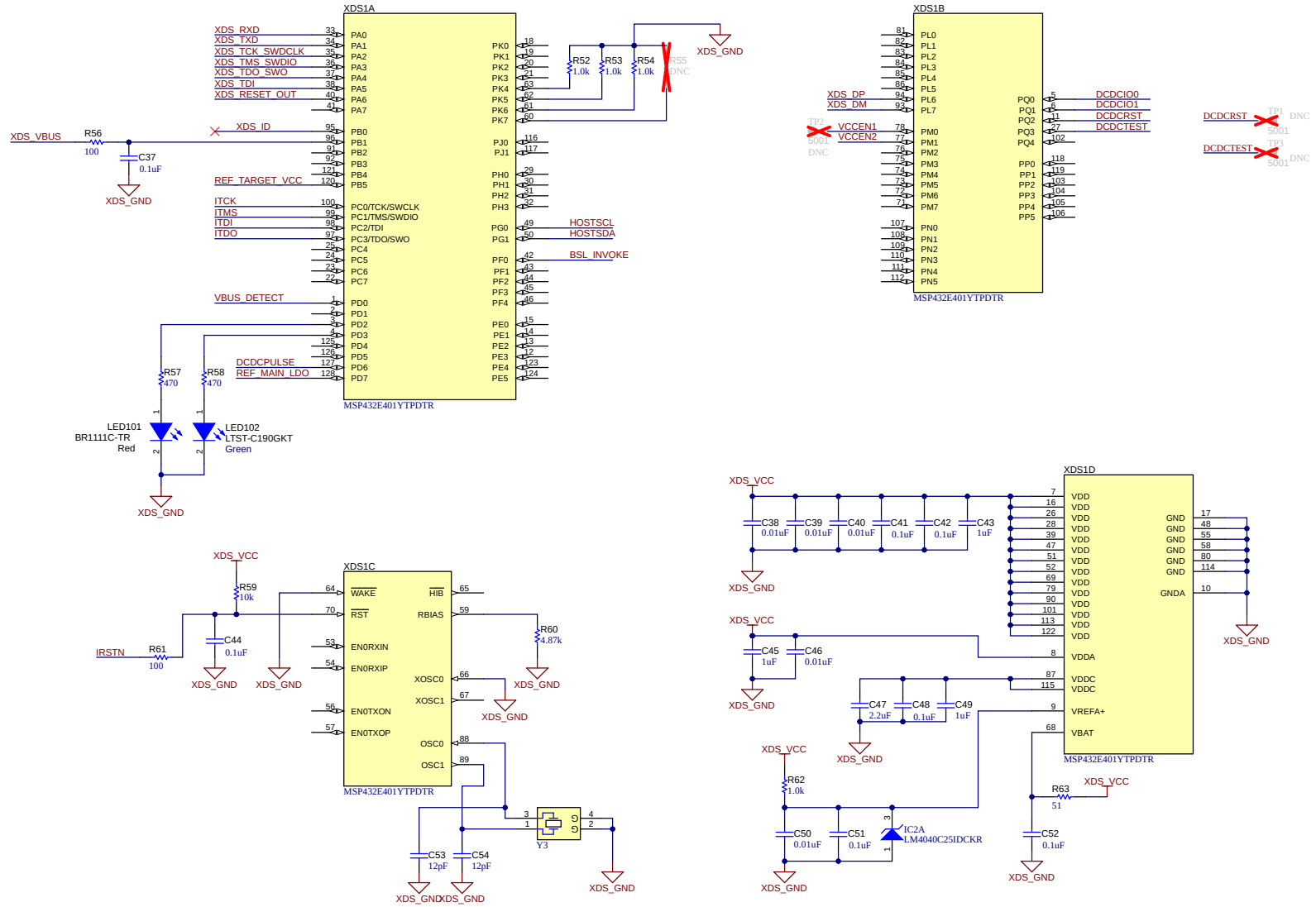
Connect J22 only when requires MCU work in the HOST mode

The 5V can be get from +5V (From XDS110 or external 5V)

Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/5/20
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170 Rev: E2	Sheet Title:	
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 3 of 8
Drawn By: N/A	File: MCU170_03_MSPM0G5187_Target_Interface.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

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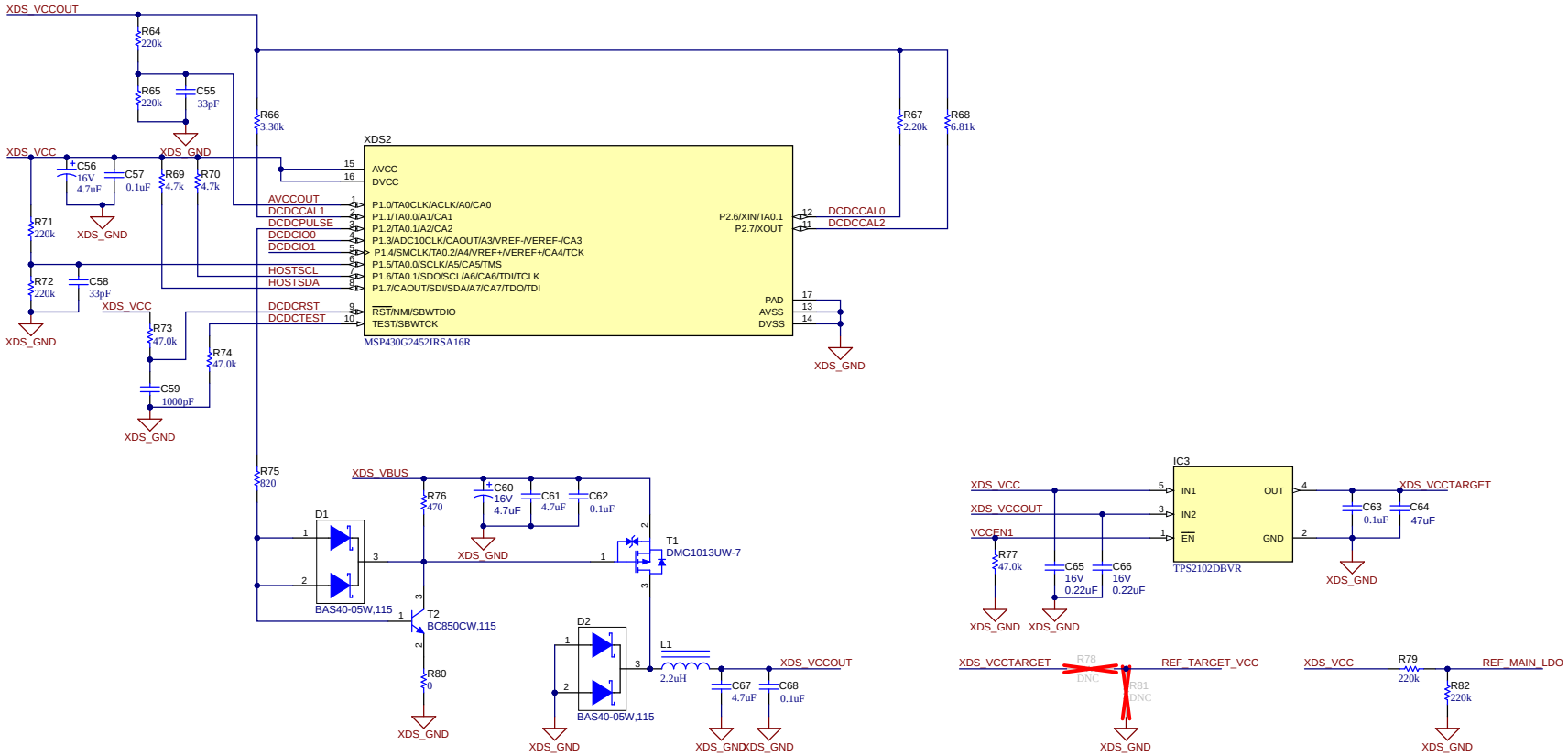
Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/5/20
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170 Rev: E2	Sheet Title: XDS110-ET Debug Probe	
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 4 of 8
Drawn By: N/A	File: MCU170_04_XDS110_Debug_Probe.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

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Software-controlled DCDC converter

Energy measurement method protected under U.S. Patent
Application 13/329,073 and subsequent patent applications



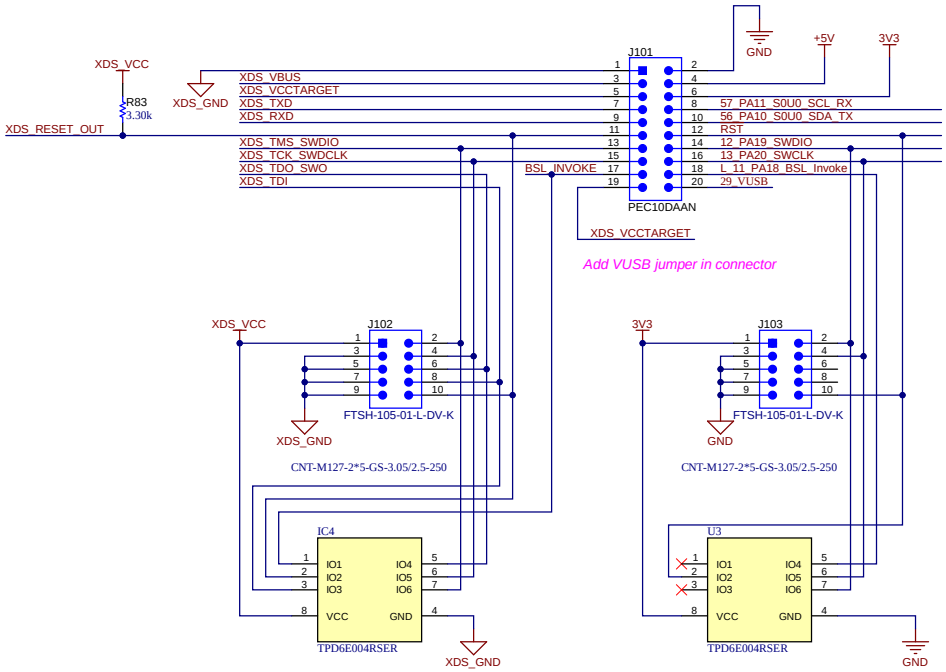
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Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/5/20
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170 Rev: E2	Sheet Title: XDS110-ET EnergyTrace	
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 5 of 8
Drawn By: N/A	File: MCU170_05_XDS110-ET_EnergyTrace.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

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XDS110-ET <<---->> LaunchPad

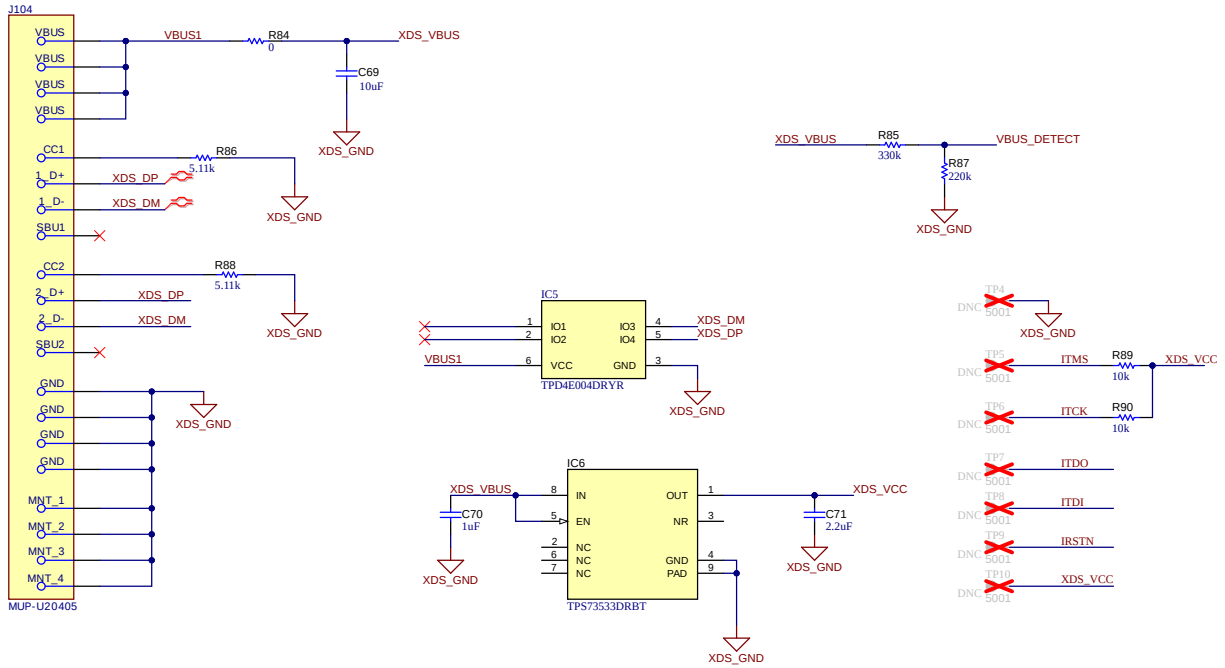


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Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/5/20
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170 Rev: E2	Sheet Title: XDS110-ET Interface	
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 6 of 8
Drawn By: N/A	File: MCU170_06_XDS110_Target_Interface.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

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Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/5/20
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170 Rev: E2	Sheet Title: XDS110-ET USB Power	
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 7 of 8
Drawn By: N/A	File: MCU170_07_XDS110-ET_USB_Power.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

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FID1 Fiducial

FID2 Fiducial

FID3 Fiducial

H1 MAE-10

H2 MAE-10

PCB Number:
PCB Rev:
Printed Circuit Board

MH1 MTG_NoPads

MH2 MTG_NoPads

MH3 MTG_NoPads

MH4 MTG_NoPads

Logo2
PCB
LOGO
Texas Instruments

Logo3
PCB
LOGO
Texas Instruments

LOGO1
CE Mark

Logo4
PCB
LOGO
ESD Susceptible

Logo5
PCB
LOGO
FCC disclaimer

Logo6
PCB
LOGO
WEEE logo

SH-J1 J101: 1-2

SH-J2 J101: 3-4

SH-J3 J101: 5-6

SH-J4 J101: 7-8

SH-J5 J101: 9-10

SH-J6 J101: 11-12

SH-J7 J101: 12-13

SH-J8 J101: 15-16

SH-J9 J101: 17-18

SH-J10 J101: 19-20

SH-J11 J8: 1-2

SH-J12 J9: 1-2

SH-J13 J10: 1-2

SH-J14 J11: 1-2

SH-J15 J12: 1-2

SH-J16 J13: 1-2

SH-J17 J14: 2

SH-J18 J15: 2

SH-J19 J23: 1-2

SH-J20 J24: 1-2

SH-J21 J25: 1-2

SH-J22 J26: 1-2

SH-J23 J6: 1-2

USB1
MECH
AK67421-0.3

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ4
Assembly Note
Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

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Orderable: LP-MSPM0G5187	Designed for: Public Release	Mod. Date: 2025/5/20
TID #: N/A	Project Title: LP-MSPM0G5187	
Number: MCU170 Rev: E2	Sheet Title: Hardware	
SVN Rev: Not in version control	Assembly Variant: Variant 1	Sheet: 8 of 8
Drawn By: N/A	File: MCU170_08_Hardware.SchDoc	Size: B
Engineer: Sal Ye	Contact: http://www.ti.com/support	

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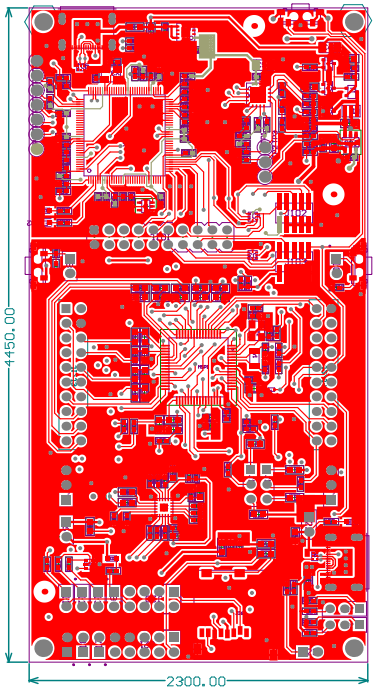
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Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.4mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.4mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.4mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.4mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				





COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:
LP-MSPM0G5187

DESIGNED FOR:
Public Release

FILE NAME:
MCU70_MSPM0G5187_PCB.PcbDoc

PCB [illegible]	SW REV: Not in version control
LAYER NAME = [illegible]	TID #: N/A
PLOT NAME = [illegible]	GENERATED: 2025/5/23 20:06:14

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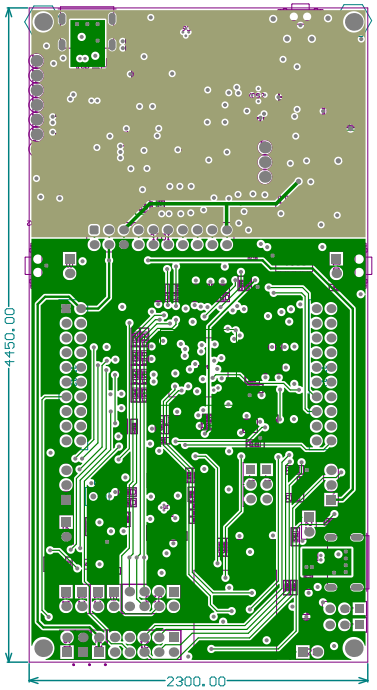
ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.4mil		
	Dielectric 2	FR-4	8.4mil	4.2	
2	VCC Layer		1.4mil		
	Dielectric1	FR-4	40.04mil	4.2	
3	GND Layer		1.4mil		
	Dielectric 3	FR-4	8.4mil	4.2	
4	Bottom Layer		1.4mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION			
MIN. TRACK WIDTH:	8	MIL	
MIN. CLEARANCE:	0.2	mm	
MIN. VIA PAD SIZE:	24	MIL	
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL	HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL:
- [ ] FR-408 [X] FR-4 High Tg [ ] OTHER
- THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
- TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
- BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
- REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
- PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
- SILKSCREEN: [X] TOP [X] BOTTOM
- SILKSCREEN COLOR: [X] WHITE [ ] OTHER
- SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red
- [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
- [X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL:
- [ ] CUT AND TRIM PER M1 BOARD OUTLINE
- [ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
- [X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
- [X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
- MICROSECTION: [ ] YES
- BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:
LP-MSPM0G5187

DESIGNED FOR:
Public Release

FILE NAME:
MCU70_MSPM0G5187_PCB.PcbDoc

PCB [illegible]	E2	SW REV: Not in version control	
LAYER NAME =		TID #: N/A	
PLOT NAME =		GENERATED: 2025/5/23 20:06:14	TEXAS INSTRUMENTS

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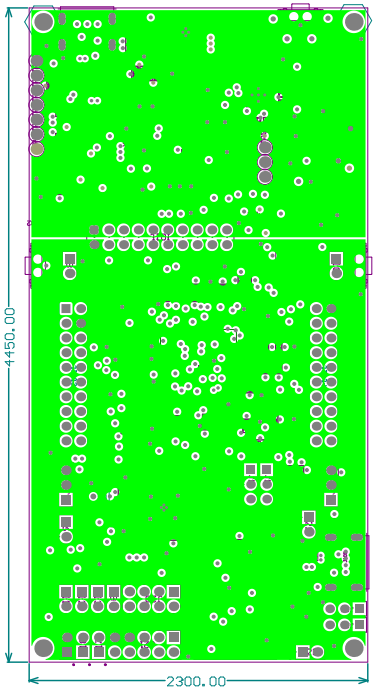
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.4mil		
	Dielectric 2	FR-4	8.4mil	4.2	
2	VCC Layer		1.4mil		
	Dielectric1	FR-4	40.04mil	4.2	
3	GND Layer		1.4mil		
	Dielectric 3	FR-4	8.4mil	4.2	
4	Bottom Layer		1.4mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				





COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION					
MIN. TRACK WIDTH:	8	MIL			
MIN. CLEARANCE:	0.2	mm			
MIN. VIA PAD SIZE:	24	MIL			
MINIMUM ANNULAR RING	0.05mm (2MIL)		EXTERNAL		
PER	IPC-D-275 CLASS 2 LEVEL C				
REGISTRATION TOLERANCES:	METAL	+/-	5	MIL HOLES	+/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):					+/- 3 MIL

MATERIAL:
- [ ] FR-408 [X] FR-4 High Tg [ ] OTHER
- THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
- TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
- BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
- REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
- PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
- SILKSCREEN: [X] TOP [X] BOTTOM
- SILKSCREEN COLOR: [X] WHITE [ ] OTHER
- SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red
- [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
- [X] MM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
- [ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
- [X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
- [X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
- MICROSECTION: [ ] YES
- BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:
LP-MSPM0G5187

DESIGNED FOR:
Public Release

FILE NAME:
MCU70_MSPM0G5187_PCB.PcbDoc

PCB [illegible]	Not in version control	E2	SVN REV:
LAYER NAME =		TID #: N/A	BOARD #: MCU70
PLOT NAME =		GENERATED: 2025/5/23	TEXAS INSTRUMENTS

ENGINEER: Sal Ye

LAYOUT BY: Sal Ye

SCALE: 1.00

ALTIUM DESIGNER VERSION: 23.4.1.23

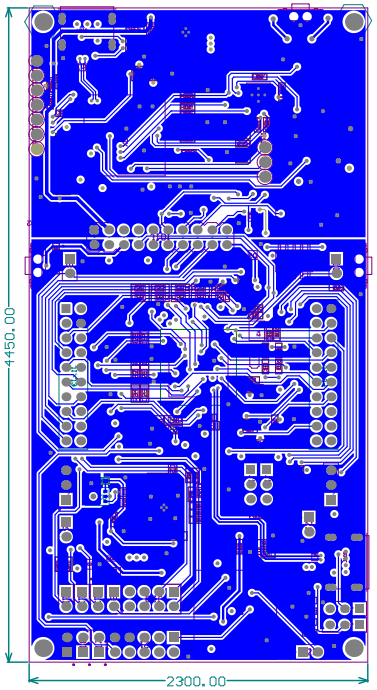
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Z24 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.4mil		
	Dielectric 2	FR-4	8.4mil	4.2	
2	VCC Layer		1.4mil		
	Dielectric1	FR-4	40.0mil	4.2	
3	GND Layer		1.4mil		
	Dielectric 3	FR-4	8.4mil	4.2	
4	Bottom Layer		1.4mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				





COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION					
MIN. TRACK WIDTH:	8	MIL			
MIN. CLEARANCE:	0.2	mm			
MIN. VIA PAD SIZE:	24	MIL			
MINIMUM ANNULAR RING	0.05mm (2MIL)		EXTERNAL		
PER	IPC-D-275 CLASS 2 LEVEL C				
REGISTRATION TOLERANCES:	METAL	+/-	5	MIL HOLES	+/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):					+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:
LP-MSPM0G5187

DESIGNED FOR:
Public Release

FILE NAME:
MCU70_MSPM0G5187_PCB.PcbDoc

PCB PART NUMBER:	Not in version control	SVN REV:	E2	BOARD #:	MCU70	MCU70	# BOARD:
LAYER NAME =				TID #:	N/A	N/A	TID #:
PLOT NAME =				GENERATED	2025-5-23	2025/5/23	GENERATED

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

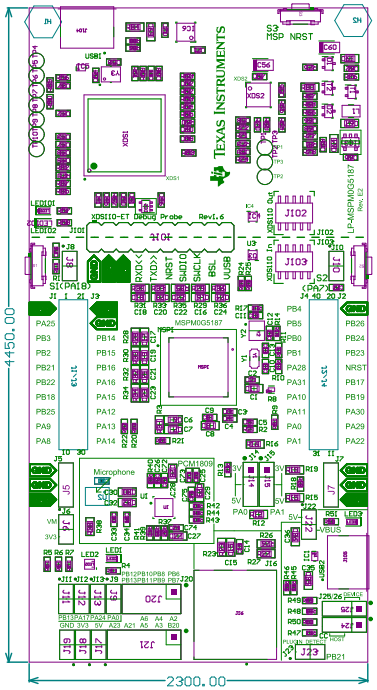
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

1000.00mil

DESIGN INFORMATION			
MIN. TRACK WIDTH:	8 MIL		
MIN. CLEARANCE:	0.2 mm		
MIN. VIA PAD SIZE:	24 MIL		
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/- 5 MIL	HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):		+/- 3 MIL	

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING: REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB NUMBER FROM BOTTOM		SVN REV:	Not in version control	E2	BOARD #:	MCU70	MCU70
LAYER NAME =		TID #:					
PLOT NAME =	TEXAS INSTRUMENTS Overlay	GENERATED	2025/5/23	20:06:16			

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TEXAS INSTRUMENTS

PROJECT TITLE: LP-MSPM0G5187

DESIGNED FOR: Public Release

FILE NAME: MCU70_MSPM0G5187_PCB.PcbDoc

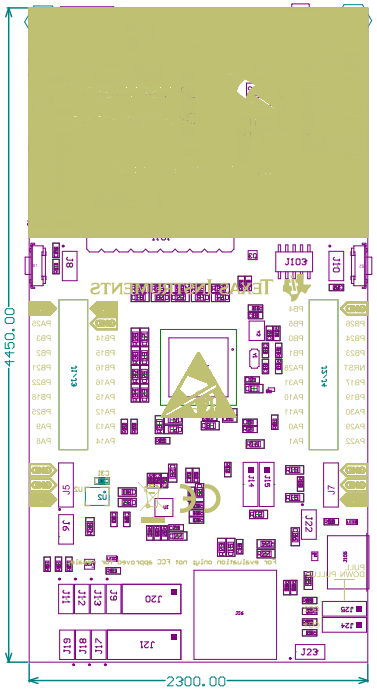
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Bottom Overlay



Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB NUMBER: [illegible]	SW REV: Not in version control	E3	BOARD #: MCU70	MCU70	# BOARD	E2	SW REV: Not in version control
LAYER NAME = [illegible]			TID #: N/A	N/A	TID #		
PLOT NAME = [illegible]Screen Overlay		[illegible]	GENERATED	2025/5/23	GENERATED	20:08:17	PLOT NAME = [illegible]Screen Overlay

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TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

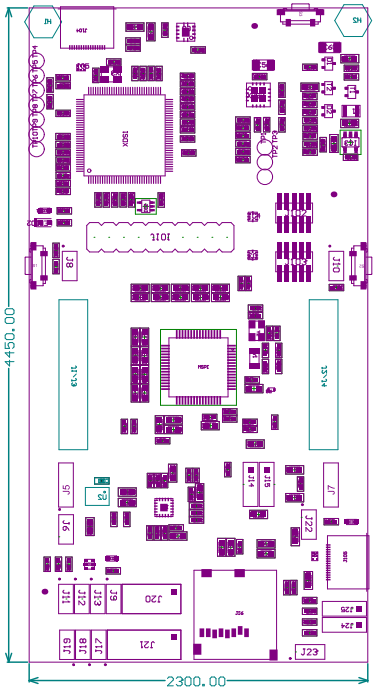
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.4mil		
	Dielectric 2	FR-4	8.4mil	4.2	
2	VCC Layer		1.4mil		
	Dielectric1	FR-4	40.04mil	4.2	
3	GND Layer		1.4mil		
	Dielectric 3	FR-4	8.4mil	4.2	
4	Bottom Layer		1.4mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVA REV:	E3	BOARD #:	MCU70	MCU70	#: [illegible]	E2
LAYER NAME =	[illegible]		TID #:	N/A	N/A	TID #:	
PLOT NAME =	[illegible] Mask Print		GENERATED	2025/5/23	[illegible]	20:06:18	

SVA REV: Not in version control

PCB VIEWED FROM BOTTOM

PLOT NAME = [illegible]

TEXAS INSTRUMENTS

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DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

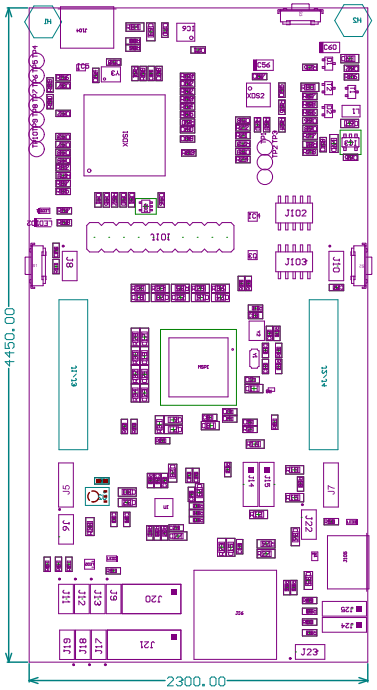
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVN REV:	E3	BOARD #:	MCU570_MCU570	#: [illegible]
LAYER NAME =	[illegible]		TID #:	N/A	N/A
PLOT NAME =	[illegible] Mask Print		GENERATED	2025/5/23	20:06:19

PCB [illegible]	E2	SVN REV: Not in version control
BOARD #:	MCU570_MCU570	#: [illegible]
TID #:	N/A	N/A
GENERATED	2025/5/23	20:06:19

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TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU570_MSPM0G5187_PCB.PcbDoc

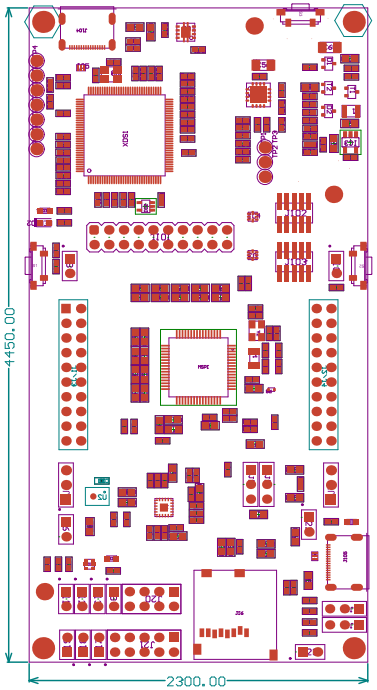
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVN REV:	E3	BOARD #:	MCU70	MCU70	S #: [illegible]	E2
LAYER NAME =			TID #:	N/A	N/A	TID #:	
PLOT NAME =			GENERATED	2025/5/23	2025-5-23	GENERATED	20:06:19

SVN REV: E2

PCB NAME = MCU70_MSPM0G5187_PCB.PcbDoc

PLOT NAME = TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

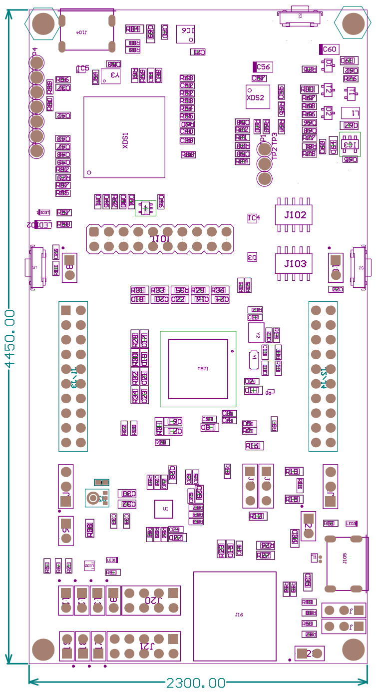
1 2 3 4 5 6

ZZ4 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

ZZ3 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 / [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 / [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red / [X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG / [X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE / [ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: LP-MSPM0G5187

DESIGNED FOR: Public Release

FILE NAME: MCU170_MSPM0G5187_PCB.PcbDoc

PCB VIEWED FROM BOTTOM SIDE

SVN REV: Not in version control

BOARD #: MCU170 REV: E2

LAYER NAME = Bottom

TID #: N/A

PLOT NAME = Bottom Solder Mask Print

GENERATED 2025/5/23 20:06:20

TEXAS INSTRUMENTS

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ENGINEER: Sal Ye

LAYOUT BY: Sal Ye

SCALE: 1.00

ALTIUM DESIGNER VERSION: 23.4.1.23

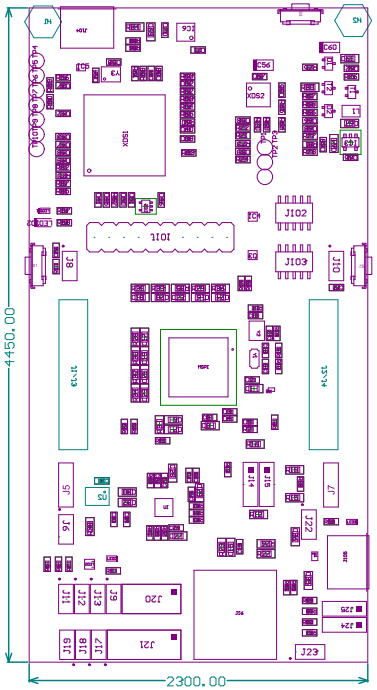
1 2 3 4 5 6

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	REV: [illegible]	E3	BOARD #:	MCU570	#: [illegible]
LAYER NAME =	[illegible]		TID #:	N/A	TID #:
PLOT NAME =	[illegible]		GENERATED	2025/5/23	GENERATED

MCU570	#: [illegible]	E2	SVA REV: Not in version control
N/A	TID #:		
2025/5/23	GENERATED	20:06:20	PLOT NAME = [illegible]

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TEXAS INSTRUMENTS

PROJECT TITLE:
LP-MSPM0G5187

DESIGNED FOR:
Public Release

FILE NAME:
MCU70_MSPM0G5187_PCB.PcbDoc

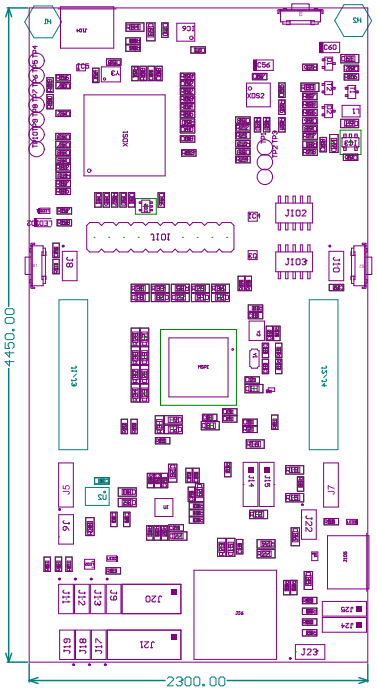
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVA REV: [illegible]	E3	BOARD #: MCU70	MCU70	SVA REV: Not in version control
LAYER NAME = [illegible]			TID #: N/A	N/A	TID #:
PLOT NAME = [illegible]			GENERATED: 2025/5/23	2025/5/23	GENERATED: 20:06:21

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ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

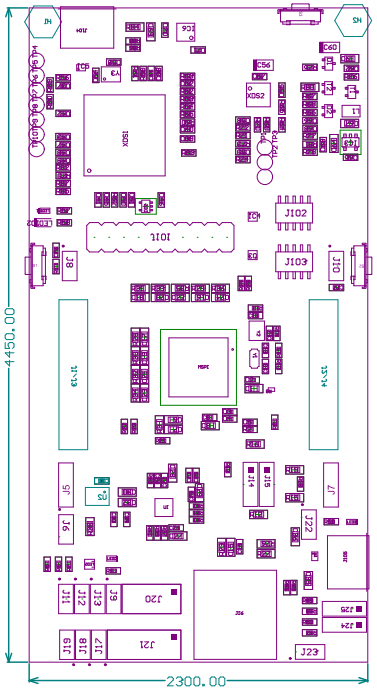
MCU70_MSPM0G5187_PCB.PcbDoc

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

ASSEMBLY VARIANT: [No Variations]

PCB NUMBER FROM BOTTOM SOLDER: SPRZ582 Rev A1	SVA REV:	E3	BOARD #: MCU70_MSPM0G5187	#: 68868	E2
LAYER NAME = M1@0.98mil,M2@8.40mil,M3@1.40mil,M4@40.00mil,M5@1.40mil,M6@8.40mil,M7@1.40mil,M8@0.98mil			TID #: N/A		
PLOT NAME = SPRZ582_TOP_SILK			GENERATED: 2025-6-23		

SVA REV: Not in version control

PCB NUMBER FROM BOTTOM SOLDER: SPRZ582 Rev A1 (No Variations)

PLOT NAME = MCU70_MSPM0G5187_TOP_SILK

TID #: N/A

GENERATED: 2025/6/23

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TEXAS INSTRUMENTS

PROJECT TITLE: LP-MSPM0G5187

DESIGNED FOR: Public Release

FILE NAME: MCU70_MSPM0G5187_PCB.PcbDoc

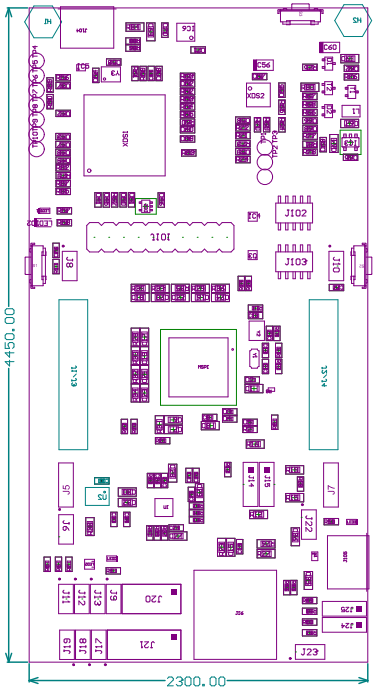
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVN REV:	E3	BOARD #: MCU70	#: 68888	E2
LAYER NAME =			TID #: N/A	TID #:	
PLOT NAME =			GENERATED: 2025/5/23	DERIVATIO: 20:06:22	PLOT NAME = Bottom

SVN REV: Not in version control

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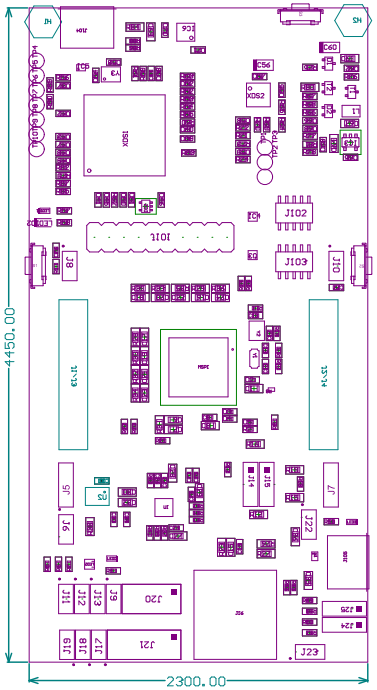
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

ZZ4 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

ZZ3 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

ENGINEER: Sal Ye

LAYOUT BY:

SCALE: 1.00

ALTIUM DESIGNER VERSION: 23.4.1.23

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

1000.00mil

PCB [illegible]	SW REV:	E3	BOARD #:	MCU70	MCU70	#: [illegible]	E2
LAYER NAME =	[illegible]		TID #:	N/A	N/A	TID #:	
PLOT NAME =	[illegible] Top		GENERATED	2025/5/23	2025/5/23	GENERATED	20:06:29

SW REV: Not in version control

PCB NAME FROM BOTTOM

ASSEMBLY VARIANT: [No Variations]

PLOT NAME = Top

GENERATED 2025/5/23 20:06:29

TEXAS INSTRUMENTS

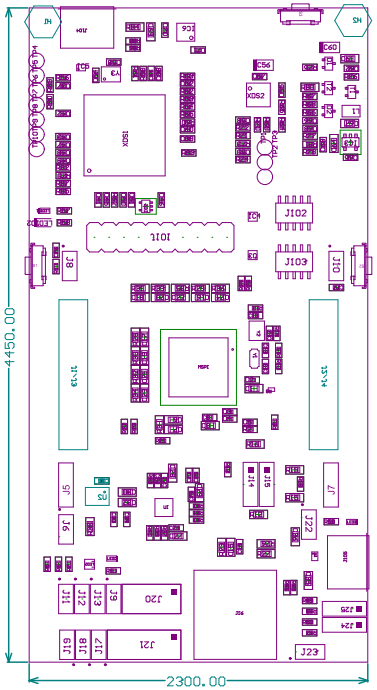
Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

1000.00mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

PCB NUMBER:	E3	BOARD #:	MCU70	#:	E2
LAYER NAME =		TID #:	N/A	TID #:	
PLOT NAME =	Bottom	GENERATED	2025/5/23	GENERATED	20:06:23

SVN REV: Not in version control

PCB NUMBER FROM BOTTOM: MCU70

PLOT NAME = Bottom

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TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

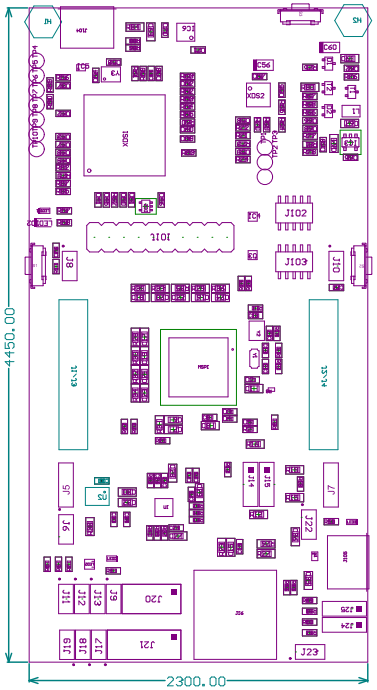
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

ZZ4 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

ZZ3 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

ENGINEER: Sal Ye

LAYOUT BY:

SCALE: 1.00

ALTIUM DESIGNER VERSION: 23.4.1.23

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

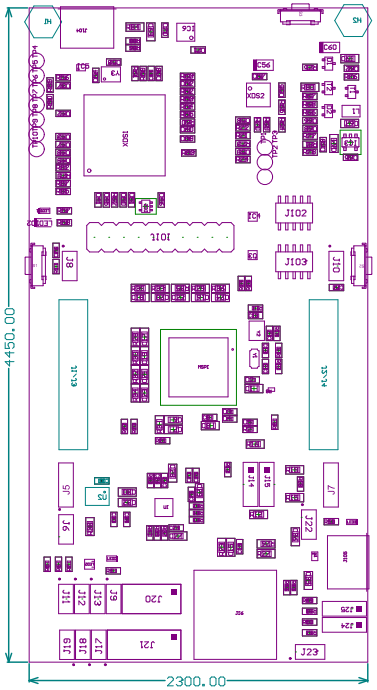
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ZZ4 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

ENGINEER: Sal Ye

LAYOUT BY:

SCALE: 1.00

ALTIUM DESIGNER VERSION: 23.4.1.23

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

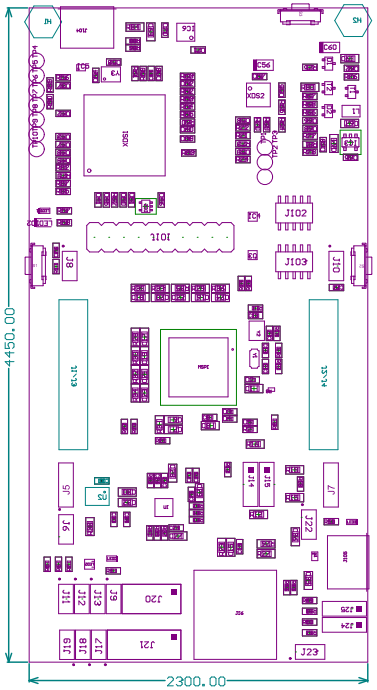
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Z24 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

1000.00mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

PCB NUMBER: [illegible]	REV: [illegible]	E3	BOARD #:	MCU70	MCU70	# REV:	E2
LAYER NAME = [illegible]			TID #:	N/A	N/A	TID #:	
PLOT NAME = [illegible]			GENERATED	2025-5-23	2025/5/23	GENERATED	20:06:25

SUN REV: Not in version control

PCB NUMBER FROM BOTTOM: [illegible]

PLOT NAME = [illegible]

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TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

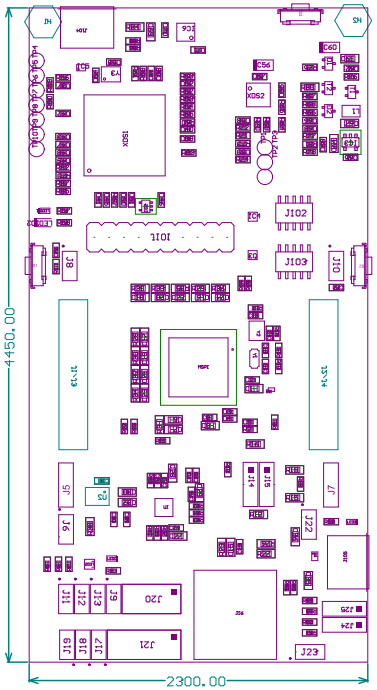
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVA REV:	E3	BOARD #: MCU70	MCU70	#: 68868
LAYER NAME =			TID #:	N/A	N/A
PLOT NAME =			GENERATED	2025/5/23	2025/5/23

E2	SVA REV:	Not in version control
TID #:		
GENERATED	2025/5/23	20:06:26
TEXAS INSTRUMENTS		PLOT NAME =

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ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

PROJECT TITLE:
LP-MSPM0G5187

DESIGNED FOR:
Public Release

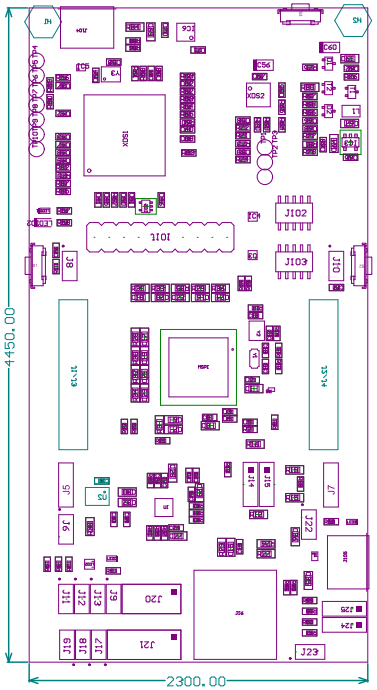
FILE NAME:
MCU70_MSPM0G5187_PCB.PcbDoc

Z24 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVA REV:	E3	BOARD #: MCU70	MCU70	#: [illegible]
LAYER NAME =	[illegible]		TID #: N/A	N/A	TID #:
PLOT NAME =	[illegible] Top		GENERATED	2025/5/23	GENERATED

E2	SVA REV:	Not in version control	PCB NAME FROM BOTTOM
20[illegible]28	PLOT NAME =	[illegible] Top	© TEXAS INSTRUMENTS

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ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

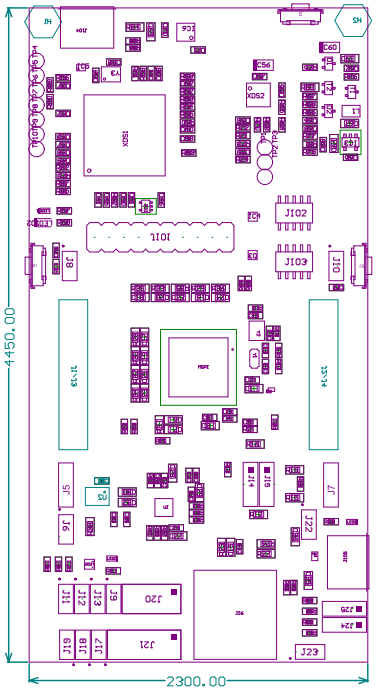
MCU70_MSPM0G5187_PCB.PcbDoc

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

1000.00mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

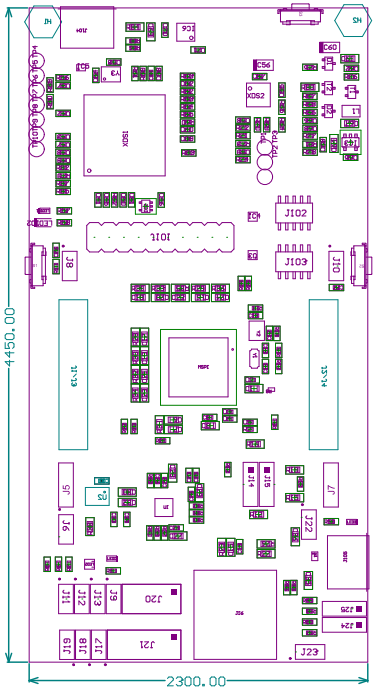
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Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION			
MIN. TRACK WIDTH:	8	MIL	
MIN. CLEARANCE:	0.2	mm	
MIN. VIA PAD SIZE:	24	MIL	
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/-	5 MIL HOLES	+/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):			+/- 3 MIL

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING: REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: LP-MSPM0G5187

DESIGNED FOR: Public Release

FILE NAME: MCU70_MSPM0G5187_PCB.PcbDoc

PCB [illegible]	E3	BOARD #: MCU70	#: E2
LAYER NAME =		TID #: N/A	
PLOT NAME =		GENERATED 2025/5/23	

SVN REV: Not in version control

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

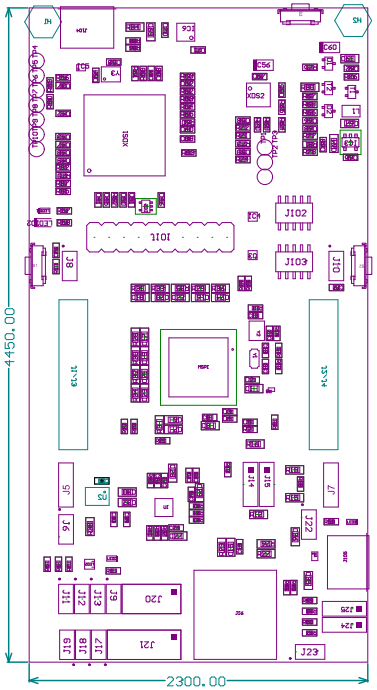
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

ZZ4 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

ZZ3 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

1000.00mil

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

PCB [illegible]	E3	BOARD #: MCU70	#: E2
LAYER NAME = [illegible]		TID #: N/A	TID #:
PLOT NAME = [illegible]		GENERATED 2025/5/23	GENERATED 20:06:28

SVN REV: Not in version control

PCB NEMKO FROM BOTTOM

PLOT NAME = [illegible] Bottom

TEXAS INSTRUMENTS

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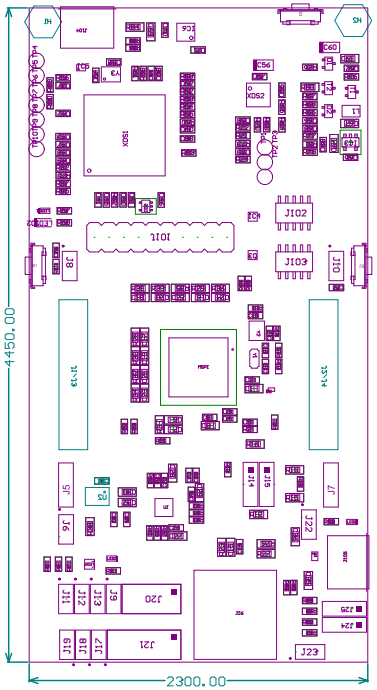
ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVA REV:	E3	BOARD #:	MCU570	#: [illegible]
LAYER NAME =	[illegible]		TID #:	N/A	TID #:
PLOT NAME =	[illegible]		GENERATED	2025/5/23	GENERATED

PCB VIEWED FROM BOTTOM	[illegible]	E2	SVA REV:	Not in version control	SVA REV:
PLOT NAME =	[illegible]		GENERATED	2025-5-23	GENERATED

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TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

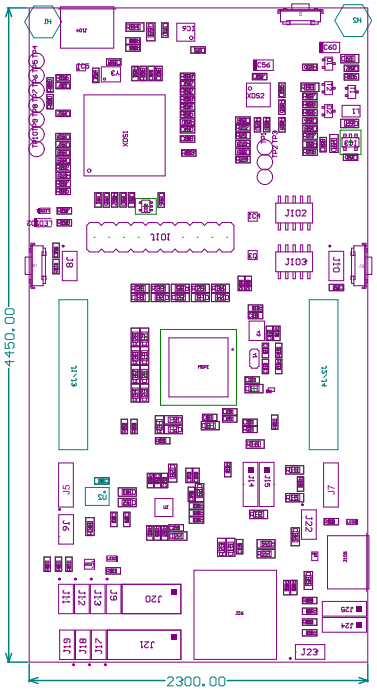
ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER



COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVA REV:	E3	BOARD #:	MCU570	MCU570
LAYER NAME =	[illegible]		TID #:	N/A	N/A
PLOT NAME =	[illegible] Assembly		GENERATED	2025/5/23	2025/5/23

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TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

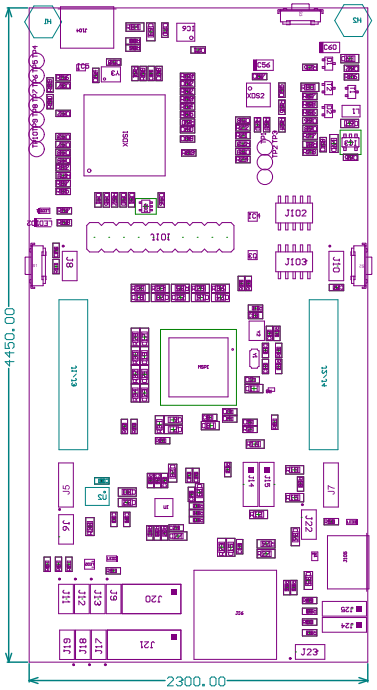
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

ENGINEER:

Sal Ye

LAYOUT BY:

Sal Ye

SCALE: 1.00

ALTIUM DESIGNER VERSION:

23.4.1.23

1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SW REV:	E3	BOARD #:	MCU70	MCU70	#: [illegible]	E2
LAYER NAME =			TID #:	N/A	N/A	TID #:	
PLOT NAME =	[illegible] Keepout		GENERATED	2025/5/23	GENERATED	20:06:30	

SUW REV: Not in version control

PCB NAME = [illegible]

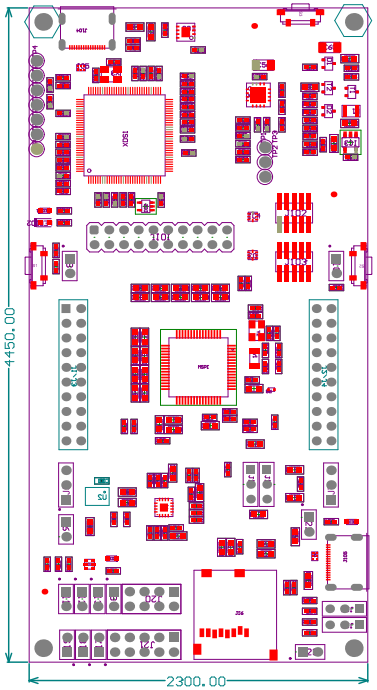
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Z24 ■ Place a click-in Standoff (MAE-IO, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

PCB [illegible]	SVN REV:	E3	BOARD #:	MCU70	MCU70	#: [illegible]	E2
LAYER NAME =	[illegible]		TID #:	N/A	N/A	TID #:	
PLOT NAME =	[illegible]		GENERATED	2025/5/23	[illegible]	2025/5/23	GENERATED

PCB [illegible]	SVN REV:	E3	BOARD #:	MCU70	MCU70	#: [illegible]	E2
LAYER NAME =	[illegible]		TID #:	N/A	N/A	TID #:	
PLOT NAME =	[illegible]		GENERATED	2025/5/23	[illegible]	2025/5/23	GENERATED

PCB [illegible] SVN REV: Not in version control

PLOT NAME = [illegible] TEXAS INSTRUMENTS

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DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

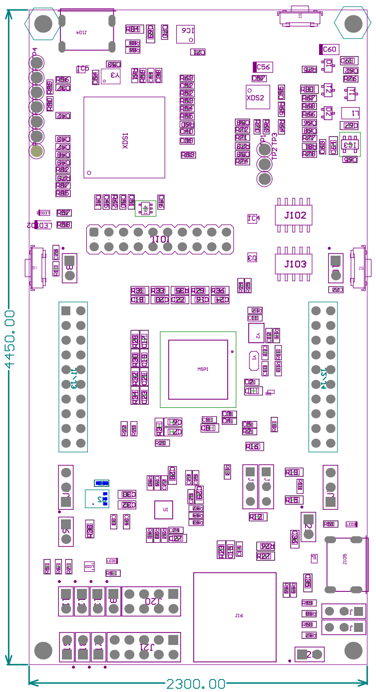
ENGINEER: Sal Ye	LAYOUT BY: Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

ZZ4 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

ZZ3 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-004	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-004	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: LP-MSPM0G5187

DESIGNED FOR: Public Release

FILE NAME: MCU170_MSPM0G5187_PCB.PcbDoc

PCB VIEWED FROM TOP SIDE	SVN REV: Not in version control	E2	BOARD #:	MCU170	REV #:	E2	SVN REV: Not in version control / PCB VIEWED FROM BOTTOM SIDE
LAYER NAME =	Bottom		TID #:	N/A			
PLOT NAME =	Bottom Pad Master	20:06:32	GENERATED	2025/5/23		20:06:32	TEXAS INSTRUMENTS / PLOT NAME = Bottom Pad Master

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ENGINEER: Sal Ye

LAYOUT BY: Sal Ye

SCALE: 1.00

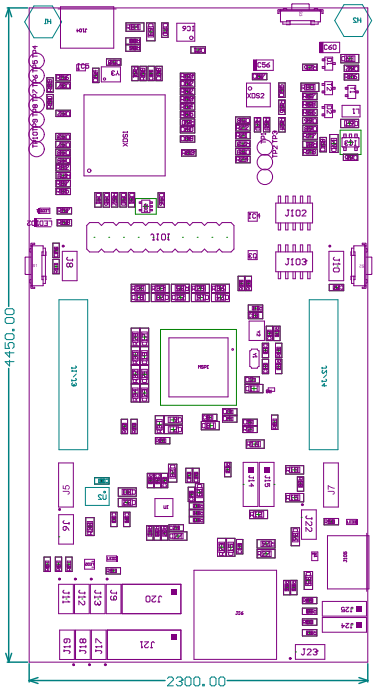
ALTIUM DESIGNER VERSION: 23.4.1.23

ZZ4 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

ZZ3 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

ZZ2 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL

MIN. CLEARANCE: 0.2 mm

MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL

PER IPC-D-275 CLASS 2 LEVEL C

REGISTRATION TOLERANCES: METAL +/- 5 MIL HOLES +/- 3 MIL

HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

[ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2

[ ] OTHER +/-

DRILLING:

REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:

SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:

LP-MSPM0G5187

DESIGNED FOR:

Public Release

FILE NAME:

MCU70_MSPM0G5187_PCB.PcbDoc

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

1000.00mil

PCB [illegible]	SVA REV: Not in ver	E3	BOARD #: MCU70	#: [illegible]	E2
LAYER NAME = [illegible]			TID #: N/A	TID #: N/A	
PLOT NAME = [illegible]			GENERATED 2025/5/23	GENERATED 20:06:39	PLOT NAME = [illegible]

SVA REV: Not in version control

PCB NEMKO FROM BOTTOM

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ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

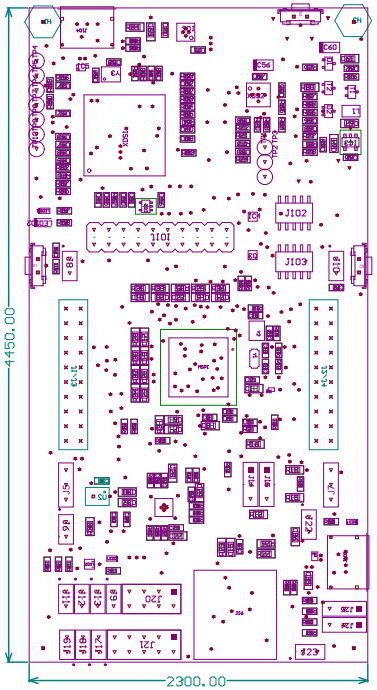
Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance	Hole Length
⊠	6	35.43mil (0.900mm)	NPTH	Round	Top Layer - Bottom Layer		-
⊠	4	125.00mil (3.175mm)	NPTH	Round	Top Layer - Bottom Layer		-
⊕	19	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer		-
⊕	290	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer		-
▼	8	20.00mil (0.508mm)	PTH	Round	Top Layer - Bottom Layer		-
○	1	39.37mil (1.000mm)	PTH	Round	Top Layer - Bottom Layer		-
▽	90	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer		-
⊠	40	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer		-
⊙	4	55.12mil (1.400mm)	PTH	Slot	Top Layer - Bottom Layer		23.62mil (0.600mm)
□	4	59.06mil (1.500mm)	PTH	Slot	Top Layer - Bottom Layer		23.62mil (0.600mm)
	460 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION			
MIN. TRACK WIDTH:	8	MIL	
MIN. CLEARANCE:	0.2	mm	
MIN. VIA PAD SIZE:	24	MIL	
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/-	5 MIL HOLES +/-	3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):			+/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-VO REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE:
LP-MSPM0G5187

DESIGNED FOR:
Public Release

FILE NAME:
MCU70_MSPM0G5187_PCB.PcbDoc

PCB [illegible]	SVN REV: Not in version control
LAYER NAME = [illegible]	TID #: N/A
PLOT NAME = [illegible] Drawing For (Top Layer - Bottom Layer)	GENERATED: 2025/5/23 20:06:39

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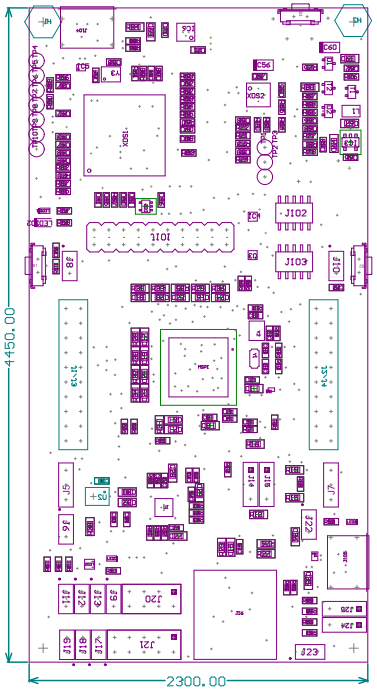
ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23

Z24 ■ Place a click-in Standoff (MAE-10, KangYang) in hole MH1/MH2

Z23 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Z22 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	0.98mil	4	
1	Top Layer		1.40mil		
	Dielectric 2	FR-4	8.40mil	4.2	
2	VCC Layer		1.40mil		
	Dielectric1	FR-4	40.00mil	4.2	
3	GND Layer		1.40mil		
	Dielectric 3	FR-4	8.40mil	4.2	
4	Bottom Layer		1.40mil		
	Bottom Solder	SM-001	0.98mil	4	
	Bottom Overlay				



1000.00mil

COMPONENTS MARKED "DNP" SHOULD NOT BE POPULATED.

ASSEMBLY VARIANT: [No Variations]

DESIGN INFORMATION			
MIN. TRACK WIDTH:	8	MIL	
MIN. CLEARANCE:	0.2	mm	
MIN. VIA PAD SIZE:	24	MIL	
MINIMUM ANNULAR RING	0.05mm (2MIL)	EXTERNAL	
PER	IPC-D-275 CLASS 2 LEVEL C		
REGISTRATION TOLERANCES:	METAL +/-	5 MIL HOLES	+/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED):			+/- 3 MIL

MATERIAL: [ ] FR-408 [X] FR-4 High Tg [ ] OTHER

THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER

TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2 [ ] OTHER +/-

DRILLING: REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES

PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH: SILKSCREEN: [X] TOP [X] BOTTOM

SILKSCREEN COLOR: [X] WHITE [ ] OTHER

SOLDER RESIST COLOR: [ ] GREEN [X] OTHER Red

[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG

[X] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE

[ ] N.C. ROUTE [X] V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:

[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3

[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.

PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: [ ] YES

BARE BOARD ELEC. TEST: [ ] NONE [ ] REQUIRED [X] PER ORDER

TEXAS INSTRUMENTS

PROJECT TITLE: LP-MSPM0G5187

DESIGNED FOR: Public Release

FILE NAME: MCU70_MSPM0G5187_PCB.PcbDoc

PCB [illegible]	E3	BOARD #: MCU70	#: [illegible] E2 SVN REV: Not in version control
LAYER NAME =		TID #: N/A	TID #:
PLOT NAME = [illegible]		GENERATED 2025/5/23	[illegible] 20:06:35

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ENGINEER:	LAYOUT BY:
Sal Ye	Sal Ye
SCALE: 1.00	ALTIUM DESIGNER VERSION: 23.4.1.23