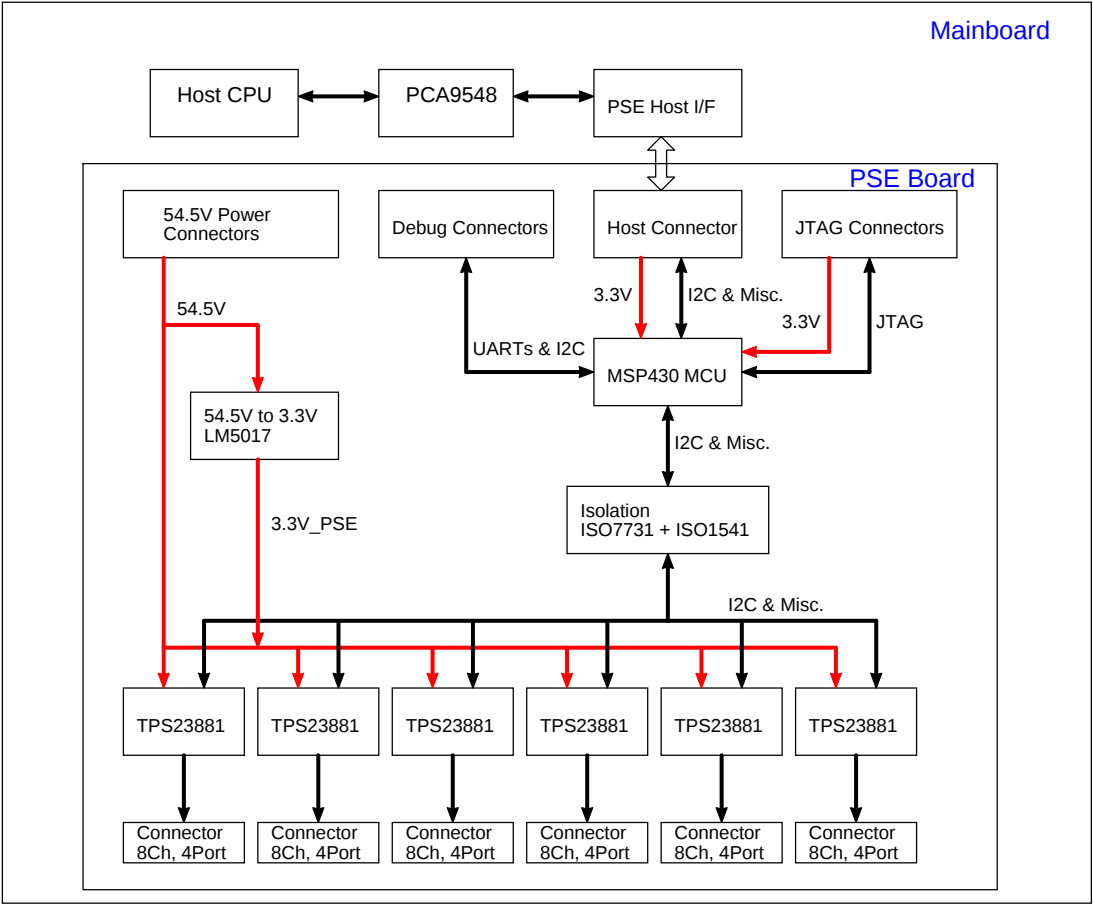
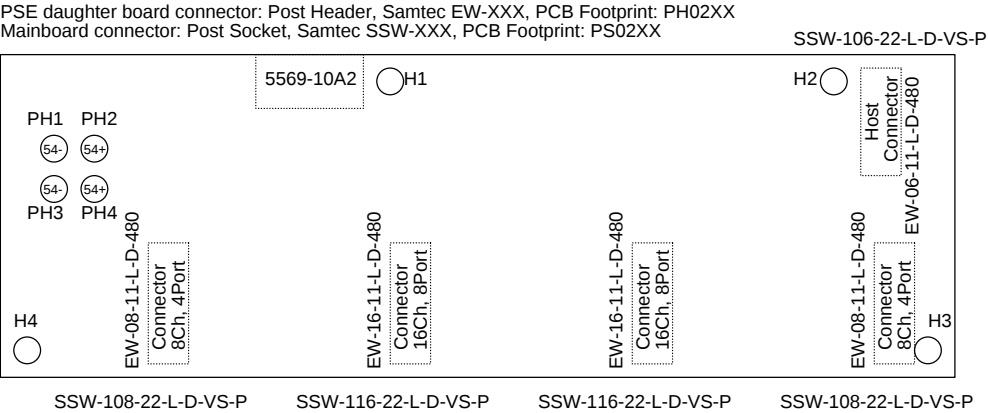


Architecture



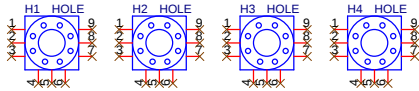
Mechanical Parts



SMT Mark



Mechanical Hole



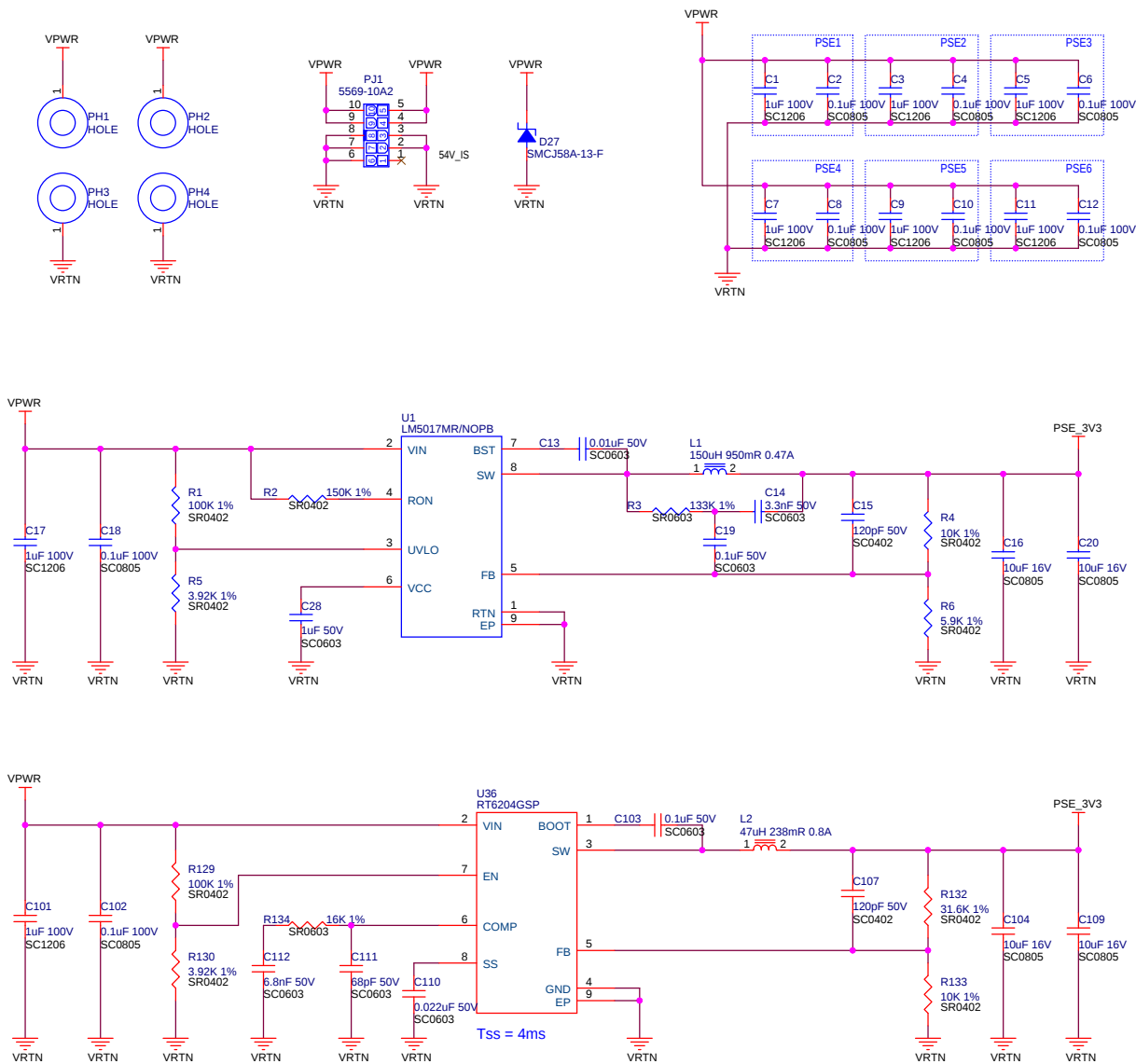
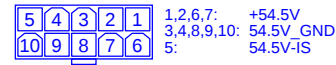
		Project Name : <Project Name>		
		Page Name : 02 Mechanical Parts		
Size :	Document Number :	Design By :	Review By :	Rev :
A3	<Doc>	<Name>	<Name>	V1.0
Date : Thursday, May 27, 2021			Sheet 2 of 10	

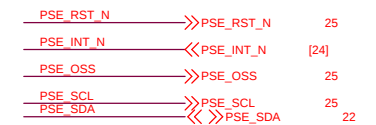
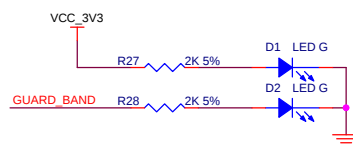
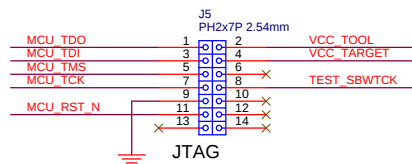
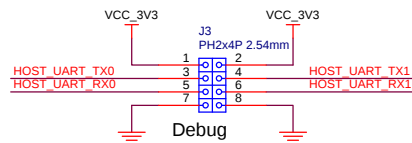
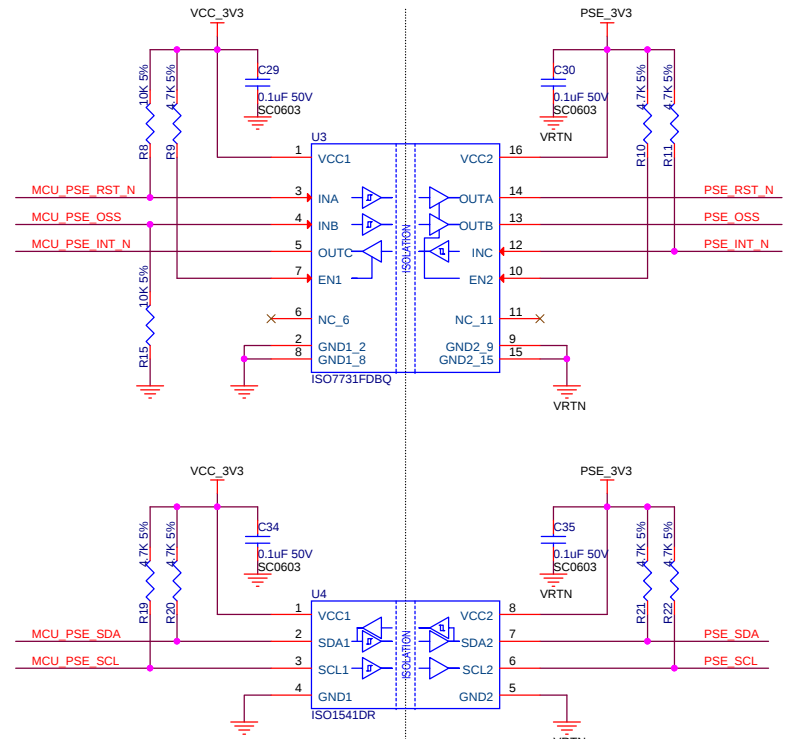
Design Schematic & PCB according to Molex 5569-08A2/5569-10A2

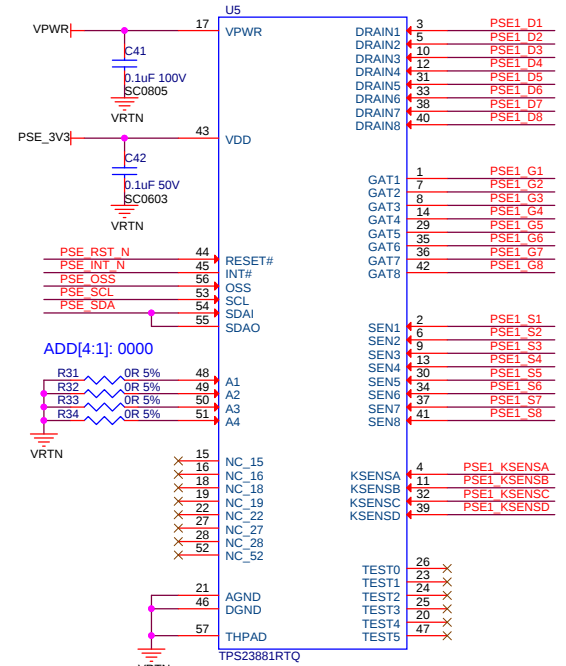
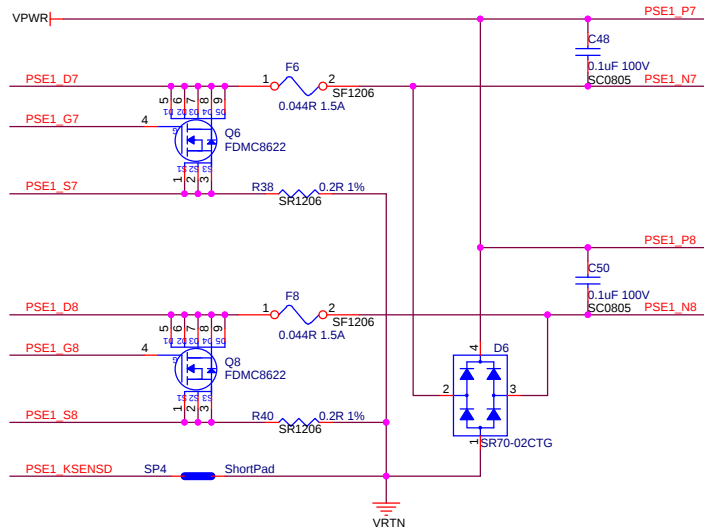
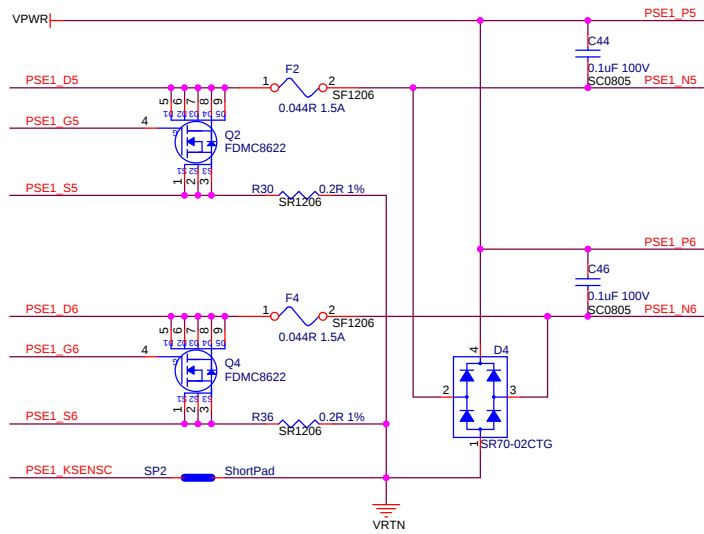
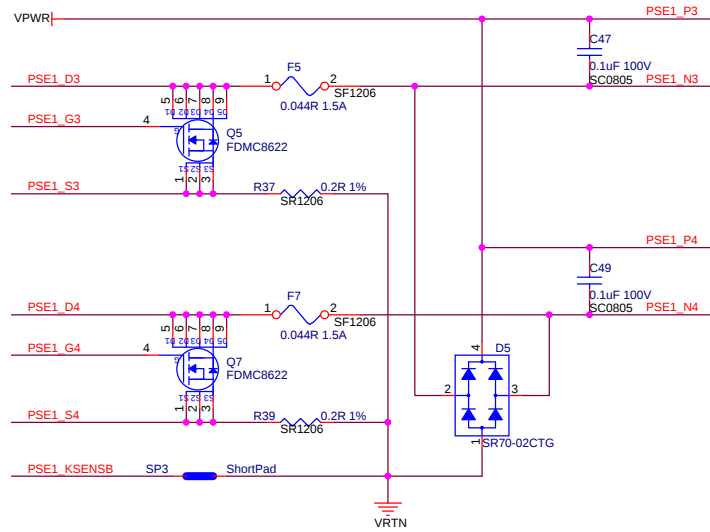
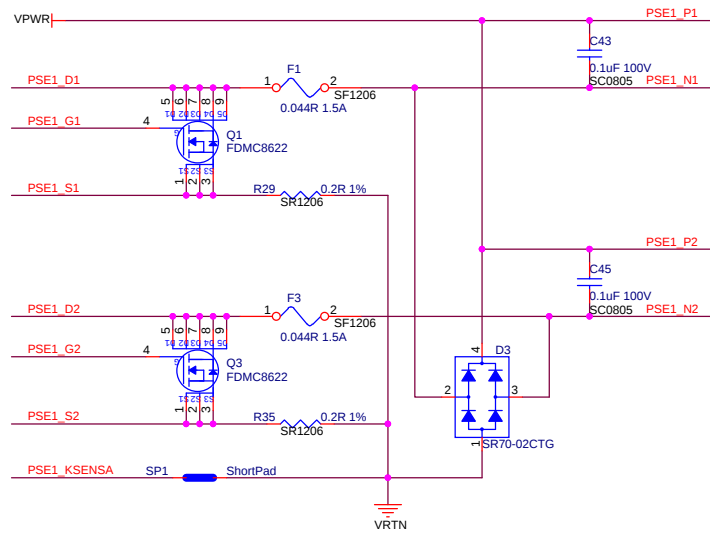
Molex 5569-10A2



Gospower G1324-950W definition

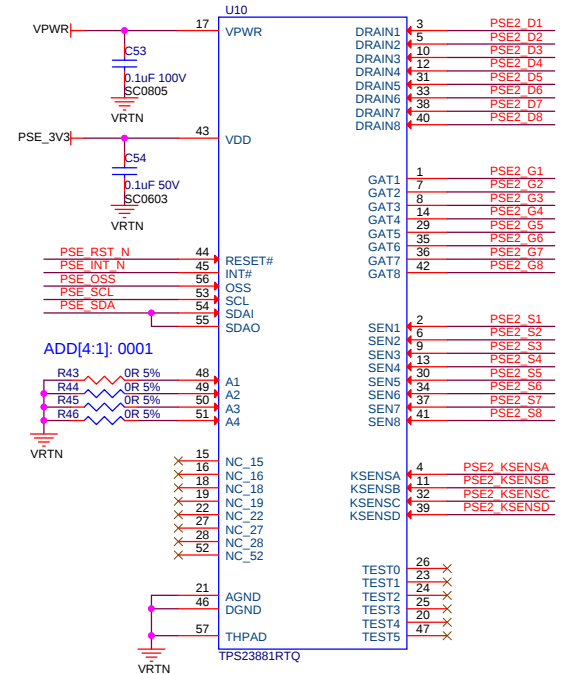
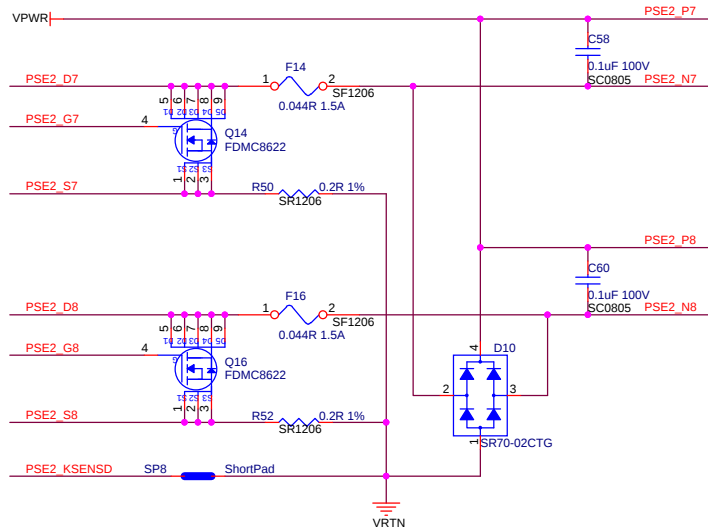
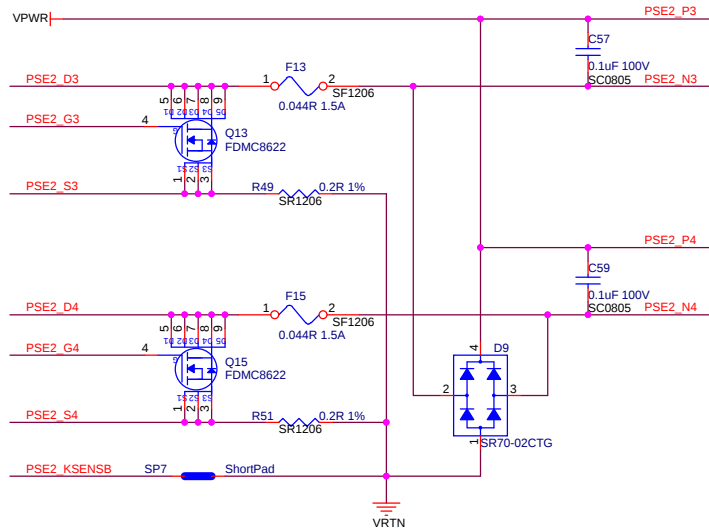
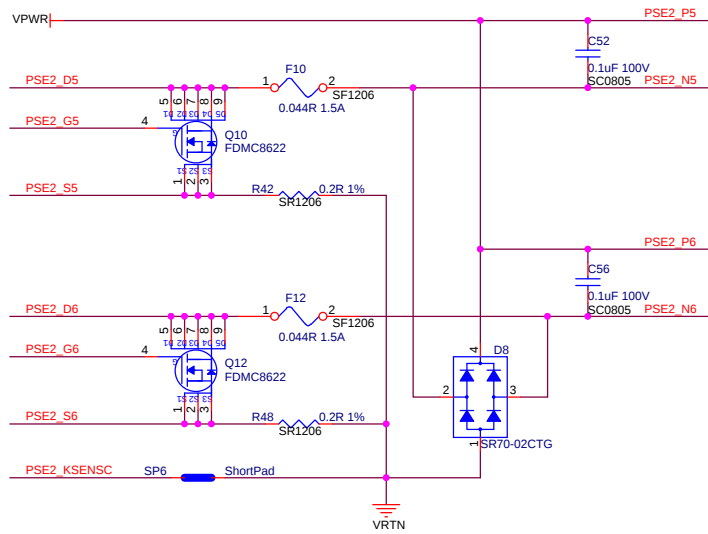
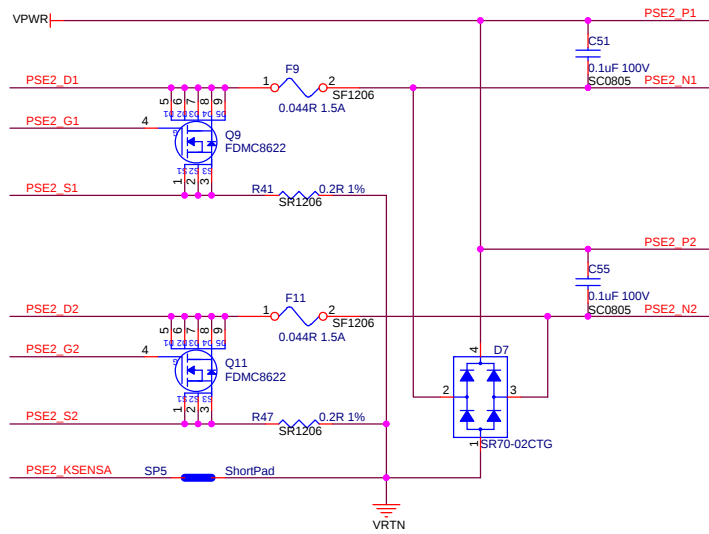






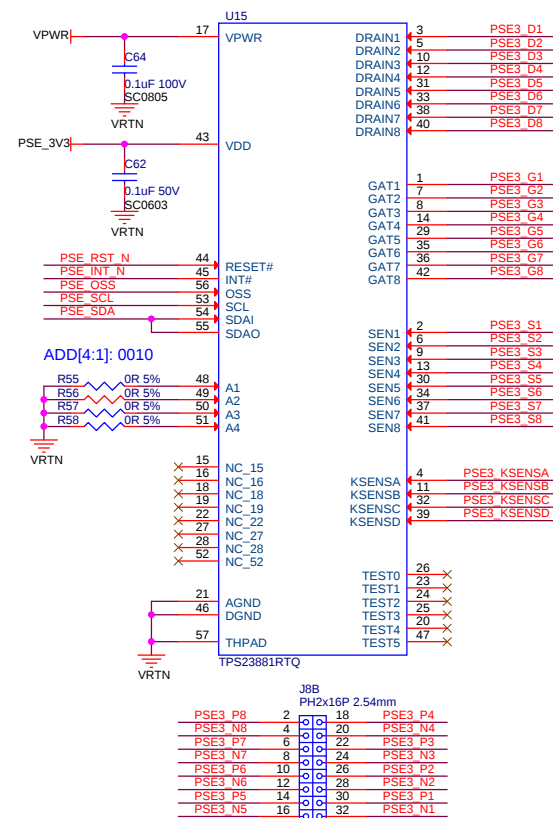
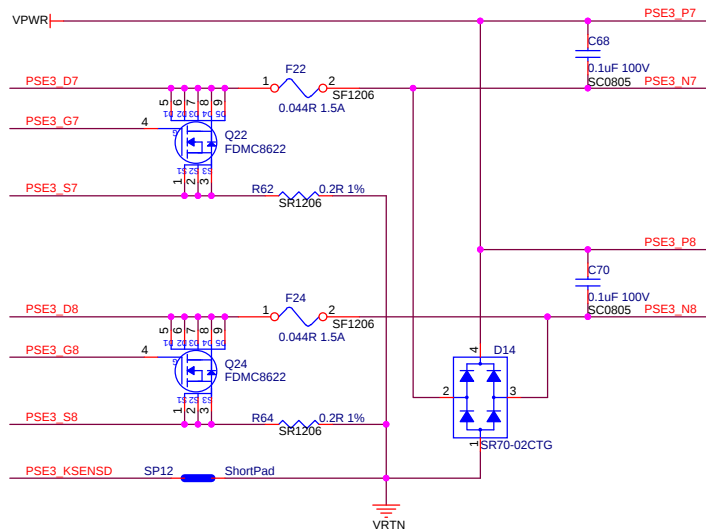
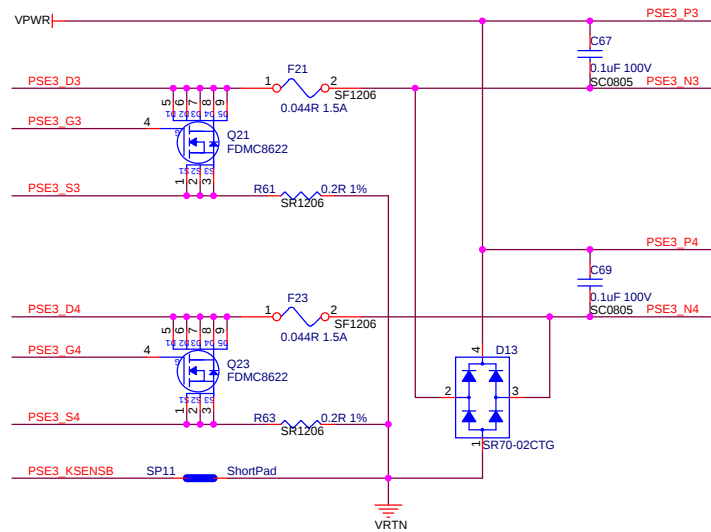
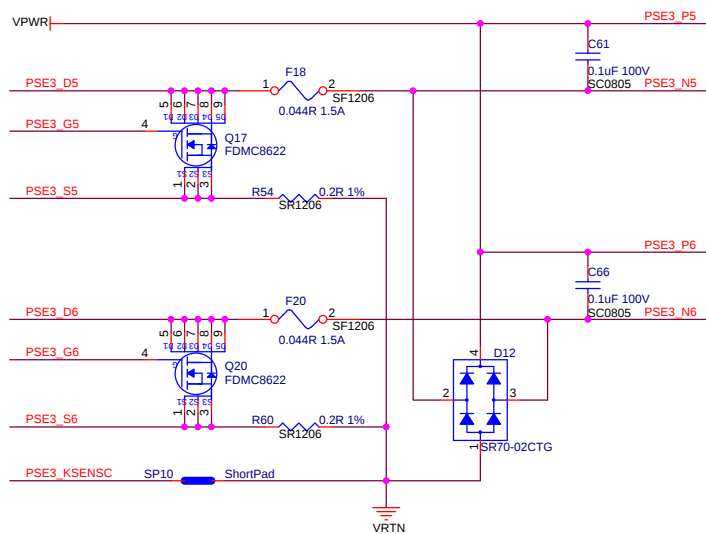
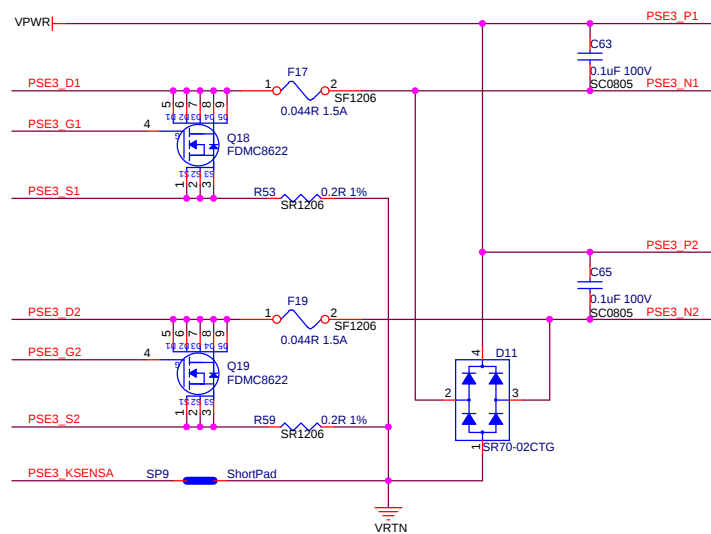
J7 PH2x8P 2.54mm	
PSE1_P1	1
PSE1_N1	2
PSE1_P2	3
PSE1_N2	4
PSE1_P3	5
PSE1_N3	6
PSE1_P4	7
PSE1_N4	8
PSE1_P5	9
PSE1_N5	10
PSE1_P6	11
PSE1_N6	12
PSE1_P7	13
PSE1_N7	14
PSE1_P8	15
PSE1_N8	16

PSE_RST_N	<<PSE_RST_N	[24]
PSE_INT_N	>>PSE_INT_N	25
PSE_OSS	<<PSE_OSS	[24]
PSE_SCL	<<PSE_SCL	[24]
PSE_SDA	>>PSE_SDA	22

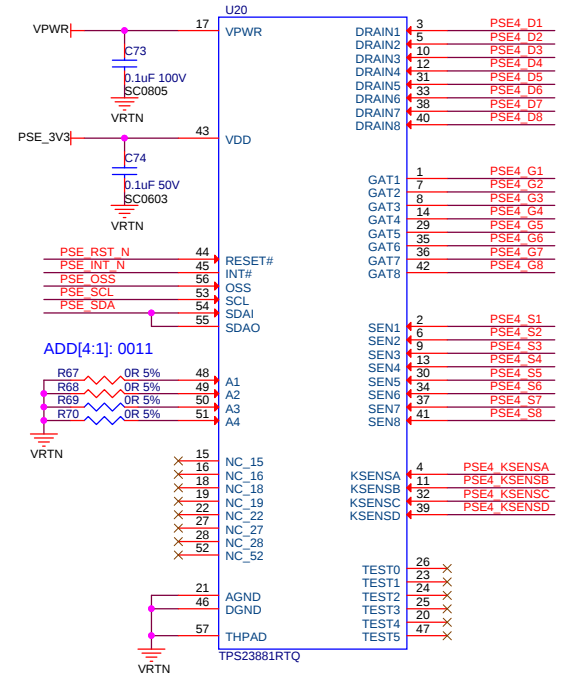
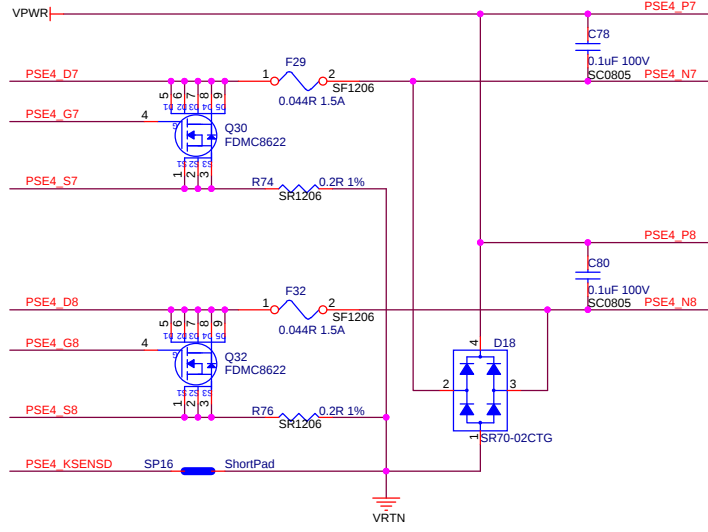
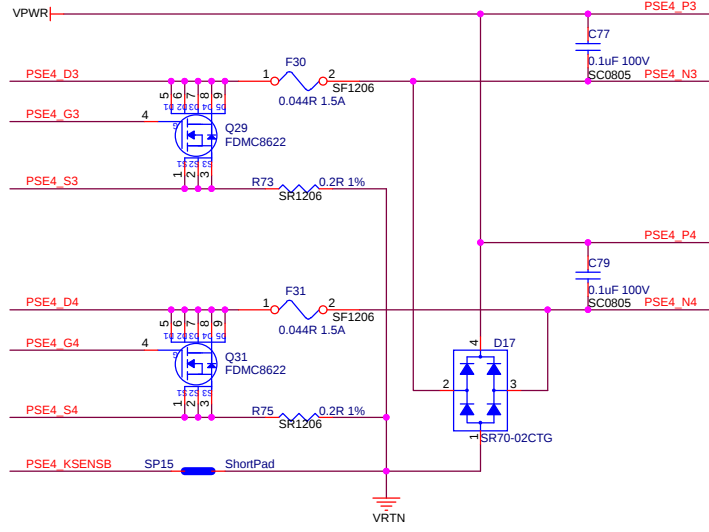
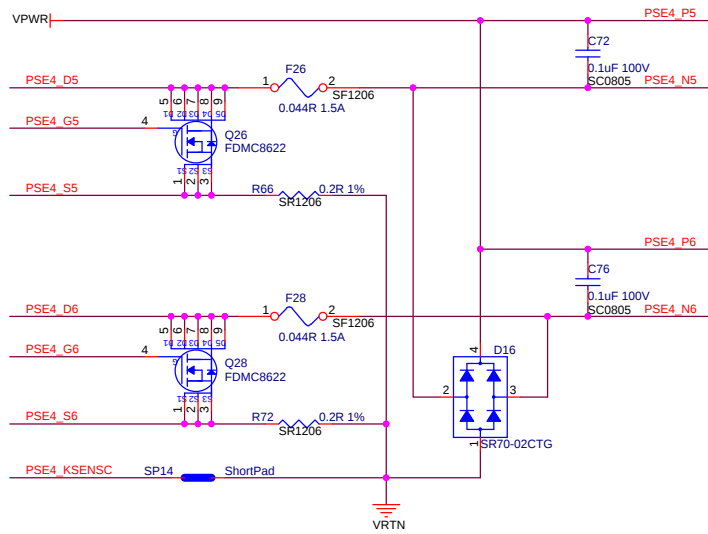
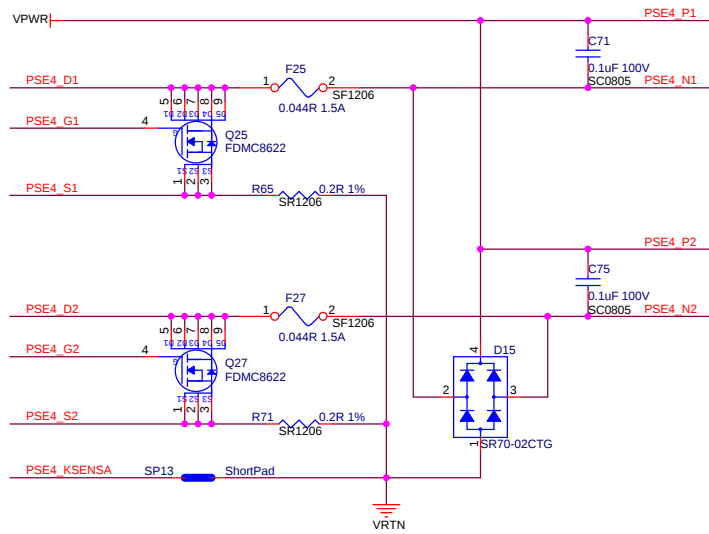


J8A		PH2x16P 2.54mm	
PSE2_P1	1	17	PSE2_P5
PSE2_N1	3	19	PSE2_N5
PSE2_P2	5	21	PSE2_P6
PSE2_N2	7	23	PSE2_N6
PSE2_P3	9	25	PSE2_P7
PSE2_N3	11	27	PSE2_N7
PSE2_P4	13	29	PSE2_P8
PSE2_N4	15	31	PSE2_N8

PSE_RST_N	<<PSE_RST_N	[24]
PSE_INT_N	>>PSE_INT_N	25
PSE_OSS	<<PSE_OSS	[24]
PSE_SCL	<<PSE_SCL	[24]
PSE_SDA	>>PSE_SDA	22

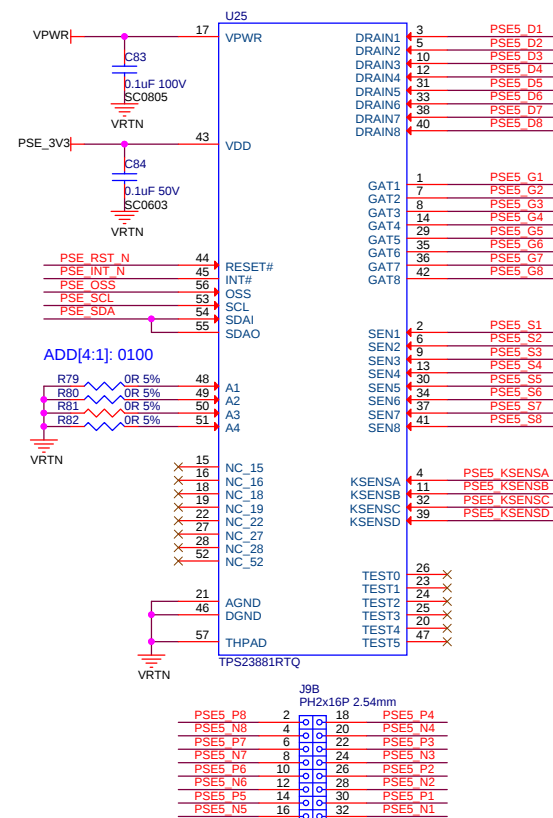
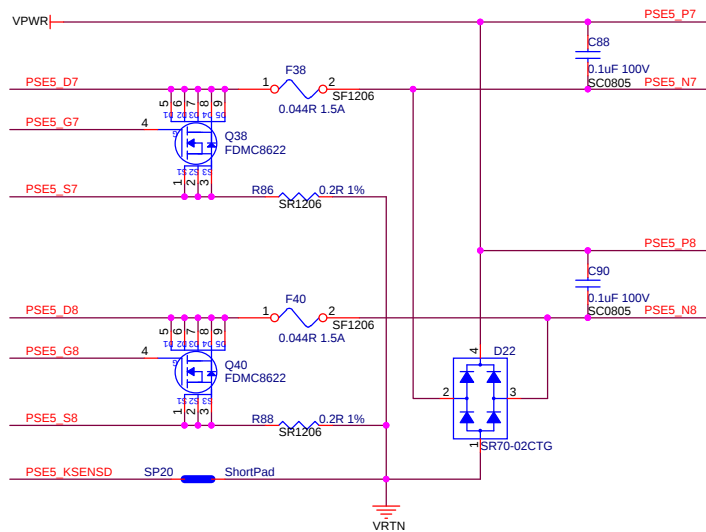
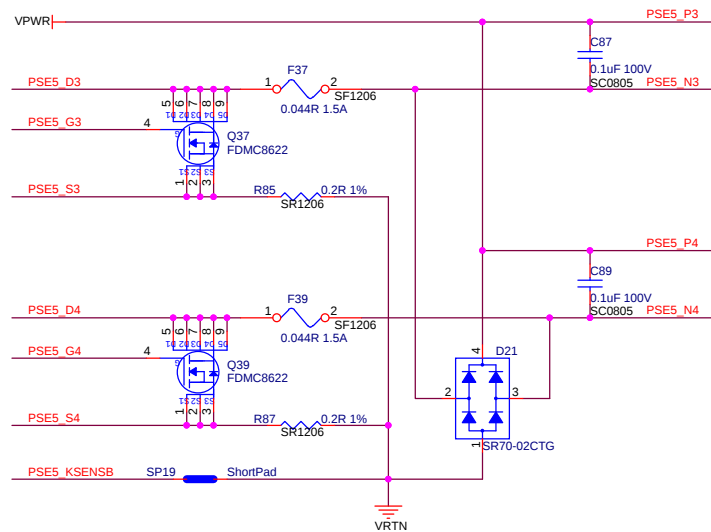
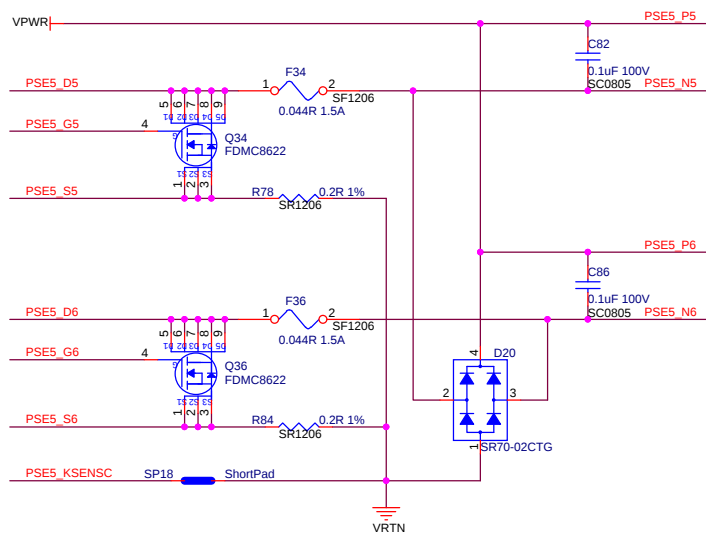
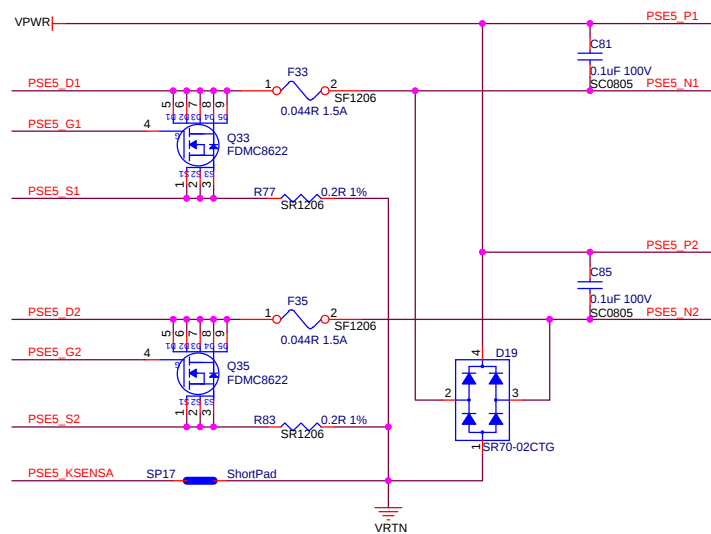


PSE_RST_N	↔	PSE_RST_N	[24]
PSE_INT_N	↔	PSE_INT_N	25
PSE_OSS	↔	PSE_OSS	[24]
PSE_SCL	↔	PSE_SCL	[24]
PSE_SDA	↔	PSE_SDA	22

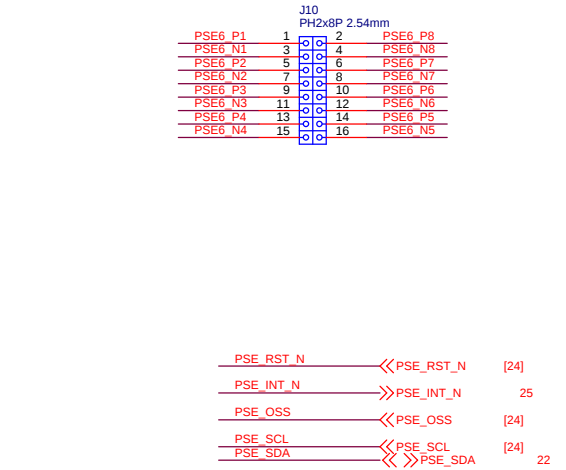
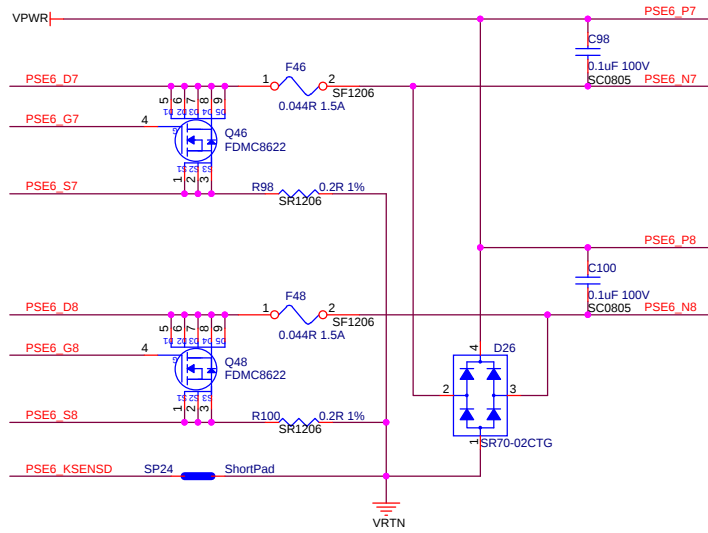
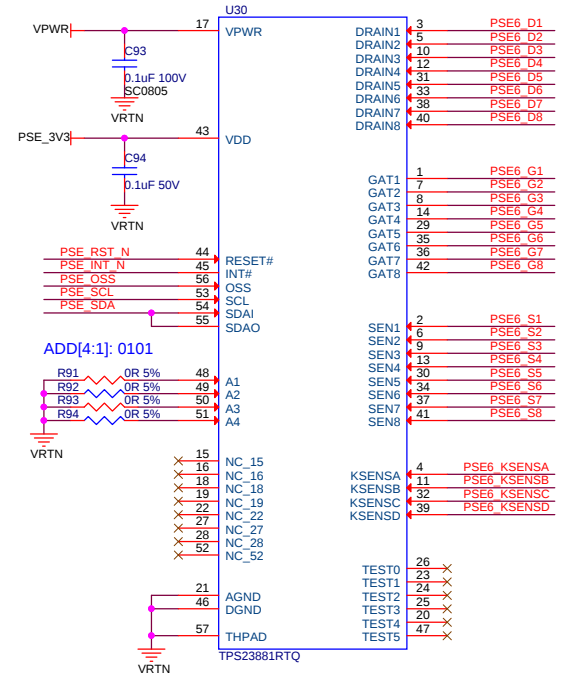
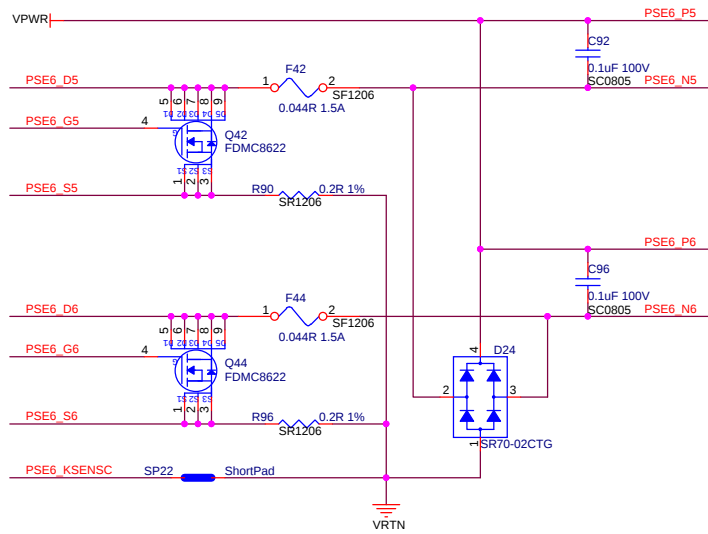
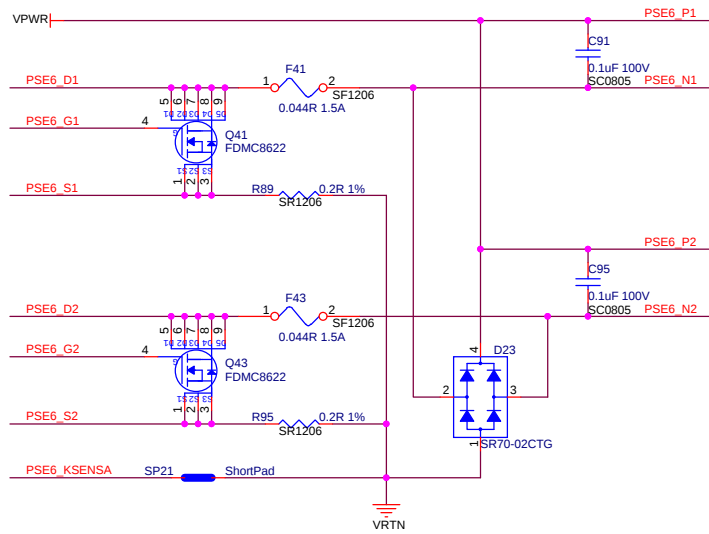


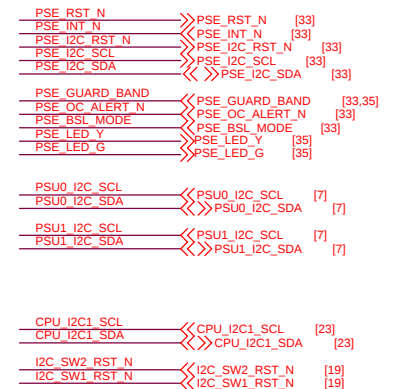
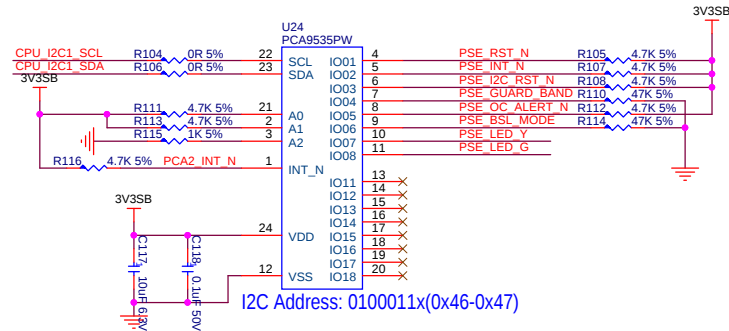
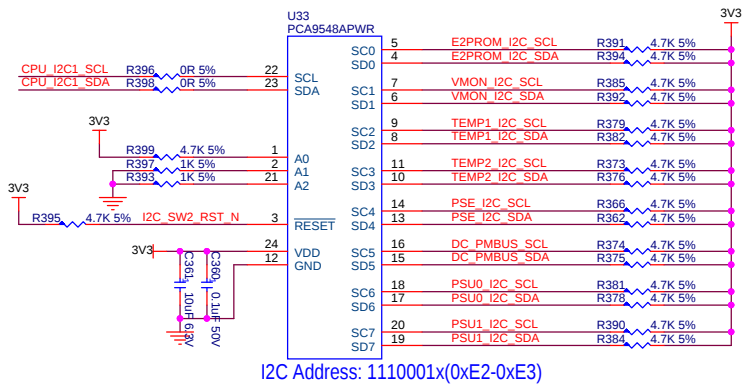
J9A		PH2x16P 2.54mm	
PSE4_P1	1	17	PSE4_P5
PSE4_N1	3	19	PSE4_N5
PSE4_P2	5	21	PSE4_P6
PSE4_N2	7	23	PSE4_N6
PSE4_P3	9	25	PSE4_P7
PSE4_N3	11	27	PSE4_N7
PSE4_P4	13	29	PSE4_P8
PSE4_N4	15	31	PSE4_N8

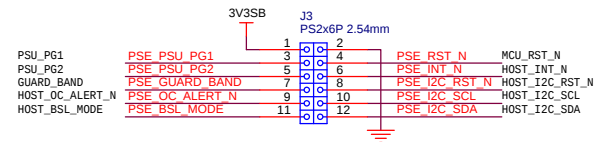
PSE_RST_N	<<<PSE_RST_N	[24]
PSE_INT_N	>>>PSE_INT_N	25
PSE_OSS	<<<PSE_OSS	[24]
PSE_SCL	<<<PSE_SCL	[24]
PSE_SDA	>>>PSE_SDA	22



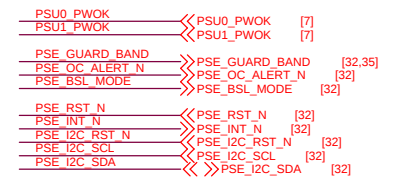
PSE_RST_N	↔	PSE_RST_N	[24]
PSE_INT_N	↔	PSE_INT_N	25
PSE_OSS	↔	PSE_OSS	[24]
PSE_SCL	↔	PSE_SCL	[24]
PSE_SDA	↔	PSE_SDA	22







The PSU2 is installed in single PSU mode.
Therefore, connect PSU1_PWOK to PSE_PSU_PG1, while PSU0_PWOK to PSE_PSU_PG2



		Project Name : <Project Name>	
		Page Name : 33 PSE Host Interface	
Size :	Document Number :	Design By :	Review By :
A3	<Doc>	<Name>	<Name>
Date :	Tuesday, February 22, 2022	Sheet	33 of 51