TEXAS
INSTRUMENTS

TSS721 M-Bus Transceiver

Application Report

1994

Linear Mixed-Signal

TSS721 M-Bus Transceiver

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1. INTRODUCTION

One of the major requirements for the realization of a cost efficient Bus concept is to reduce the number of electrial parts and costs for the module interface, because the module interfaces are high volume products. The major objective in the development of the TSS721 therefore was the integration of all necessary functions in one chip with only a few external parts needed.

2. DESCRIPTION

2.1. Structure and function

The most important features of the TSS721 are:

- receiver logic according to the M-Bus specification with dynamic level recognition
- adjustable constant current sink via resistor (typical 20 mA according to the standards DIN 66258 and DIN 66348)
- polarity independent
- power-fail function
- module supply voltage switch
- remote powering

The circuit design with the TSS721 depends on which supply mode is needed (see section 2.2). In Figure 1 you can see the block diagram of the TSS721 with the external parts for the remote supply operating mode.

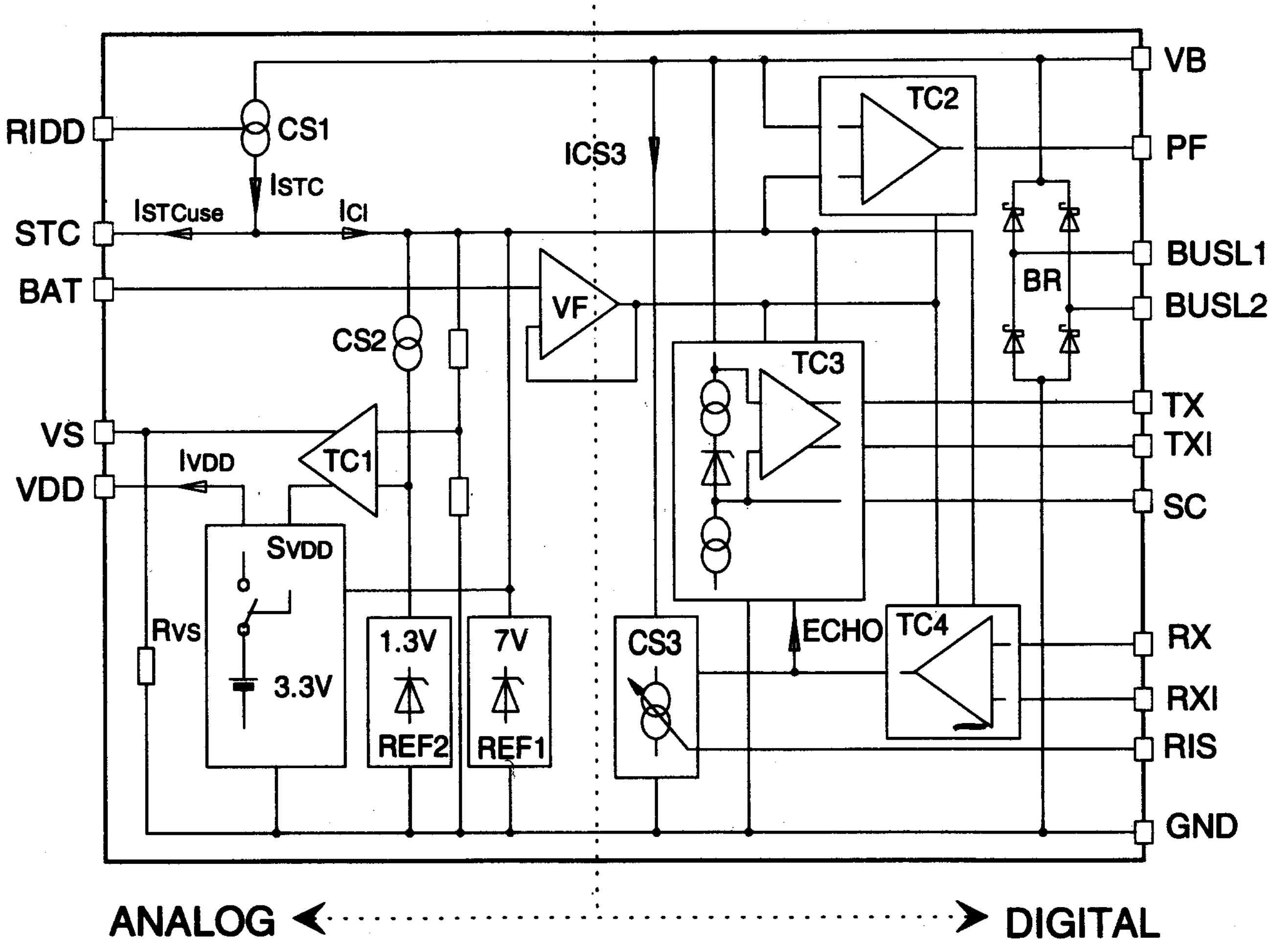


Figure 1. Block diagram of TSS721

2.1.1. Analog functions

Rectifier bridge BR:
The Bus lines are connected to the pins BUSL1 and BUSL2. Between the Bus lines and the pins should be positioned two protection resistors (see section 2.3). The Bus voltage is rectified by the integrated rectifier bridge which makes the device independent of polarization. The rectified Bus voltage is then available between the pins GND and VB, where in most cases GND is also the system ground. If you don't want to use the rectifier bridge of the TSS721 input, you may also connect the Bus lines between the pins VB and GND. This causes a disadvantage, in that the device is then not independent of polarization, which is the basis for an easy to install Bus system. You should use this wiring only if the Bus voltage is very low and you can't afford the voltage drop on the Schottky rectifier diodes.

$U_{VB} = |U_{BUSL1} - U_{BUSL2}| - U_{BR}$

Constant current source CS1:
The Bus voltage available on the pins VB and GND supplies several constant current sources. These constant current sources are the power supply for the entire TSS721 and also partly for the module. This concept that the whole power supply is taken out of constant current sources is required by the M-Bus, which demands that the quiescent current of the Bus is always constant. Without this principle, the current variations of each module would be added together and cause transmission errors.

The constant current source CS1 supplies the current for almost the entire device and also partially for the module, depending on which supply mode is used. The value of this constant current I_{STC} can be programmed by an external resistor and varies typically between 400 µA to 960 µA. It is fixed by the reference voltage on pin RIDD and the resistor connected to this pin. The current can be calculated with the following formula:

$$I_{STC} = \frac{V_{RIDD}}{R_{IDD}} \qquad (1)$$

here:
I_{STC} = constant current of CS1 in Amperes
V_{RIDD} = reference voltage on pin RIDD (typically 1.26 V)
R_{IDD} = 13 kΩ to 80 kΩ

The constant current I_{STC} splits up into the current for the device supply and the charge current for a support capacitor. This support capacitor provides the module current at current peaks or when the Bus voltage fails.

$$I_{STC} = I_{STC\_use} + I_{CI} \qquad (2)$$

here:
I_{STC_use} = load current for the support capacitor
I_{CI} = supply current for the TSS721

The maximum resistance on RIDD (minimum current) depends on the current needed for the internal chip supply and the required load current for the support capacitor.

The minimum resistance (maximum current) is determined by CS1 which is able to supply a minimum current of 1 mA. This current of 1 mA is also enough to isolate the TSS721 interface chip via the optocoupler from the M-Bus. Opto-couplers with a good current transfer ratio, require driver currents of only 300 µA to 500 µA.

'Wakeup' time:

When the Bus voltage of the M-Bus is switched on and the TSS721 is powered, a certain time is needed to charge the support capactior. Because the load current is limited, it could, in some cases, require up to a minute before the TSS721 becomes functional. The load time of the support capacitor depends on its value, its format current and its leakage current. The loadtime can be calculated with the following formula:

$$t_{LOAD} = \frac{C_{STC} * V_{VDDon}}{I_{STC\_use} - I_{FOR} - I_{LC}} \qquad -(3)$$

here:
C_{STC} = value of the support capacitor
V_{VDDon} = support-capacitor voltage level at which VDD is switched on and VS switched off (typically 6.0 V)
I_{STC_use} = support-capacitor -load current
I_{FOR} = " " -format current
I_{LC} = " " -leakage current

note: Formula (3) is only correct under the condition, that the format current and the leakage current are voltage independent.

example:

V_{STC} = 6.0 V STC-parameter C_{STC} = 4.7 µF
I_{STC_use} = 300 µA I_{LC} = 5 µA
I_{FOR} = 10 µA

load time: t_{LOAD} = 99 ms

When the STC voltage reaches the value of typically 7.0 V, a Zener diode takes over the additional current from the constant current source and holds the STC voltage at this level. As described before, it is important that the additional current is taken over because current variations may not appear on the Bus lines.

3.3-V constant voltage source

When the Bus voltage is switched on and the STC voltage increases, a comparator switches on a constant voltage source when the STC voltage reaches 6.0 V (typical). This constant voltage source could be used as module power supply. It's voltage level is regulated via a Bandgap diode to a constant 3.3 V and is supplied on pin VDD. This constant voltage source enables a supply current of up to 8 mA, as it is needed for temperature measurement applications

To avoid a possible oscillation of the constant voltage source, a capacitor of approximately 100 nF should be connected to the VDD pin. This capacitor is also required to give SVDD time for regulation of its voltage where the current load peaks.

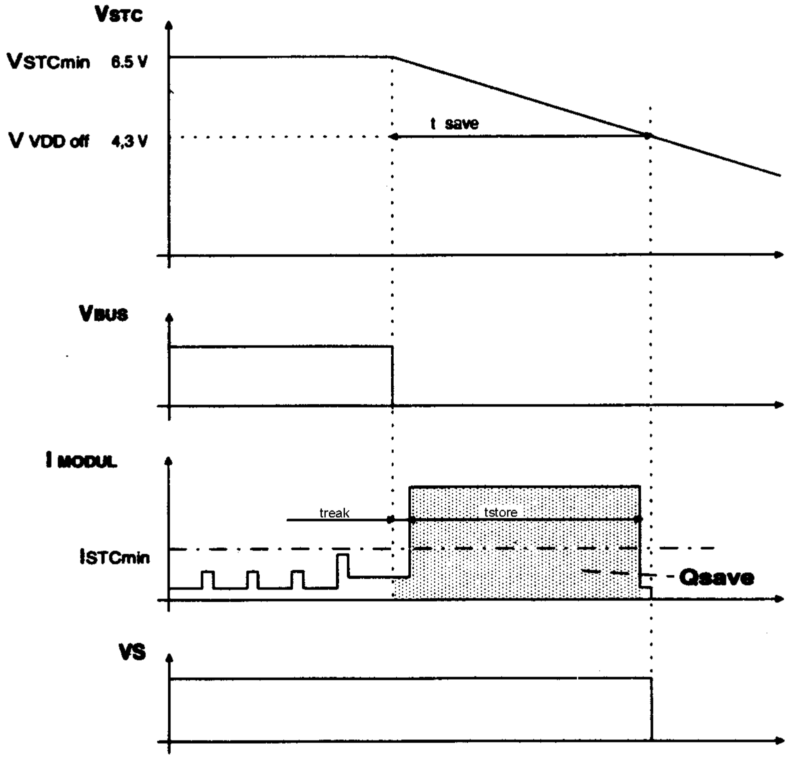
Power-fail and support capacitor:

When the Bus voltage breaks down, it could, under some conditions, be important that this is registered by the module processor as early as possible. The prewarning enables the processor of a remote supplied module to save important data and parameters such as meter readings in a nonvolatile memory. To realize this prewarning the TSS721 provides a so-called power-fail logic.

A comparator therefore activates the PF pin, as soon as the VB voltage level falls below typically V_{STC} + 0.3 V, because below this level the constant current source CS1 isn't able to load the support capacitor anymore and the module is supplied only by the support capacitor.

The time which is available for the recognition of the power-fail signal and for the storing of the data corresponds to the time which passes when the STC-voltage sinks from the level at Bus breakdown to its minimum value of typically 4.0 V, because at this level SVDD is switched off. Therefore, the support capacitor must be calculated so that the processor has enough time for recognizing power-fail and storing data.

The available time is dependent on the minimum STC voltage level during normal operation. When the module takes more current out of the TSS721 than the constant current source CS1 can supply (this is for example often the case during temperature measurements), the STC voltage drops to a value lower than its typical value. If the Bus voltage breaks down presicely at this moment, the available sink voltage is lower. You should design your module so that the STC voltage is at all times approximately 5.5 V, or higher. Figures 2 and 3 show two examples of a possible voltage diagram of the support capacitor and the respective calculations.



Calculations:

$C_{STC} = Q_{save} / (V_{STC} - V_{VDDoff})$

Parameter:

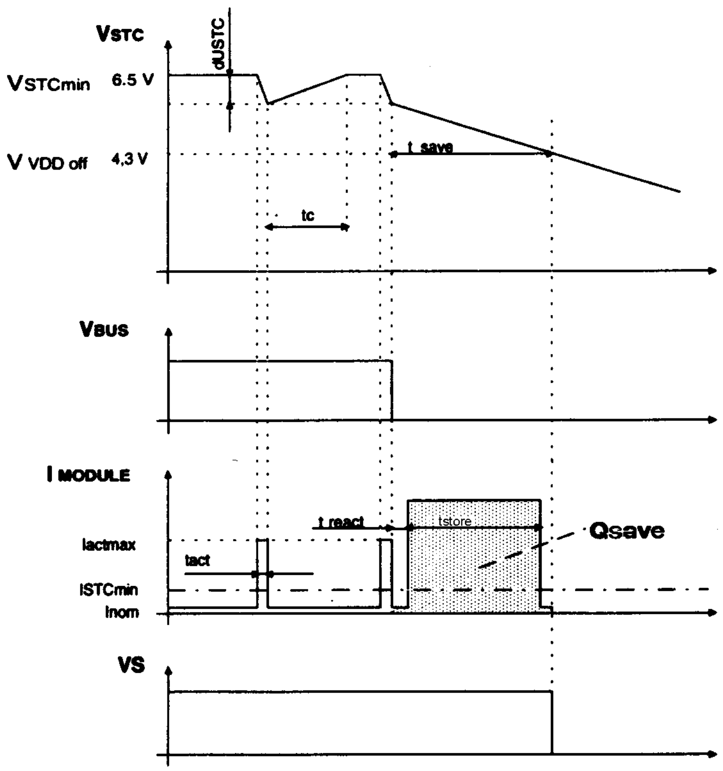
C_{STC} = capacity of support - capacitor

Q_{save} = for recognition of the Power-Fail signal and for storing of the relevant data needed load

V_{STC} = min. voltage of support - capacitor (min. 6.5V)

V_{VDDoff} = max. switch off level of the constant voltage source (max. 4.3V)

Figure 2. Voltage of support-capacitor over time (example 1)



Calculation of CSTC via interpolation :

(1) $C_{STC} = Q_{save} / (V_{STC} - dV_{STC} - V_{VDDoff})$

(2) $dV_{STC} = (I_{actmax} - I_{STC}) * t_{act} / C_{STC}$

(3) Repetition of (1) and (2) with calculated values until they don't change anymore

Parameter:

C_{STC} = capacity of support - capacitor

Q_{save} = for recognition of the Power - Fail signal and for storing of the relevant data needed load

V_{STC} = min. voltage of support - capacitor (min. 6.5V)

dV_{STC} = voltage drop of support- capacitor at module current peaks

I_{actmax} = max. possible module current

t_{act} = duration of module current

I_{STC} = support - capacitor load current

V_{VDDoff} = max. switch off level of the current voltage source (max. 4.3V)

Calculation of tc:

$t_c = C_{STC} * dV_{STC} / (I_{STC} - I_{nom})$

t_c = support - capacitor loadtime = min. waittime between two module current peaks

Figure 3. Voltage of support-capacitor over time (example 2)

Voltage switch VS:

If the voltage of the STC sinks below typically 4.0 V, a comparator switches SVDD off, because it isn't able to regulate the voltage at this level.

At the same time the VS output goes from high to low. This is important for use with mixed battery- /remote power supply. In those applications theVS pin must be connected to a FET, for example the BSS84 p-channel DMOS FET in reverse mode (reverse mode because this transistor has a diode from drain to source). This diode loads the battery if its voltage is lower than VDD and it would then overload the battery.

When the Bus voltage breaks down, the VS pin becomes low and the FET switches the battery to the VDD pin, so that the module is now powered from the battery. Because the TSS721 is made in a bipolar process, an integration of the FET isn't possible, as a biploar transistor needs too high a basic current.

When switching over from remote- to battery-supply or vice versa it is possible that the regulation circuit of SVDD may react slower than the FET and a short voltage collapse could be the effect. This can be avoided by connecting a capacitor to the VDD pin.

System voltage monitoring via BAT:

Because the module could be supplied either by battery or via Bus and therefore the voltage levels vary, the inputs and outputs of the interface device on the processor side must be adjusted accordingly. This is realized in the TSS721 with an automatic level adjust. With the BAT pin the processor supply voltage is measured and the input and output drivers are regulated accordingly.

2.1.2. Digital functions

Dynamic level detection:

Because of the potentially great line resistance and very varying action locations, not every module has the same Bus voltage on its inputs. A module near to the controller has approximately 42-V Bus voltage, while a module at the end of the Bus lines, for example, gets only 24-V Bus voltage. As a result of that, the voltage level for the detection of a SPACE signal cannot be static, but must be adapted to the respective local MARK voltage level.

To realize this, a capacitor is connected to the SC pin of the TSS721 and is charged with a constant current of nominal 15 µA. The voltage level of this capacitor is typically, in operating mode, 8.6 V below the Bus voltage in MARK state. The SPACE recognition level of the receive logic is 1.8 V higher at MARK - 6.8 V and varies over temperature, Bus voltage and process variations between MARK - 5.7 V and MARK - 7.9 V. From this voltage level the maximum voltage drop of the SC capatior must be subtracted (Figure 4).

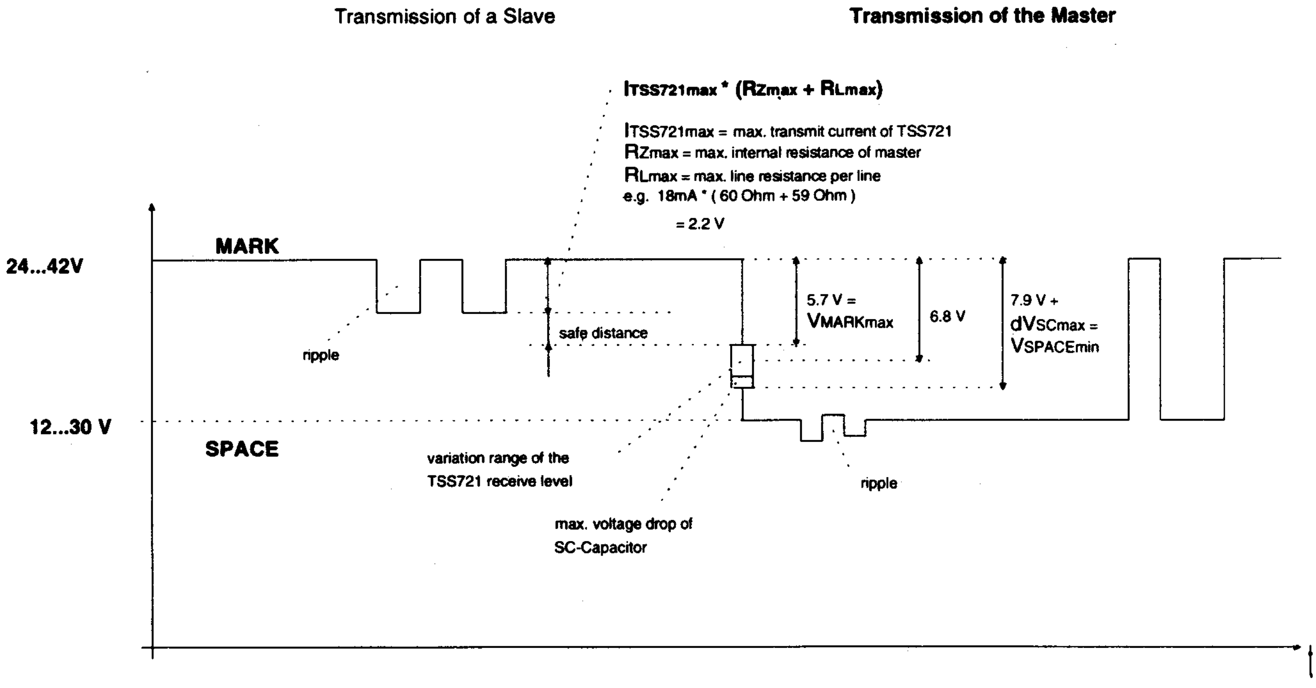


Figure 4. M-BUS voltage level at the module

Because the Bus voltage varies, the SC capacitor has to be unloaded with a specific current. This current is about a factor of 10 lower than the charge current. This is caused by the UART Bus-protocol, which requires a minimum of 1 SPACE bit per 11 bits. To compensate the maximum 10 bit-time long unload of the SC capacitor, it has therefore to be charged in one bit-time. The load and unload of the capacitor during the transmission causes a fluctuating voltage on the SC capacitor.

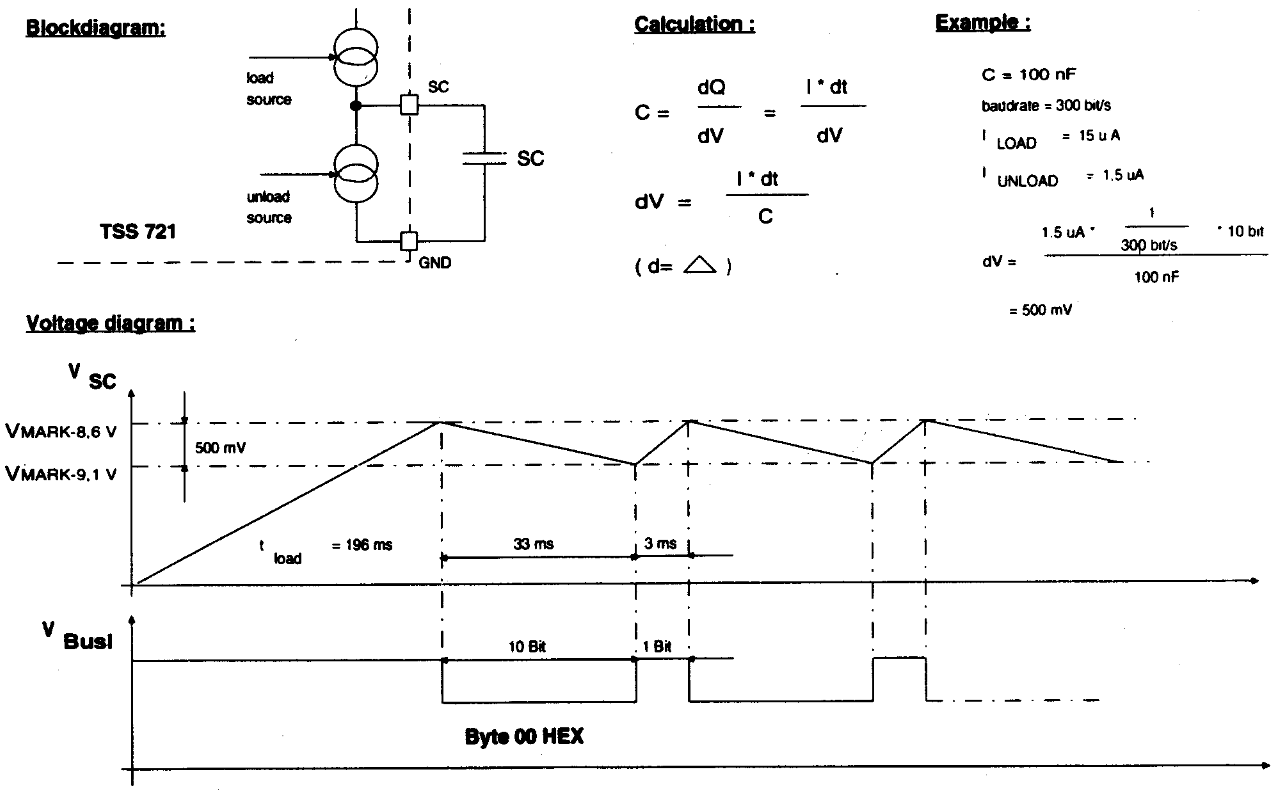


Figure 5. Possible voltage diagram of SC capacitor

When calculating the value of the SC capacitor, two things must be taken into account:

1. With a very low baudrate (e.g. 300 bits/s) and a small capacitor, the drop voltage of the SC capacitor is very high. If the voltage lift of the controller in SPACE transmit is also on the lower limit, then an error in transmission could result. As you can see in the example in Figure 5, the drop voltage could be about 500 mV.

2. The higher the value of the SC capatior is, the longer it requires until it reaches the operating voltage level after switching on the Bus voltage.

example:

V_{BUS}	= max. 42 V	:	Bus voltage in MARK state
I_{LOAD}	= min. 10 µA	:	current of the load source
S_C	= 100 nF	:	capacity of the SC capacitor

$$t_{LOAD} = \frac{(V_{BUS} - 8.6\ V) * SC}{I_{LOAD}} = 334\ ms$$

By selecting a greater capacitor and with minimum load current, load times of some seconds could be the result.

For the SC capacitor only film or ceramic capacitors should be used, because these are characterised by low leakage and format currents.

Receive and transmit logic:
In MARK state the TX-pin outputs a high signal. If the Bus voltage drops under the SC level, then the TX-pin outputs a low level.

The RX pin has an internal pull-up resistor and therefore when in Mark-state (idle state) at high level, the transmit current source CS3 is switched off. When a voltage level lower than UBAT/2 is input on the RX pin, the constant current source CS3 is switched on and a current pulse appears on the Bus lines.

The value of CS3 is adjustable via a resistor on pin RIS. It can be calculated with the following formula:

$$I_{CS3} = \frac{V_{RIS}}{R_{RIS}} \quad 0.3\mathrm{mA} \qquad (4)$$

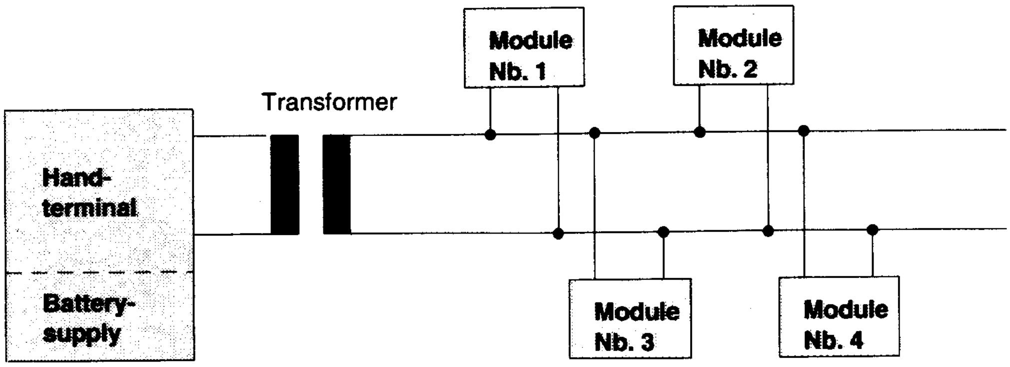
here: V_{RIS} = voltage on pin RIS (typically 1.76 V)
R_{RIS} = resistor between RIS and GND
I_{CS3} = value of pulse current of CS3

That the CS3 is adjustable is a great advantage for Minibus systems with limited power supplies, which could not drive the 20 mA current pulses. Such Minibus systems are, for example, Bus systems where the meters are readout inductive.

Both the receive and the transmit parts provide a non-inverting and an inverting input and output, so that a connection to every processor is possible. For battery powered modules it is recommended to use the inverting logic, because by using the non-inverting logic it is possible that the current/necessary Bus voltage could be diverted from the battery.

An ECHO function is implemented between the transmit and receive parts of the TSS721. This function makes it possible for a signal input on the RX pin to output on the TX pin. This enables collision detection, because in case of simultaneous transmission of master and slave the received byte is mixed with the transmitted byte.

The ECHO function can also be helpful in operation of the TSS721 with optocouplers, because with it, it's easy to detect if the Bus is powered or not. If the Bus isn't powered, the transmitted byte could not be received.



reduced energy supply capacity → transmitt current of TSS721 << 20mA

Minibus Application Example

2.2 Description of the TSS721 Operating Modes

With the TSS721 three different energy supply modes can be utilized. They differ in whether the module is powered from the Bus, or if it has its own power supply, for example a battery. The circuit diagram of these three possible supply modes can be seen in Figure 6.

note: In all three operating modes the power for the TSS721 is taken from the Bus, so that the module supply is not charged.

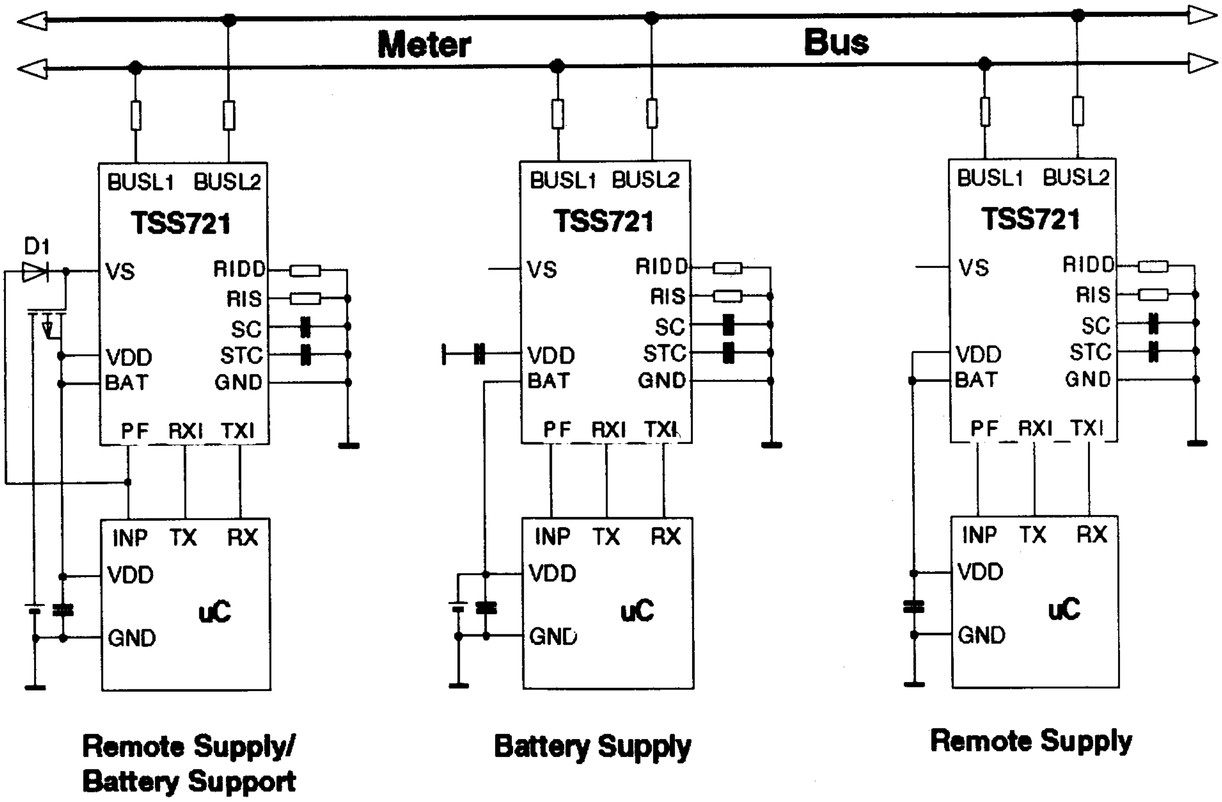


Figure 6. TSS721 Supply-Modes

Battery supply

In these applications the module is powered via battery or mains adaptor. To ensure level-fit of the inputs and outputs the TSS721 monitors the module power-supply voltage and regulates the level accordingly. The TSS721 acts only as transceiver device. The PF pin has no important function; it can only give information about the Bus activity.

This operating mode can be used for Bus installations, where the Bus voltage is available only during the transmission. Please note, that after switching on the Bus, a specific time is needed before the modules are ready for communication. This time depends mainly on the value of the support capacitor and the RIDD resistor.

Remote-supply / battery-support

While the Bus voltage is available, the module is powered from the M-Bus and the battery capacity isn't used. When the Bus voltage drops, the VS output becomes low-level and makes the FET low-resistant, which switches the battery voltage onto the module. Via the BAT input, the input and output levels are automatically regulated so that they fit to the supply voltage. During the switching, lulls in the power supply could occur which can be eliminated with a capacitor on the VDD Pin.

This operating mode provides advantages, if the Bus voltage is usually available, but the module must be powered the whole time. It is then possible to use batteries with little capacities by offering full module operating time.

The external diode D1 between pins PF and VS must meet the following requirements:

$$V_f < V_{GS} \; [\, ID < I_{STC}\text{-use} \,] \text{ at } I_f < 10\ \mu A$$
$$I_r < 1\mu A \text{ at } 7.5\ V$$

An example for the diode D1 is 1N6263 and for the FET is BSS84. Please watch R_{DSon} at low level battery voltage.

Remote-supply

In this case the module is fully powered from the Bus via the TSS721. The dropout of the Bus voltage is signalled to the processor via the power-fail signal. This enables the processor to save important data such as calibration values and counter readings in non-volatile memories (EEPROM, NVRAM). The support capacitor must be calculated so that the processor has time for recognition and storing of the data until the constant voltage source SVDD is switched off.

2.3 FUNCTION OF THE PROTECTION RESISTANCE

The protection resistor which should be connected in every module between the Bus line and the TSS721 must have a value of 430 Ω ± 2%. Because of better EMC results it can be divided into two resistors, so that before every Bus input of the TSS721, a resistor with the value of RS/2 is positioned (Figure 6).

The protection resistor performs vital services for the function of the M-Bus, which are detailed below:

Fuse against Bus fallout at device defect

In the case of any defect in the functioning of a module, it must be guaranteed that the Bus does not short-circuit, because only then can the power-supply of all modules on the Bus be guaranteed. Additionally, communication in both directions should be facilitated, because this makes it much easier to find the defective module. This demands a great protection resistor to minimize the short-circuit current.

Limitation of the thermal power dissipation of the TSS721

During transmission of many SPACE signals (00 hex) from the module to the master, the thermal power dissipation in the TSS721 could increase in extreme circumstances to 42 V x 20 mA = 840 mW. This is too much power for the small 16-pin SO-package of the TSS721. The protection resistor now takes over a part of this power dissipation so that the module can be used at higher free-air temperatures up to 85°C.

For the calculation of the protection resistor, the following points must be taken into consideration:

- The maximum value must complement the minimum possible voltage of the TSS721 due to the maximum acceptable voltage-drop caused by the protection resistor during transmission of the module.

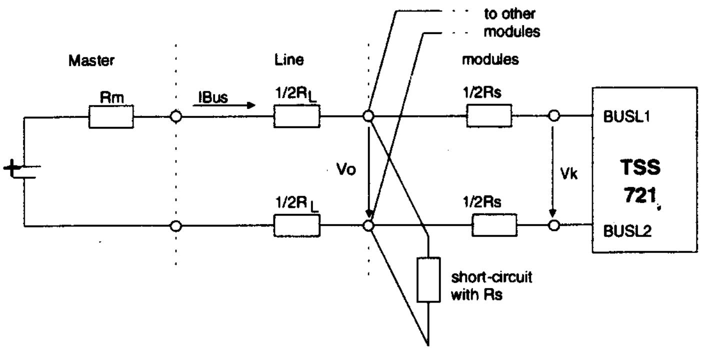
- The minimum value is fixed by the demand for the safe remote supply of all modules even when one module has a defect and short-circuits the bus.

The protection resistor has decisive influence on the value of the line resistance and thereby on the maximum distance. In this case we must distinguish between the transmit directions. In the case that one module has a short-circuit, the following scenarios could occur:

module transmits:	allowed line resistance decreases with increasing protection resistor because of increasing voltage drop;
master transmits:	allowed line resistance increases with increasing protection resistor because of decreasing short circuit current;

Both directions have therefore, in response to the value of the protection resistor, contrary effects. The optimum protection resistor depends on the number of modules and is with 256 modules approximately 450 Ω and for 64 modules approximately 340 Ω . Because the module number would mostly be in the range of 200 to 250 and the stock values of 430 Ω or 215 Ω (RS/2) are freely available, the M-Bus specification requires a value of 430 Ω . In Figures 7 and 8 you can see the calculation for each transmit direction and the specific resistance diagram.

Simplified M-BUS substitude circuit diagram :



Parameter

Vzm = Mark voltage master		(min 36V)
Vzs = Space voltage master		(min 24V)
Vks = clamp-voltage of TSS721 @ current transmit		(min 12V)
Vke = clamp-voltage of TSS721 @ receive		(min 11.3V)
Im = current absorbtion of the module		(max 1.5 mA)
Is = module current		(max 18mA)
Rm = measurement resistor of master		(max 60 Ohm)
nMod = number of modules		

Calculation :

assumption : short-circuit in a module receiver

1. Module transmits

Vm = Rm * Is = voltage drop at measurement resistor of master at pulse current

Vo = Vks + Rs (Im + Is) = module voltage at transmission

Ibus = Vo / Rs + Im (nMod - 1)+ Is = bus - current

Rl = (Vzm - Vo - Vm) / Ibus = max. line resistance

2. Master transmits

Vo = Vke + Rs * Im = module voltage at receive

Ibus = Vo / Rs + Im (nMod -1) = bus-current

Rl = (Vzs - Vo) / Ibus = max. line-resistance

Figure 7. Maximum line resistance R$_L$ depending on protection resistor R$_S$

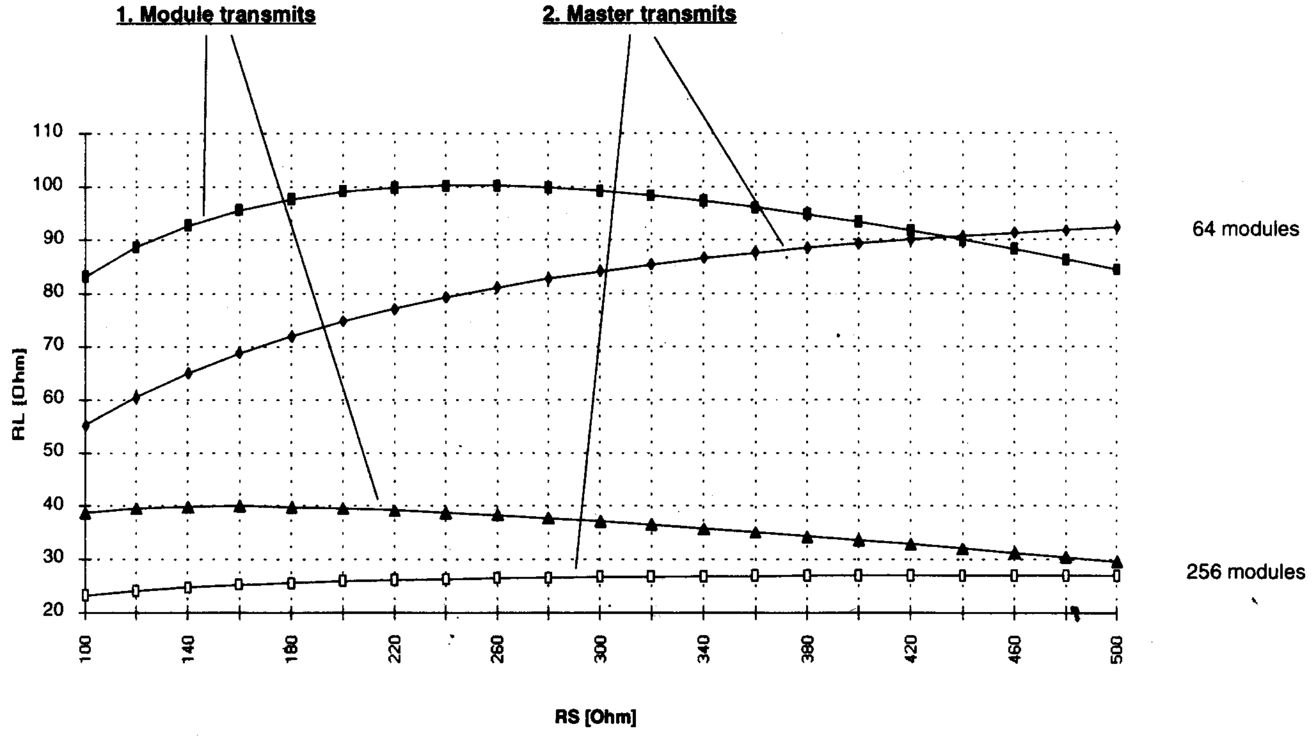


Figure 8. Maximum line resistance depending on protection resistor

Parameter:

Rja	= thermal resistance of S0-package	(125 grdC/W)
Vzm	= MARK-voltage of master	(max. 42V)
Rs	= protection resistor of the module	
Is	= module-transmit current	(max. 18mA)
Im	= current absorption of the Module	(max 3.0 mA)
Rm	= measurement resistor of master	(min. 47 Ohm)
TR	= tactrate (at least one bit at 10 bit high)	10/11
T	= max. free-air temperature of TSS721	

Calculation formula :

Vrs = Rs * (Is + Im)	= max. voltage drop on protection resistor
Vm = Rm * Is	= min. voltage drop at measurement resistor of master with peak current load
Ptot = (Vzm - Vrs - Vm) * (Is + Im) * TR	= max. power dissipation of TSS721

Graphic:

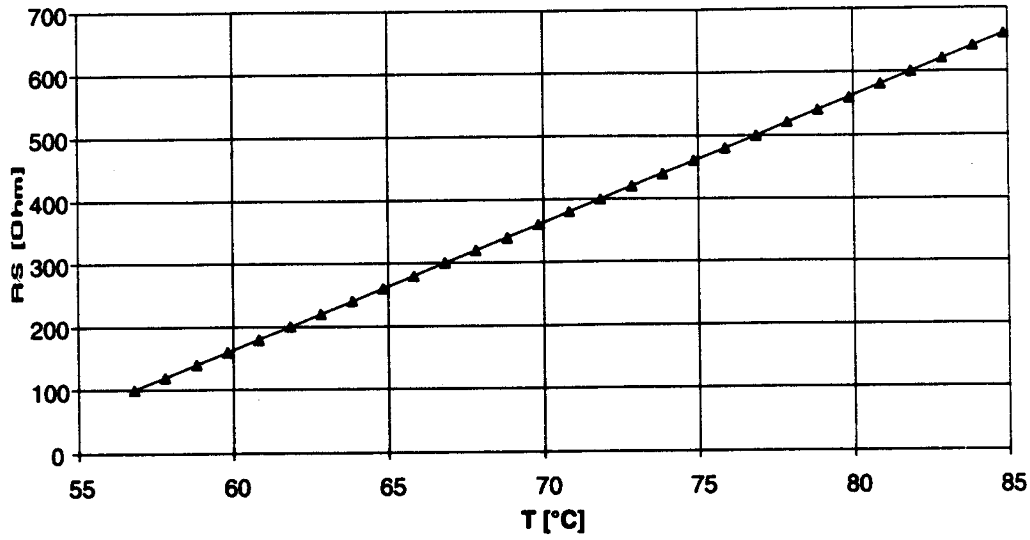


Figure 9. Maximum free-air temperature of TSS721 refering to the protection resistor

In Figure 9 it is obvious how the free-air temperature increases with increasing protection resistance. With a protection resistor of 430 Ω a free-air temperature of 75°C is possible.

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3. CONCLUSION

The TSS721 meets all requirements for a cost efficient transceiver device and is therefore predestined for use in M-Bus applications. The specification of the M-Bus Physical Layer is fulfilled with this device.

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