REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

#3 - Remove these components to stack north
#4 - Populate these components to stack north
Use 1k Resistors or adjust as needed
Header - Molex 90131-0765

#5 - THESE CAPACITORS ARE USED IN DESIGNS THAT HAVE
HIGH NOISE LEVELS WHEN STACKING IC'S. USE 22pF - 100pF CAPS AS NEEDED
(33pF 50V 0603 NPO 10% ARE THE DEFAULT CAPACITORS)

NORTH
1 - ALERT
2 - DRDY
3 - FAULT
4 - CONV
5 - CELL6
6 - CELL6
7 - SCLK
8 - CS
9 - SDO
10 - SDI

#4 P10 10P/DIL NORTH DNP

CAUTION
HIGH VOLTAGE

INDIVIDUAL GROUND PLANES ARE NECESSARY FOR PROPER NOISE REJECTION AND STABILITY OF THESE CIRCUITS

NOTE: The ground reference per circuit block is unique
The most negative connection of CELL0 is the ground reference for each chip.

DO NOT connect ground references from different chips

Only the ground reference CELL0 of circuit 1 is safe to connect non-isolated test equipment grounds.

SHUNT, ECON, TIN, BLACK
MOLEX part number# 90059-0007
Distributor - Digikey

P3 39502-1007_7-POS TP6 TP5
CELL 18 + / CELL 17 + / CELL 16 + / CELL 15 + / CELL 14 + / CELL 13 + / CELL 13 -
R152 0R0 RES0603 · R149 DNP RES0603 · C89 0.0033uf 50V CAP0603 · 3-VSS · 2-VSS

P2 39502-1007_7-POS TP4
CELL 12 + / CELL 11 + / CELL 10 + / CELL 9 + / CELL 8 + / CELL 7 + / CELL 7 -
R110 0R0 RES0603 · R90 DNP RES0603 · TP3 · CS3 0.0033uf 50V CAP0603 · 2-VSS · 1-VSS

P1 39502-1007_7-POS TP2
CELL 6 + / CELL 5 + / CELL 4 + / CELL 3 + / CELL 2 + / CELL 1 + / CELL 1 -
R40 0R0 RES0603 · TP1 · 1-VSS

3-VBAT [1,4] · #5 C122 DNP CAP0603 · #5 C120 DNP CAP0603 · #5 C116 DNP CAP0603
#4 R204 DNP RES0603 · #3 R205 0R0 RES0603 · #3 R206 0R0 RES0603 · #3 R207 0R0 RES0603 · #3 R208 0R0 RES0603 · #3 R209 0R0 RES0603 · #3 R210 0R0 RES0603 · #3 R211 0R0 RES0603 · #3 R212 0R0 RES0603 · #4 R213 DNP RES0603 · #4 R214 DNP RES0603 · #4 R215 DNP RES0603
C125 0.0033uf 50V CAP0603 · 3-VSS · 3-VBAT [1,4] · #5 C123 DNP CAP0603

3-CONV_N · 3-DRDY_N · 3-ALERT_N · 3-FAULT_N · 3-SCLK_N · 3-SDO_N · 3-SDI_N · 3-CS_N

BQ76PL536_CIRCUIT3 SHEET-4
3-VBAT · 3-CELL6 · 3-CELL5 · 3-CELL4 · 3-CELL3 · 3-CELL2 · 3-CELL1 · 3-CELL0
CONV_N · DRDY_N · ALERT_N · FAULT_N · SCLK_N · SDO_N · SDI_N · CS_N

JP18 2P/SIP R180 1K 0.1% RES0805
JP17 2P/SIP R177 1K 0.1% RES0805
JP16 2P/SIP R171 1K 0.1% RES0805
JP15 2P/SIP R166 1K 0.1% RES0805
JP14 2P/SIP R163 1K 0.1% RES0805
JP13 2P/SIP R155 1K 0.1% RES0805

*1 - LOCATE THESE RESISTORS CLOSE TO THE MOST NORTH IC

R150 0R0 RES0603

GROUND PLANE OF CIRCUIT 3
GROUND PLANE OF CIRCUIT 2

EXTEND THE GROUND PLANE UNDER THE SOUTH COMM LINES TO JUST BELOW THE NORTH COMM PINS OF THE CHIP BELOW

*1 R159 1K RES0603 · *1 R157 1K RES0603 · *1 R158 1K RES0603
*2 R145 1K RES0603 · *2 R146 1K RES0603 · *2 R147 1K RES0603 · *2 R148 1K RES0603

C90 0.0033uf 50V CAP0603 · 3-VSS · 2-VSS

2-VBAT
2-CELL6 · 2-CELL5 · 2-CELL4 · 2-CELL3 · 2-CELL2 · 2-CELL1 · 2-CELL0
CONV_N · DRDY_N · ALERT_N · FAULT_N · SCLK_N · SDO_N · SDI_N · CS_N

JP12 2P/SIP R131 1K 0.1% RES0805
JP11 2P/SIP R128 1K 0.1% RES0805
JP10 2P/SIP R121 1K 0.1% RES0805
JP9 2P/SIP R119 1K 0.1% RES0805
JP8 2P/SIP R116 1K 0.1% RES0805
JP7 2P/SIP R112 1K 0.1% RES0805

*2 - LOCATE THESE RESISTORS CLOSE TO THE MOST SOUTH IC

BQ76PL536_CIRCUIT2 SHEET-3

*3 - LOCATE THESE RESISTORS CLOSE TO THE MOST NORTH IC

R89 0R0 RES0603

GROUND PLANE OF CIRCUIT 2
GROUND PLANE OF CIRCUIT 1

*3 R97 1K RES0603 · *3 R98 1K RES0603 · *3 R99 1K RES0603 · *3 R100 1K RES0603
*4 R85 1K RES0603 · *4 R86 1K RES0603 · *4 R87 1K RES0603 · *4 R88 1K RES0603

C54 0.0033uf 50V CAP0603 · 2-VSS · 1-VSS

1-VBAT
1-CELL6 · 1-CELL5 · 1-CELL4 · 1-CELL3 · 1-CELL2 · 1-CELL1 · 1-CELL0
CONV_N · DRDY_N · ALERT_N · FAULT_N · SCLK_N · SDO_N · SDI_N · CS_N

JP6 2P/SIP R80 1K 0.1% RES0805
JP5 2P/SIP R72 1K 0.1% RES0805
JP4 2P/SIP R65 1K 0.1% RES0805
JP3 2P/SIP R54 1K 0.1% RES0805
JP2 2P/SIP R50 1K 0.1% RES0805
JP1 2P/SIP R44 1K 0.1% RES0805

*4 - LOCATE THESE RESISTORS CLOSE TO THE MOST SOUTH IC

BQ76PL536_CIRCUIT1 SHEET-2

1-GPIO · 1-FAULT · 1-ALERT · 1-DRDY/TX · 1-CONV/RX · 1-SPI-MISO · 1-SPI-MOSI · 1-SPI-SCLK · 1-SPI-SS

P6 10P/DIL DNP · 1-VSS

ISO/COMMS SHEET-5
VSIG · FAULT · ALERT · DRDY · CONV · AGND
1-FAULT · 1-ALERT · 1-DRDY/TX · 1-CONV/RX · 1-SPI-MISO · 1-SPI-MOSI · 1-SPI-SCLK · 1-SPI-SS · 1-VSS
USB-5VDC · I2C-SCL · I2C-SDA · SPI-MISO · SPI-SCLK · SPI-SS · SPI-MOSI · AGND · 5VDC+ · AGND

P4 MTA100-HEADER-10PIN
VSIG · FAULT · ALERT · DRDY · CONV · GND · MOSI · MISO · CS · SCLK

P5 10P/DIL
SCL · SDA · MISO · SCLK · CS · GND · 5VDC · 5VDC · MOSI · GND

FEET/Mounting holes
X1 · X2 · X3 · X4

J5 DNP CONN JACK POWER 2.1MM PCB

EXTERNAL POWER
5VDC @200mA

J5- PART NUMBER
CUI INC. PJ-102A
2.1MM PCB MOUNT JACK

FIDUCIAL_MARK TPA · FIDUCIAL_MARK TPB · FIDUCIAL_MARK TPC · FIDUCIAL_MARK TPD

#5 - THESE CAPACITORS ARE USED IN DESIGNS THAT HAVE
HIGH NOISE LEVELS WHEN STACKING IC'S. USE 22pF - 100pF CAPS AS NEEDED

#1 - Populate these components to stack south
Use 1k Resistors or adjust as needed
Header - Molex 90131-0765
#2 - Remove these components to stack south

#5 C6 DNP CAP0603 · #5 C7 DNP CAP0603 · #5 C10 DNP CAP0603 · #5 C15 DNP CAP0603 · 1-VSS

#1 R5 DNP RES0603 · #1 R6 DNP RES0603 · #1 R7 DNP RES0603
#2 R8 0R0 RES0603 · #2 R9 0R0 RES0603 · #2 R10 0R0 RES0603 · #2 R11 0R0 RES0603 · #2 R12 0R0 RES0603 · #2 R13 0R0 RES0603 · #2 R14 0R0 RES0603 · #2 R15 0R0 RES0603 · #1 R16 DNP RES0603

#1 P7 10P/DIL SOUTH DNP

CAUTION
HIGH VOLTAGE

SOUTH
1 - ALERT
2 - DRDY
3 - FAULT
4 - CONV
5 - VSS
6 - VSS
7 - SCLK
8 - CS
9 - SDO
10 - SDI

ALL RESISTERS 5% UNLESS NOTED

SHEET 1

COMPANY:	Texas Instruments		
TITLE:	bq76PL536EVM-3 Stack Design Industrial Grade		
DRAWN: GORDON VARNEY	DATED: 8/12/2010	CODE:	SIZE: D / DRAWING NO: HPA507 / REV: E6
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	03/23/2010 / SHEET: 1 OF 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

** - Locate these components very close to U1.

CAUTION
HIGH VOLTAGE

@1 - THESE RESISTORS ARE USED TO INCREASE THE CURRENT LEVELS IN THE VERTICAL COMMS LINES IN DESIGNS THAT HAVE HIGH NOISE LEVELS OR LONG CABLE LENGTHS IN THE VERTICAL COMMS USE 2.0MEG RESISTORS WHEN NEEDED.

SLAVE MODE - REMOVE R36 AND ADD R33
S - USE A 100K RESISTOR IN R212 FOR SLAVE MODE

HOST MODE - REMOVE R33 AND ADD R36 (DEFAULT)
H - USE A 0R0 RESISTOR IN R213 FOR HOST MODE

THERMISTOR NTC 10K OHM 1% 0603
PANASONIC PART NUMBER # ERT-J1VG103FA

T2-1,2 T1-3,4 pair on 0.100" spacing

THE GPIA FILTER COMPONENTS ARE NOT POPULATED
*5 - REMOVE THESE PARTS AND POPULATE THE FILTER AS NEEDED

"Bottom" part connects all _S pins to 1-VSS.

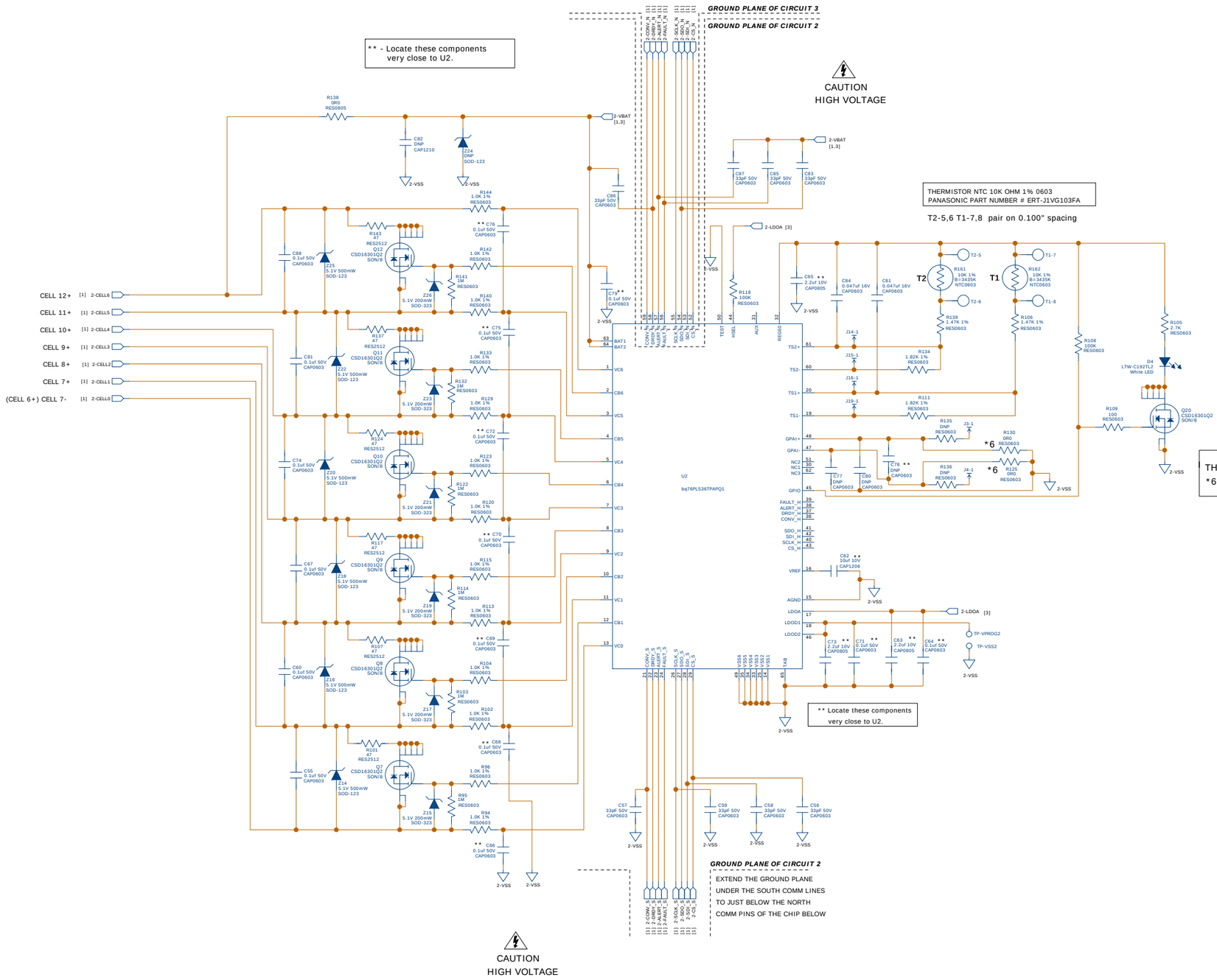
** Locate these components very close to U1.

ALL RESISTERS 5% UNLESS NOTED

SHEET 2

COMPANY:	Texas Instruments		
TITLE:	bq76PL536EVM-3 Stack Design Industrial Grade		
DRAWN: GORDON VARNEY	DATED: 8/12/2010		
CHECKED:	DATED:		
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:		
CODE:	SIZE: D	DRAWING NO: CIRCUIT 1 HPA507	REV: E6
SCALE:		SHEET: 2 OF 5	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



ALL RESISTERS 5% UNLESS NOTED

SHEET 3

COMPANY:	Texas Instruments		
TITLE:	bq76PL536EVM-3 Stack Design Industrial Grade		
DRAWN: GORDON VARNEY	DATED: 8/12/2010	CODE:	SIZE: D
CHECKED:	DATED:	DRAWING NO: CIRCUIT 2 HPA507	REV: E6
QUALITY CONTROL:	DATED:		
RELEASED:	DATED:	SCALE:	SHEET: 3 of 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

CAUTION
HIGH VOLTAGE

** - Locate these components very close to U3.

THERMISTOR NTC 10K OHM 1% 0603
PANASONIC PART NUMBER # ERT-J1VG103FA

T2-9,10 T1-11,12 pair on 0.100" spacing

"Top" part connects all _N pins to CELL6 of U3

THE GPIA FILTER COMPONENTS ARE NOT POPULATED
*7 - REMOVE THESE PARTS AND POPULATE THE FILTER AS NEEDED

** Locate these components very close to U3.

@2 - THIS RESISTOR IS USED TO INCREASE THE CURRENT LEVELS IN THE VERTICAL COMMS LINES IN DESIGNS THAT HAVE HIGH NOISE LEVELS OR LONG CABLE LENGTHS IN THE VERTICAL COMM PATHS. USE A 512K RESISTOR WHEN NEEDED

CAUTION
HIGH VOLTAGE

GROUND PLANE OF CIRCUIT 3
EXTEND THE GROUND PLANE UNDER THE SOUTH COMM LINES TO JUST BELOW THE NORTH COMM PINS OF THE CHIP BELOW

ALL RESISTERS 5% UNLESS NOTED

SHEET 4

COMPANY:	Texas Instruments
TITLE:	bq76PL536EVM-3 Stack Design Industrial Grade
DRAWN: GORDON VARNEY	DATED: 8/12/2010
CHECKED:	DATED:
QUALITY CONTROL:	DATED:
RELEASED:	DATED:
CODE:	SIZE: D
DRAWING NO:	CIRCUIT 3 HPA507
REV:	E6
SCALE:	SHEET: 4 OF 5

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

CAUTION
HIGH VOLTAGE

ISOLATION BOUNDRY
48 MIL ISOLATION REQUIRED

U5 ISO7241 — C34 0.1uf 50V CAP0603 — C47 0.1uf 50V CAP0603 — 1-VSS — AGND

U6 ISO7241 — C51 0.1uf 50V CAP0603 — C52 0.1uf 50V CAP0603 — 1-VSS — AGND

[1,2] 1-FAULT — FAULT — R84 100 RES0603
[1,2] 1-ALERT — ALERT — R79 100 RES0603
[1,2] 1-DRDY/TX — DRDY/TX — R75 100 RES0603
[1,2] 1-CONV/RX — CONV/RX — R70 100 RES0603
[1,2] 1-SPI-MISO — SPI - MISO — R64 100 RES0603
[1,2] 1-SPI-MOSI — SPI - MOSI — R51 100 RES0603
[1,2] 1-SPI-SCLK — SPI - SCLK — R58 100 RES0603
[1,2] 1-SPI-SS — SPI - SS — R48 100 RES0603

R92 1.0M RES0603 — R52 1.0M RES0603 — R91 1.0M RES0603 — C35 0.1uf 50V CAP0603 — R71 1.0M RES0603 — R67 100K RES0603 — AGND

U4 PCA9557PWR — R49 10K RES0603 — R53 10K RES0603 — R60 10K RES0603 — R39 DNP RES0603 — R43 DNP RES0603 — R48 DNP RES0603

UART or DATA FLAGS
VSIG [1]
FAULT [1]
ALERT [1]
DRDY [1]
CONV [1]

SPI / I2C
I2C-SDA [1]
I2C-SCL [1]
SPI-SS [1]
SPI-MOSI [1]
SPI-SCLK [1]
SPI-MISO [1]
R59 100 RES0603

CAUTION: WHEN USING AN EXTERNAL MICROCONTROLLR
PULL UP RESITORS CAN APPLY VOLTAGE TO THE MICRO WHEN
THE MICRO IS POWERED DOWN.

TP-SIN

JP19 A = 3.3VDC
JP19 B = 5.0VDC
JP19 JUMPER2SIP3 — A - 3.3VDC — B - 5VDC

U12 TPS76933DBVT — C30 10uF 10Vdc CAP0805 — C21 1.0uf 16V CAP0603 — R17 280 RES0603 — C4 0.1uf 50V CAP0603 — JP20 JUMPER2SIP3 — A - INT USB — B - EXT PWR

USB INPUT 4.5-5.5VDC
JP20 A = 5VDC / INT USB
JP20 B = 5VDC / EXT PWR
USB-5VDC [1]
5VDC 100MA
5VDC+ [1]

TP-SOUT — 5VDC OUT

U8 TPS76901DBVT — L1 LBC2012T100K 10uH 200mA IND0805 — C26 10uF 10Vdc CAP0805 — R37 523K 1% RES0603 — R34 169K 1% RES0603 — C20 4.7uf 10V CAP0603 — C11 4.7uf 10V CAP0603 — C12 0.1uf 50V CAP0603 — D1 BAT54WS-TP 30V 200mA SOD-323 — D2 BAT54WS-TP 30V 200mA SOD-323 — TP-VSS — 1-VSS

T1 Q4470-CLD 400uH 0.95DCR 1:1:3 SMD-C

Q22 CSD16301Q2 SON/8 — Q23 CSD16301Q2 SON/8 — C8 4.7uf 10V CAP0603 — C24 0.1uf 50V CAP0603 — C3 4.7uf 10V CAP0603 — C5 0.1uf 50V CAP0603 — C1 0.001uF 3kV CAP1808 — R19 1R0 RES0603 — AGND

U7 UCC2808 UCC2808D-2 — 1MHZ OSC — R26 10K RES0603 — R22 1K RES0603 — C13 150pF CAP0603 — TP-AGND

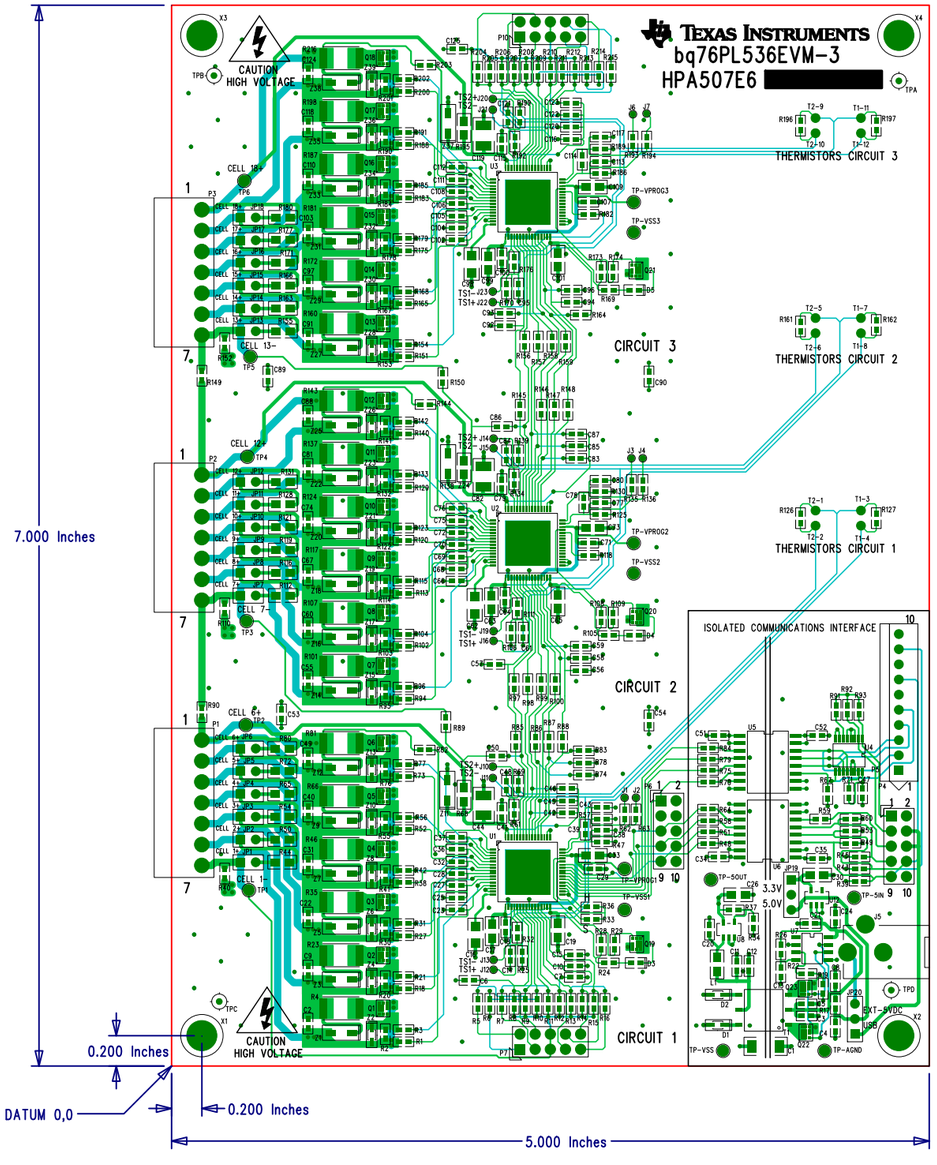
ALL RESISTERS 5% UNLESS NOTED

CAUTION
HIGH VOLTAGE

SHEET 5

DRAWN: GORDON VARNEY	DATED: 8/12/2010	COMPANY: Texas Instruments	
CHECKED:	DATED:	TITLE: bq76PL536EVM-3 Stack Design Industrial Grade	
QUALITY CONTROL:	DATED:	CODE:	SIZE: D / DRAWING NO: ISO/COMMS HPA507 / REV: E6
RELEASED:	DATED:	SCALE:	SHEET: 5 OF 5

*HOLE CHART IS IN MILS



COMPONENT SIDE VIEW

FABRICATION CHART

FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

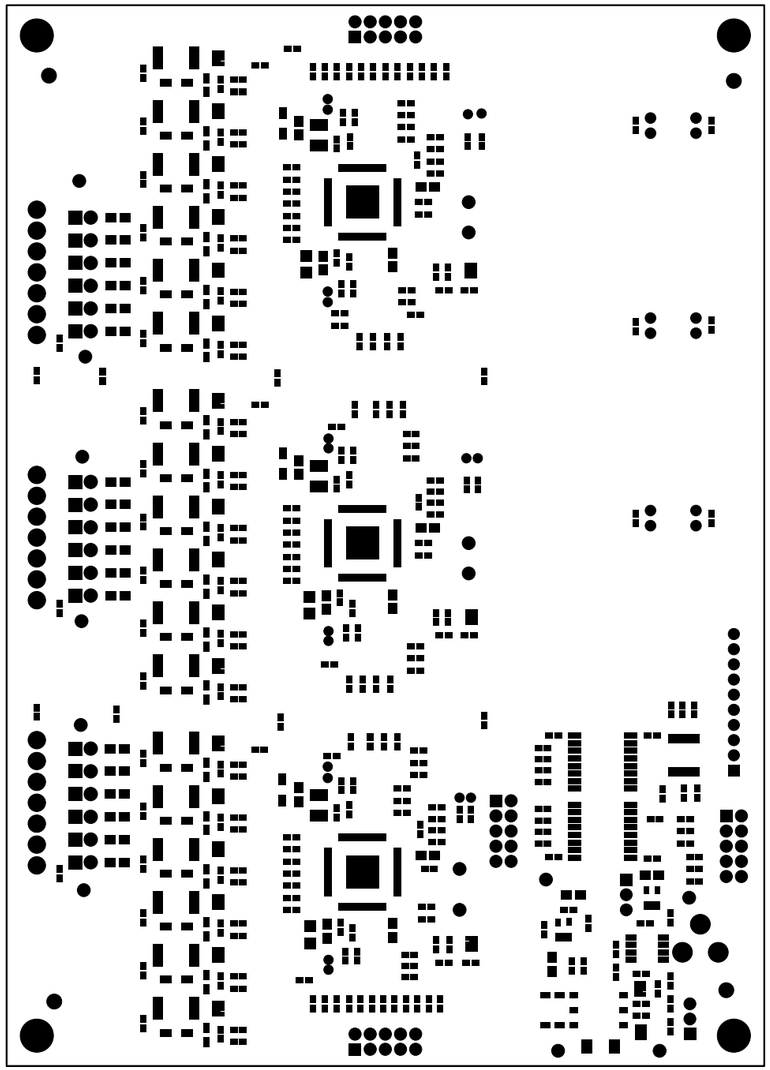
DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ALL MATERIALS, INCLUDING BUT NOT LIMITED TO BASE LAMINATE, BONDING MATERIALS AND SOLDERMASK COATINGS FORMING THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET UL-796 REQUIREMENTS AND BE RoHS COMPLIANT AND HAVE A FLAMMABILITY OF UL94V-0
2. BASE LAMINATE: PLASTIC SHEET, LAMINIATED METAL CLAD, ONE OR TWO SIDES, BASE MATERIAL NE A TYPE FR-4 OR EQUIVA.LENT, W/Tg = 180 Deg C OR HIGHER MINIMUM COMPOSITION TEMP (Td) OF 340 Deg C. GLASS EPOXY RESIN, COPPER-CLAD IN ACCORDANCE WITH 2 LAYER STACK-UP, COMPLIANT WITH LEAD FREE PROCESS
3. SOLDERMASK: SOLDERMASK OVER BARE COPPER (SMOBC) USING LIQUID PHOTO-IMAGEABLE SOLDERMASK IN ACCORDANCE WITH IPC-SM-840. COLOR GREEN. MINOR SOLDERMASK ADJUSTMENTS TO FACILITATE PCB FAB OR ASSEMBLY ARE ALLOWED PROVIDED NO DEFECTS ARE CREATED AS A RESULT.
4. PLATING: HOLES REQUIRING PLATING SHALL HAVE .001 MIL MIN THICK COPPER PLATE
5. FINISH: PLATE WITH RoHS COMPLIANT, IMMERSION SILVER PREFERRED, OR Sn/Ag/Cu, WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS
6. LEGEND: IF REQUIRED, SILKSCREEN LEGEND(S) WITH WHITE NON-CONDUCTIVE EPOXY INK.
7. MARKINGS: BOARD MUST BEAR VENDOR'S IDENTIFICATION CODE (ETCH OR WHITE NON-CONDUCTIVE INK) LOCATION OPTIONAL.
8. WORKMANSHIP: BOARD IS TO BE MANUFACTURED PER IPC-A-600 CLASS 2 REQUIREMENTS OR BETTER
9. DOCUMENTATION: PCB VENDOR IS REQUIRED TO RETURN ANY AND ALL DOCUMENTS SUPPLIED OR ULTIMATELY PURCHASED BY TEXAS INSTRUMENTS UPON COMPLETION OF PURCHASE ORDER
10. DRILL SIZES: HOLE DIAMETERS SHOWN ARE FINISHED SIZES AFTER PLATING UNLESS OTHERWISE NOTED.
11. TOLERANCES: UNLESS OTHERWISE SPECIFIED PCB TOLERANCES SHALL BE:
PCB THICKNESS TOLERANCE = +/ – 10% RELATIVE TO FINISHED THICKNESS, MEASURED FROM COPPER TO COPPER
PCB DIMENSIONAL TOLERANCE = +/–.005 INCHES RELATIVE TO BOARD PROFILE AND DRILL TO EDGE DIMENSIONS.
FINISHED HOLE DIAMETERS SHALL BE +/ –.003 INCHES RELATIVE THE DRILL TABLE DIMENSIONS.
12. PANEL BORDER: ANY METAL IN BORDER AREA INCLUDING PART NUMBER, DATECODE AND/OR REVISION LETTERS MUST BE COVERED WITH SOLDERMASK.
13. PROCESS CHANGES: NO DIMENSIONAL, MATERIAL, OR PROCESS CHANGES ARE ALLOWED WITHOUT PRIOR EXPLICIT WRITTEN PERMISSION FROM TEXAS INSTRUMENTS.

TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6	LY1			LY4	SST								FB

DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	



FABRICATION CHART

FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

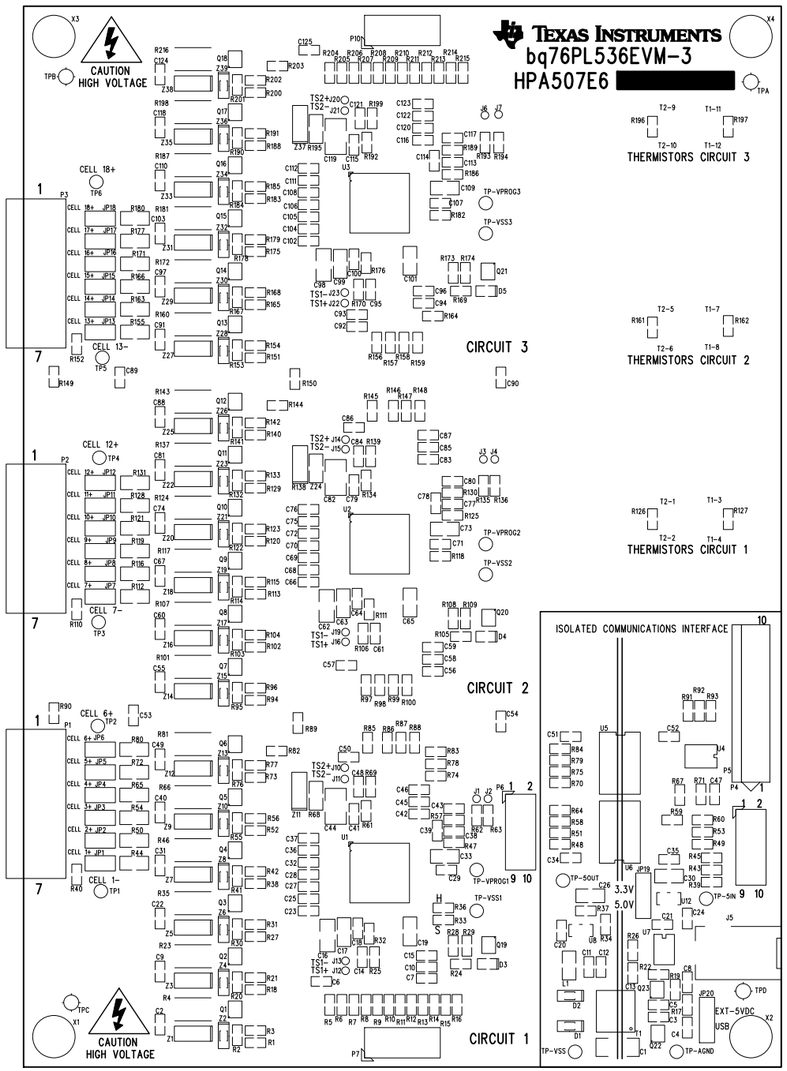
DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ALL MATERIALS, INCLUDING BUT NOT LIMITED TO BASE LAMINATE, BONDING MATERIALS AND SOLDERMASK COATINGS FORMING THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET UL-796 REQUIREMENTS AND BE RoHS COMPLIANT AND HAVE A FLAMMABILITY OF UL94V-0
2. BASE LAMINATE: PLASTIC SHEET, LAMINIATED METAL CLAD, ONE OR TWO SIDES, BASE MATERIAL NE A TYPE FR-4 OR EQUIVA.LENT, W/Tg = 180 Deg C OR HIGHER MINIMUM COMPOSITION TEMP (Td) OF 340 Deg C. GLASS EPOXY RESIN, COPPER-CLAD IN ACCORDANCE WITH 2 LAYER STACK-UP, COMPLIANT WITH LEAD FREE PROCESS
3. SOLDERMASK: SOLDERMASK OVER BARE COPPER (SMOBC) USING LIQUID PHOTO-IMAGEABLE SOLDERMASK IN ACCORDANCE WITH IPC-SM-840. COLOR GREEN. MINOR SOLDERMASK ADJUSTMENTS TO FACILITATE PCB FAB OR ASSEMBLY ARE ALLOWED PROVIDED NO DEFECTS ARE CREATED AS A RESULT.
4. PLATING: HOLES REQUIRING PLATING SHALL HAVE .001 MIL MIN THICK COPPER PLATE
5. FINISH: PLATE WITH RoHS COMPLIANT, IMMERSION SILVER PREFERRED, OR Sn/Ag/Cu, WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS
6. LEGEND: IF REQUIRED, SILKSCREEN LEGEND(S) WITH WHITE NON-CONDUCTIVE EPOXY INK.
7. MARKINGS: BOARD MUST BEAR VENDOR'S IDENTIFICATION CODE (ETCH OR WHITE NON-CONDUCTIVE INK) LOCATION OPTIONAL.
8. WORKMANSHIP: BOARD IS TO BE MANUFACTURED PER IPC-A-600 CLASS 2 REQUIREMENTS OR BETTER
9. DOCUMENTATION: PCB VENDOR IS REQUIRED TO RETURN ANY AND ALL DOCUMENTS SUPPLIED OR ULTIMATELY PURCHASED BY TEXAS INSTRUMENTS UPON COMPLETION OF PURCHASE ORDER
10. DRILL SIZES: HOLE DIAMETERS SHOWN ARE FINISHED SIZES AFTER PLATING UNLESS OTHERWISE NOTED.
11. TOLERANCES: UNLESS OTHERWISE SPECIFIED PCB TOLERANCES SHALL BE: PCB THICKNESS TOLERANCE = +/ – 10% RELATIVE TO FINISHED THICKNESS, MEASURED FROM COPPER TO COPPER PCB DIMENSIONAL TOLERANCE = +/-.005 INCHES RELATIVE TO BOARD PROFILE AND DRILL TO EDGE DIMENSIONS. FINISHED HOLE DIAMETERS SHALL BE +/ -.003 INCHES RELATIVE THE DRILL TABLE DIMENSIONS.
12. PANEL BORDER: ANY METAL IN BORDER AREA INCLUDING PART NUMBER, DATECODE AND/OR REVISION LETTERS MUST BE COVERED WITH SOLDERMASK.
13. PROCESS CHANGES: NO DIMENSIONAL, MATERIAL, OR PROCESS CHANGES ARE ALLOWED WITHOUT PRIOR EXPLICIT WRITTEN PERMISSION FROM TEXAS INSTRUMENTS.

TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6							SMT						FB

DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	



FABRICATION CHART

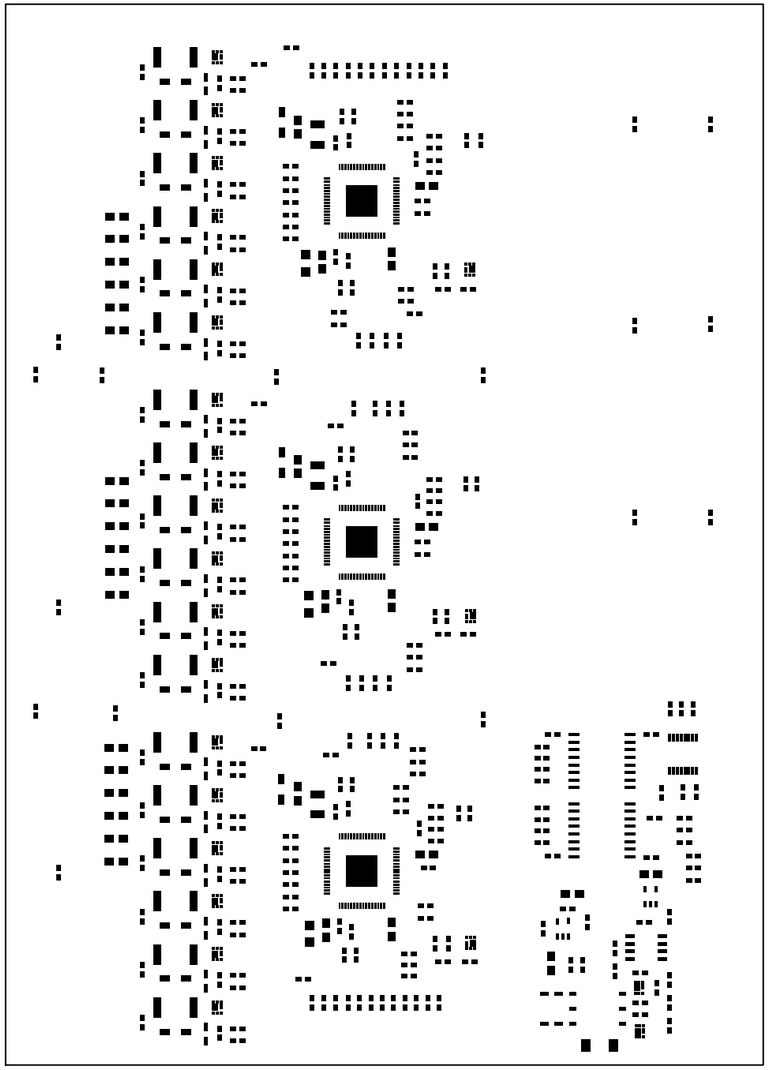
FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ALL MATERIALS, INCLUDING BUT NOT LIMITED TO BASE LAMINATE, BONDING MATERIALS AND SOLDERMASK COATINGS FORMING THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET UL-796 REQUIREMENTS AND BE RoHS COMPLIANT AND HAVE A FLAMMABILITY OF UL94V-0
2. BASE LAMINATE: PLASTIC SHEET, LAMINIATED METAL CLAD, ONE OR TWO SIDES, BASE MATERIAL NE A TYPE FR-4 OR EQUIVA.LENT, W/Tg = 180 Deg C OR HIGHER MINIMUM COMPOSITION TEMP (Td) OF 340 Deg C. GLASS EPOXY RESIN, COPPER-CLAD IN ACCORDANCE WITH 2 LAYER STACK-UP, COMPLIANT WITH LEAD FREE PROCESS
3. SOLDERMASK: SOLDERMASK OVER BARE COPPER (SMOBC) USING LIQUID PHOTO-IMAGEABLE SOLDERMASK IN ACCORDANCE WITH IPC-SM-840. COLOR GREEN. MINOR SOLDERMASK ADJUSTMENTS TO FACILITATE PCB FAB OR ASSEMBLY ARE ALLOWED PROVIDED NO DEFECTS ARE CREATED AS A RESULT.
4. PLATING: HOLES REQUIRING PLATING SHALL HAVE .001 MIL MIN THICK COPPER PLATE
5. FINISH: PLATE WITH RoHS COMPLIANT, IMMERSION SILVER PREFERRED, OR Sn/Ag/Cu, WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS
6. LEGEND: IF REQUIRED, SILKSCREEN LEGEND(S) WITH WHITE NON-CONDUCTIVE EPOXY INK.
7. MARKINGS: BOARD MUST BEAR VENDOR'S IDENTIFICATION CODE (ETCH OR WHITE NON-CONDUCTIVE INK) LOCATION OPTIONAL.
8. WORKMANSHIP: BOARD IS TO BE MANUFACTURED PER IPC-A-600 CLASS 2 REQUIREMENTS OR BETTER
9. DOCUMENTATION: PCB VENDOR IS REQUIRED TO RETURN ANY AND ALL DOCUMENTS SUPPLIED OR ULTIMATELY PURCHASED BY TEXAS INSTRUMENTS UPON COMPLETION OF PURCHASE ORDER
10. DRILL SIZES: HOLE DIAMETERS SHOWN ARE FINISHED SIZES AFTER PLATING UNLESS OTHERWISE NOTED.
11. TOLERANCES: UNLESS OTHERWISE SPECIFIED PCB TOLERANCES SHALL BE:
    PCB THICKNESS TOLERANCE = +/ – 10% RELATIVE TO FINISHED THICKNESS, MEASURED FROM COPPER TO COPPER
    PCB DIMENSIONAL TOLERANCE = +/–.005 INCHES RELATIVE TO BOARD PROFILE AND DRILL TO EDGE DIMENSIONS.
    FINISHED HOLE DIAMETERS SHALL BE +/ –.003 INCHES RELATIVE THE DRILL TABLE DIMENSIONS.
12. PANEL BORDER: ANY METAL IN BORDER AREA INCLUDING PART NUMBER, DATECODE AND/OR REVISION LETTERS MUST BE COVERED WITH SOLDERMASK.
13. PROCESS CHANGES: NO DIMENSIONAL, MATERIAL, OR PROCESS CHANGES ARE ALLOWED WITHOUT PRIOR EXPLICIT WRITTEN PERMISSION FROM TEXAS INSTRUMENTS.

TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6	LY1				SST								FB
DATE: 06/15/2010	FILENAME: HPA507E6 bq76PL536EVM-3 Stack Design.PCB	ENGINEER: Gordon Varney	PCB DESIGNER: Gordon Varney	MODIFIED DATE: 08/10/2010	TIME STAMP:								



FABRICATION CHART

FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ALL MATERIALS, INCLUDING BUT NOT LIMITED TO BASE LAMINATE, BONDING MATERIALS AND SOLDERMASK COATINGS FORMING THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET UL-796 REQUIREMENTS AND BE RoHS COMPLIANT AND HAVE A FLAMMABILITY OF UL94V-0
2. BASE LAMINATE: PLASTIC SHEET, LAMINIATED METAL CLAD, ONE OR TWO SIDES, BASE MATERIAL NE A TYPE FR-4 OR EQUIVA.LENT, W/Tg = 180 Deg C OR HIGHER MINIMUM COMPOSITION TEMP (Td) OF 340 Deg C. GLASS EPOXY RESIN, COPPER-CLAD IN ACCORDANCE WITH 2 LAYER STACK-UP, COMPLIANT WITH LEAD FREE PROCESS
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4. PLATING: HOLES REQUIRING PLATING SHALL HAVE .001 MIL MIN THICK COPPER PLATE
5. FINISH: PLATE WITH RoHS COMPLIANT, IMMERSION SILVER PREFERRED, OR Sn/Ag/Cu, WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS
6. LEGEND: IF REQUIRED, SILKSCREEN LEGEND(S) WITH WHITE NON-CONDUCTIVE EPOXY INK.
7. MARKINGS: BOARD MUST BEAR VENDOR'S IDENTIFICATION CODE (ETCH OR WHITE NON-CONDUCTIVE INK) LOCATION OPTIONAL.
8. WORKMANSHIP: BOARD IS TO BE MANUFACTURED PER IPC-A-600 CLASS 2 REQUIREMENTS OR BETTER
9. DOCUMENTATION: PCB VENDOR IS REQUIRED TO RETURN ANY AND ALL DOCUMENTS SUPPLIED OR ULTIMATELY PURCHASED BY TEXAS INSTRUMENTS UPON COMPLETION OF PURCHASE ORDER
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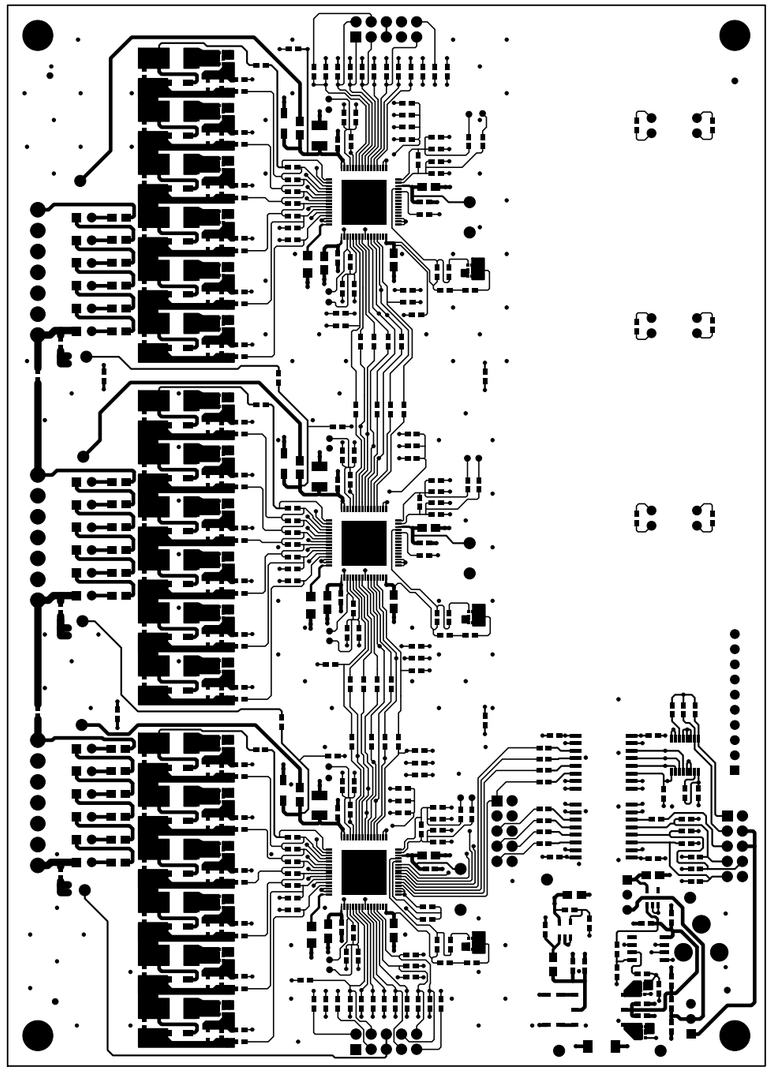
12. PANEL BORDER: ANY METAL IN BORDER AREA INCLUDING PART NUMBER, DATECODE AND/OR REVISION LETTERS MUST BE COVERED WITH SOLDERMASK.
13. PROCESS CHANGES: NO DIMENSIONAL, MATERIAL, OR PROCESS CHANGES ARE ALLOWED WITHOUT PRIOR EXPLICIT WRITTEN PERMISSION FROM TEXAS INSTRUMENTS.

TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6									PMT				FB

DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	



FABRICATION CHART

FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ALL MATERIALS, INCLUDING BUT NOT LIMITED TO BASE LAMINATE, BONDING MATERIALS AND SOLDERMASK COATINGS FORMING THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET UL-796 REQUIREMENTS AND BE RoHS COMPLIANT AND HAVE A FLAMMABILITY OF UL94V-0
2. BASE LAMINATE: PLASTIC SHEET, LAMINIIATED METAL CLAD, ONE OR TWO SIDES, BASE MATERIAL NE A TYPE FR-4 OR EQUIVA.LENT, W/Tg = 180 Deg C OR HIGHER MINIMUM COMPOSITION TEMP (Td) OF 340 Deg C. GLASS EPOXY RESIN, COPPER-CLAD IN ACCORDANCE WITH 2 LAYER STACK-UP, COMPLIANT WITH LEAD FREE PROCESS
3. SOLDERMASK: SOLDERMASK OVER BARE COPPER (SMOBC) USING LIQUID PHOTO-IMAGEABLE SOLDERMASK IN ACCORDANCE WITH IPC-SM-840. COLOR GREEN. MINOR SOLDERMASK ADJUSTMENTS TO FACILITATE PCB FAB OR ASSEMBLY ARE ALLOWED PROVIDED NO DEFECTS ARE CREATED AS A RESULT.
4. PLATING: HOLES REQUIRING PLATING SHALL HAVE .001 MIL MIN THICK COPPER PLATE
5. FINISH: PLATE WITH RoHS COMPLIANT, IMMERSION SILVER PREFERRED, OR Sn/Ag/Cu, WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS
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7. MARKINGS: BOARD MUST BEAR VENDOR'S IDENTIFICATION CODE (ETCH OR WHITE NON-CONDUCTIVE INK) LOCATION OPTIONAL.
8. WORKMANSHIP: BOARD IS TO BE MANUFACTURED PER IPC-A-600 CLASS 2 REQUIREMENTS OR BETTER
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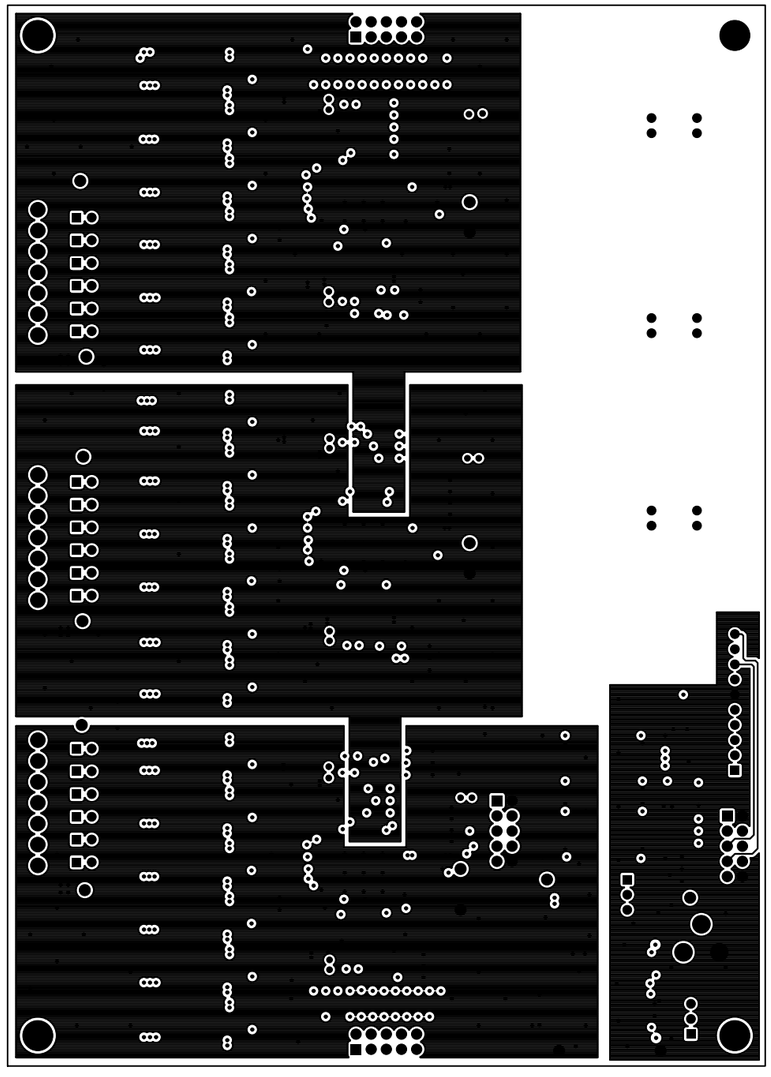
TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6	LY1												FB

DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	



FABRICATION CHART

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☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

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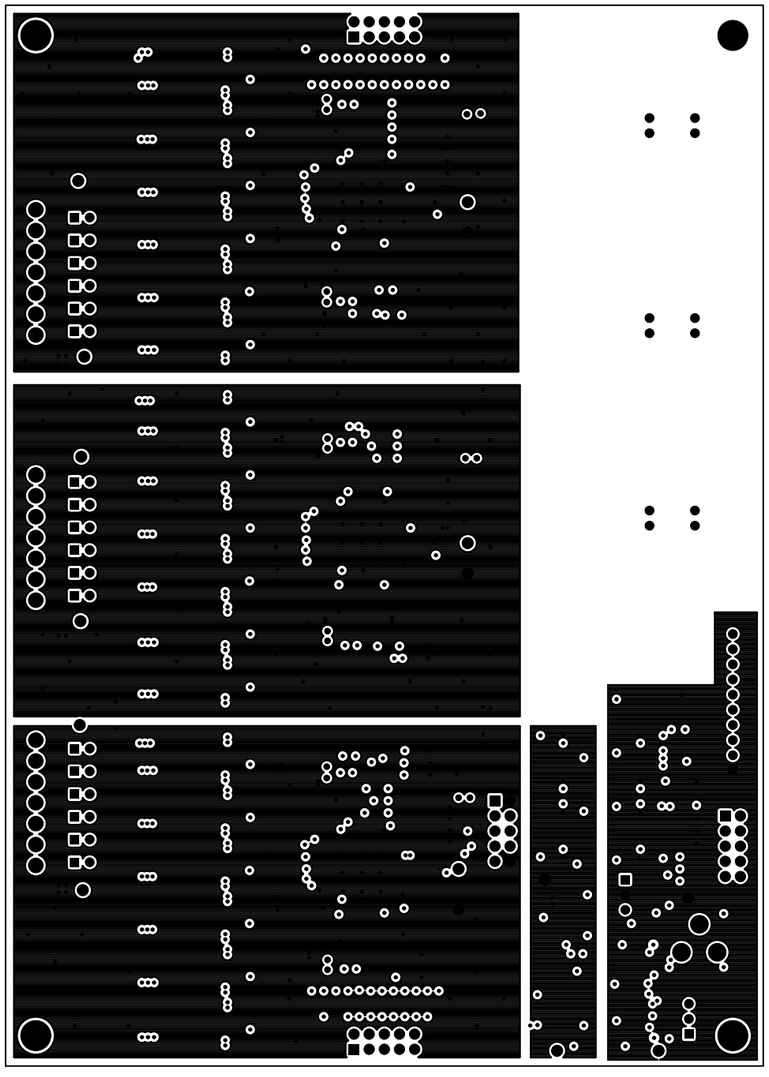
TEXAS INSTRUMENTS

COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
	LY2											FB

BOARD NO:	REV:	DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
HPA507	E6	06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	



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DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

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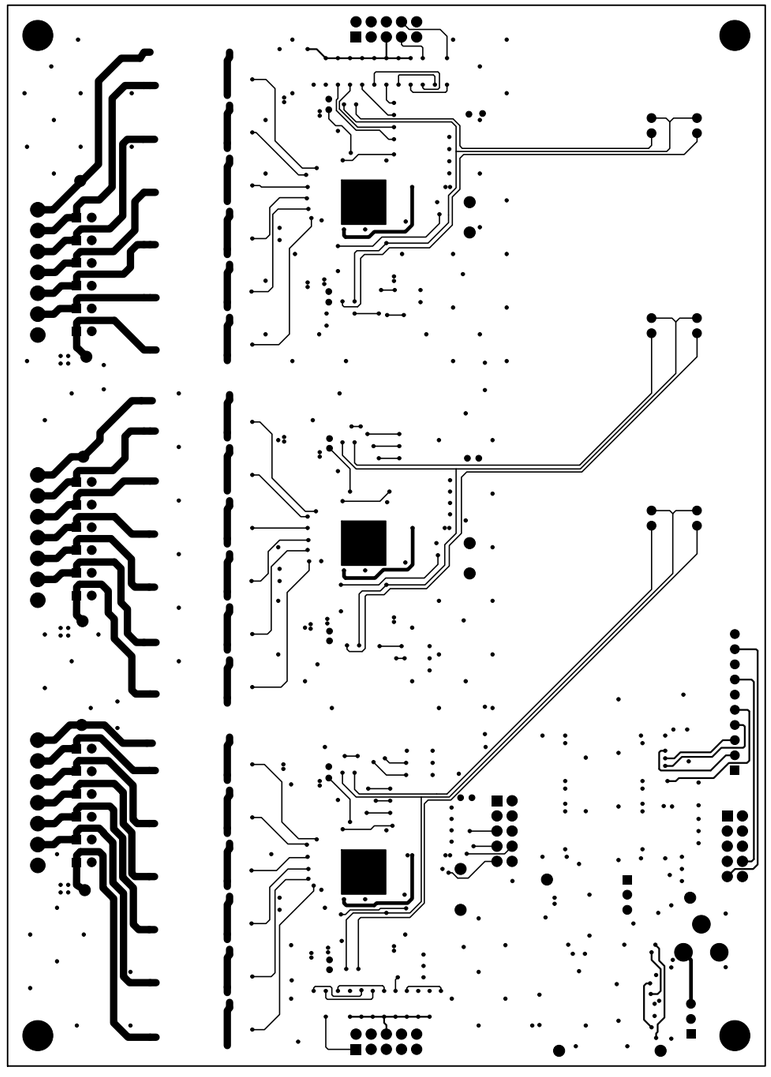
TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6			LY3										FB

DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	



FABRICATION CHART

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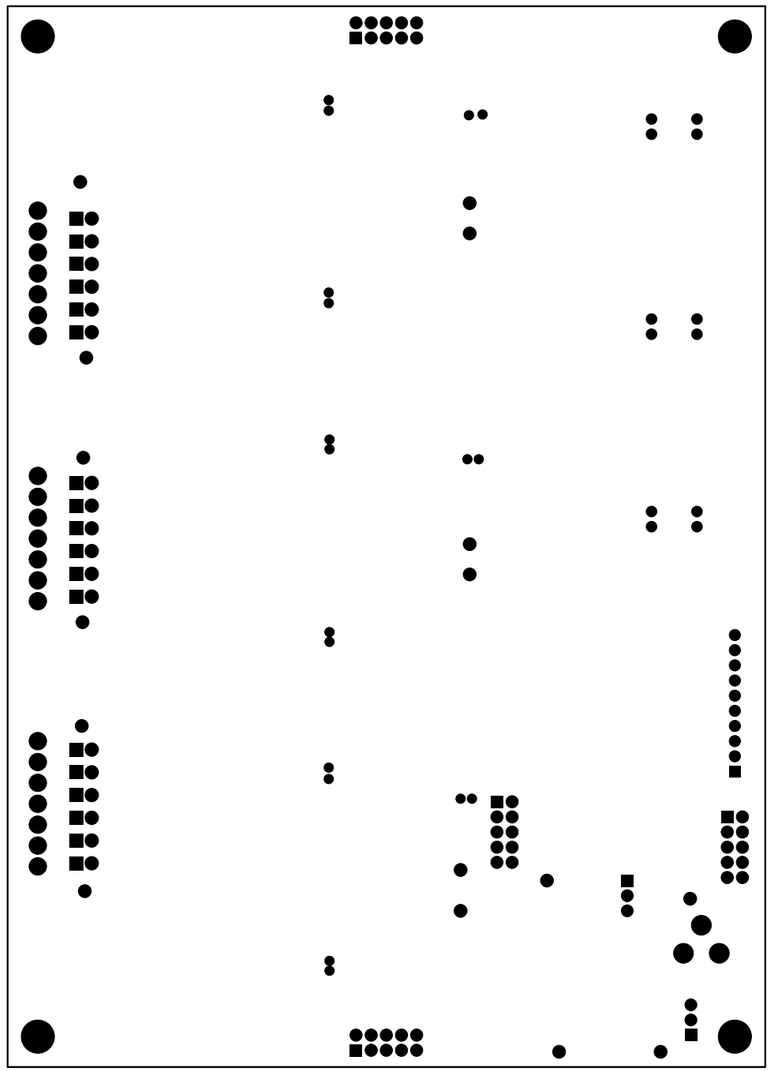
13. PROCESS CHANGES: NO DIMENSIONAL, MATERIAL, OR PROCESS CHANGES ARE ALLOWED WITHOUT PRIOR EXPLICIT WRITTEN PERMISSION FROM TEXAS INSTRUMENTS.

TEXAS INSTRUMENTS

BOARD NO:	REV:	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
		TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
HPA507	E6				LY4									FB

DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	



FABRICATION CHART

FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

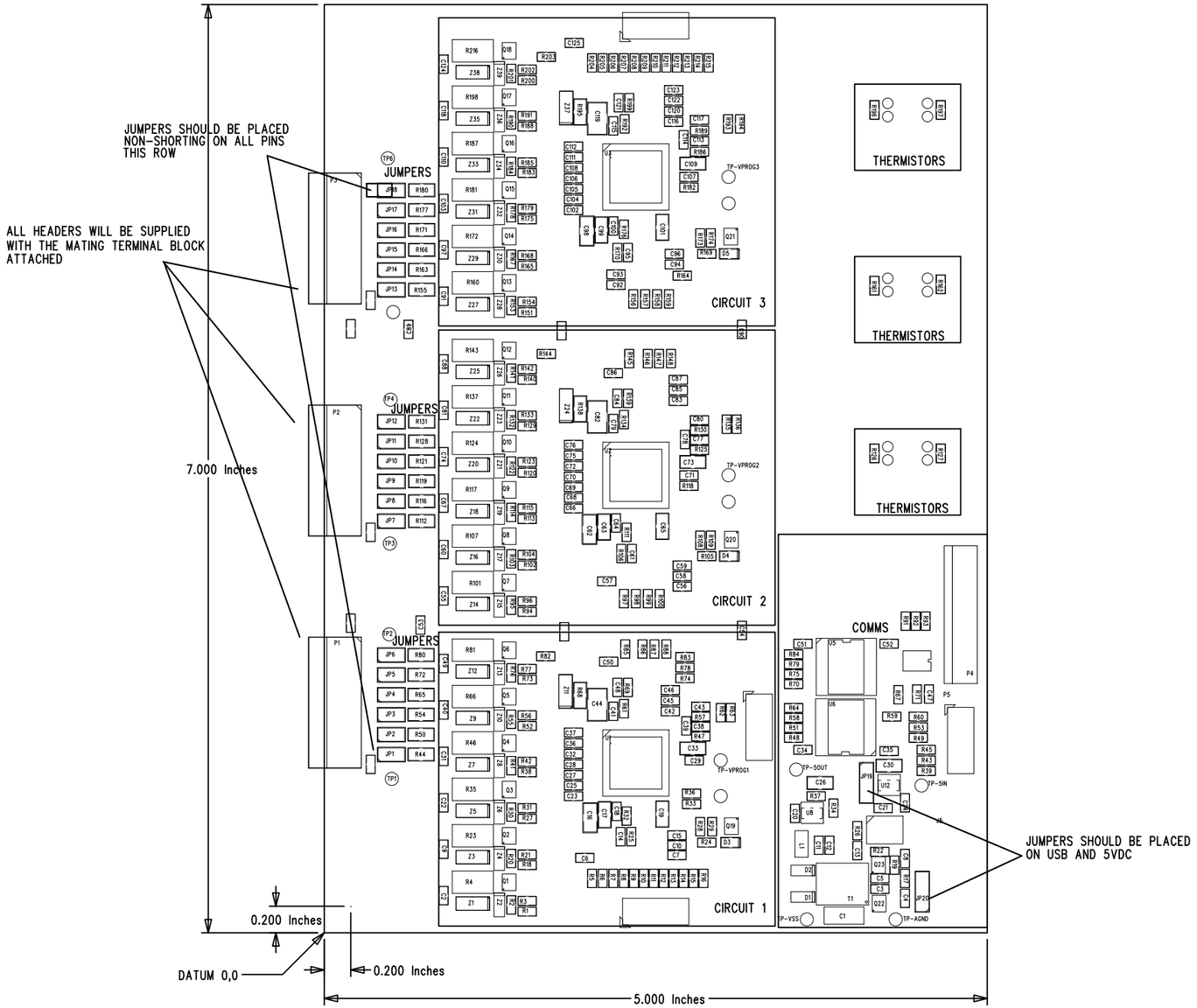
NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ALL MATERIALS, INCLUDING BUT NOT LIMITED TO BASE LAMINATE, BONDING MATERIALS AND SOLDERMASK COATINGS FORMING THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET UL-796 REQUIREMENTS AND BE RoHS COMPLIANT AND HAVE A FLAMMABILITY OF UL94V-0
2. BASE LAMINATE: PLASTIC SHEET, LAMINIIATED METAL CLAD, ONE OR TWO SIDES, BASE MATERIAL NE A TYPE FR-4 OR EQUIVA.LENT, W/Tg = 180 Deg C OR HIGHER MINIMUM COMPOSITION TEMP (Td) OF 340 Deg C. GLASS EPOXY RESIN, COPPER-CLAD IN ACCORDANCE WITH 2 LAYER STACK-UP, COMPLIANT WITH LEAD FREE PROCESS
3. SOLDERMASK: SOLDERMASK OVER BARE COPPER (SMOBC) USING LIQUID PHOTO-IMAGEABLE SOLDERMASK IN ACCORDANCE WITH IPC-SM-840. COLOR GREEN. MINOR SOLDERMASK ADJUSTMENTS TO FACILITATE PCB FAB OR ASSEMBLY ARE ALLOWED PROVIDED NO DEFECTS ARE CREATED AS A RESULT.
4. PLATING: HOLES REQUIRING PLATING SHALL HAVE .001 MIL MIN THICK COPPER PLATE
5. FINISH: PLATE WITH RoHS COMPLIANT, IMMERSION SILVER PREFERRED, OR Sn/Ag/Cu, WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS WITH RMA FLUX, 0.0005" +/ – 0.0003" THICK MIN ALL EXPOSED AREAS
6. LEGEND: IF REQUIRED, SILKSCREEN LEGEND(S) WITH WHITE NON-CONDUCTIVE EPOXY INK.
7. MARKINGS: BOARD MUST BEAR VENDOR'S IDENTIFICATION CODE (ETCH OR WHITE NON-CONDUCTIVE INK) LOCATION OPTIONAL.
8. WORKMANSHIP: BOARD IS TO BE MANUFACTURED PER IPC-A-600 CLASS 2 REQUIREMENTS OR BETTER
9. DOCUMENTATION: PCB VENDOR IS REQUIRED TO RETURN ANY AND ALL DOCUMENTS SUPPLIED OR ULTIMATELY PURCHASED BY TEXAS INSTRUMENTS UPON COMPLETION OF PURCHASE ORDER
10. DRILL SIZES: HOLE DIAMETERS SHOWN ARE FINISHED SIZES AFTER PLATING UNLESS OTHERWISE NOTED.
11. TOLERANCES: UNLESS OTHERWISE SPECIFIED PCB TOLERANCES SHALL BE:
    PCB THICKNESS TOLERANCE = +/ – 10% RELATIVE TO FINISHED THICKNESS, MEASURED FROM COPPER TO COPPER
    PCB DIMENSIONAL TOLERANCE = +/–.005 INCHES RELATIVE TO BOARD PROFILE AND DRILL TO EDGE DIMENSIONS.
    FINISHED HOLE DIAMETERS SHALL BE +/ –.003 INCHES RELATIVE THE DRILL TABLE DIMENSIONS.
12. PANEL BORDER: ANY METAL IN BORDER AREA INCLUDING PART NUMBER, DATECODE AND/OR REVISION LETTERS MUST BE COVERED WITH SOLDERMASK.
13. PROCESS CHANGES: NO DIMENSIONAL, MATERIAL, OR PROCESS CHANGES ARE ALLOWED WITHOUT PRIOR EXPLICIT WRITTEN PERMISSION FROM TEXAS INSTRUMENTS.

TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6								SMB					FB
DATE: 06/15/2010	FILENAME: HPA507E6 bq76PL536EVM-3 Stack Design.PCB		ENGINEER: Gordon Varney		PCB DESIGNER: Gordon Varney		MODIFIED DATE: 08/10/2010		TIME STAMP:				

*HOLE CHART IS IN MILS

FABRICATION CHART			
FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____
DESIGN	TRACE/GAP SPACING		LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____		☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____



COMPONENT SIDE VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: ALL MATERIALS, INCLUDING BUT NOT LIMITED TO BASE LAMINATE, BONDING MATERIALS AND SOLDERMASK COATINGS FORMING THE FINISHED PRINTED CIRCUIT BOARD SHALL MEET UL-796 REQUIREMENTS AND BE RoHS COMPLIANT AND HAVE A FLAMMABILITY OF UL94V-0
2. BASE LAMINATE: PLASTIC SHEET, LAMINIIATED METAL CLAD, ONE OR TWO SIDES, BASE MATERIAL NE A TYPE FR-4 OR EQUIVA.LENT, W/Tg = 180 Deg C OR HIGHER MINIMUM COMPOSITION TEMP (Td) OF 340 Deg C. GLASS EPOXY RESIN, COPPER-CLAD IN ACCORDANCE WITH 2 LAYER STACK-UP, COMPLIANT WITH LEAD FREE PROCESS
3. SOLDERMASK: SOLDERMASK OVER BARE COPPER (SMOBC) USING LIQUID PHOTO-IMAGEABLE SOLDERMASK IN ACCORDANCE WITH IPC-SM-840. COLOR GREEN. MINOR SOLDERMASK ADJUSTMENTS TO FACILITATE PCB FAB OR ASSEMBLY ARE ALLOWED PROVIDED NO DEFECTS ARE CREATED AS A RESULT.
4. PLATING: HOLES REQUIRING PLATING SHALL HAVE .001 MIL MIN THICK COPPER PLATE
5. FINISH: PLATE WITH RoHS COMPLIANT, IMMERSION SILVER PREFERRED, OR Sn/Ag/Cu, WITH RMA FLUX, 0.0005" +/ - 0.0003" THICK MIN ALL EXPOSED AREAS WITH RMA FLUX, 0.0005" +/ - 0.0003" THICK MIN ALL EXPOSED AREAS
6. LEGEND: IF REQUIRED, SILKSCREEN LEGEND(S) WITH WHITE NON-CONDUCTIVE EPOXY INK.
7. MARKINGS: BOARD MUST BEAR VENDOR'S IDENTIFICATION CODE (ETCH OR WHITE NON-CONDUCTIVE INK) LOCATION OPTIONAL.
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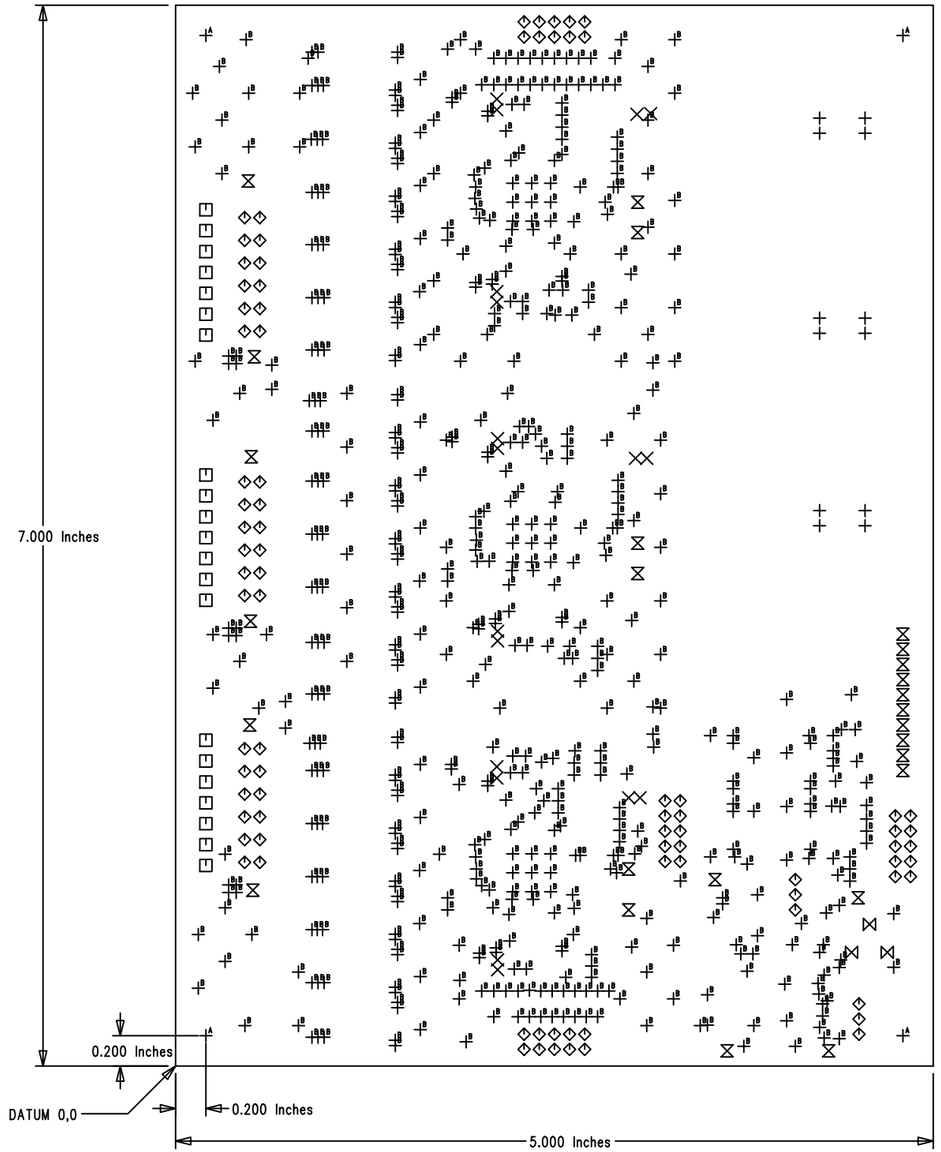
TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6											AST		FB
DATE: 06/15/2010	FILENAME: HPA507E6 bq76PL536EVM-3 Stack Design.PCB	ENGINEER: Gordon Varney	PCB DESIGNER: Gordon Varney	MODIFIED DATE: 08/10/2010	TIME STAMP:								



COMPONENT SIDE VIEW

*HOLE CHART IS IN MILS

SIZE	QTY	SYM	PLATED	TOL
32	12	+	YES	+/-0.0
20	18	X	YES	+/-0.0
48.03	21	square	YES	+/-0.0
37	82	diamond	YES	+/-0.0
40	26	hourglass	YES	+/-0.0
78.74	3	bowtie	YES	+/-0.0
187	4	A	YES	+/-0.0
12	616	B	YES	+/-0.0

FABRICATION CHART

FINISHED THICKNESS	SILKSCREEN	SOLDERMASK	FINISHED COPPER WEIGHT
☐ 0.031 ☒ 0.062 ☐ 0.093 ☐ 0.125	☒ LAYER 1 ☐ LAYER 2 ☐ NONE	☒ LAYER 1 ☒ LAYER 2 ☐ NONE	☐ 1 OZ. ☒ 2 OZ. ☐ OTHER _____

DESIGN	TRACE/GAP SPACING	LAYER COUNT
☐ SMD ☐ THRU-HOLE ☒ MIX	☐ 0.010/0.010 ☒ 0.008/0.007 ☐ 0.006/0.006 ☐ OTHER _____	☐ SINGLE SIDED ☐ 2 LAYER ☒ 4 LAYER ☐ OTHER _____

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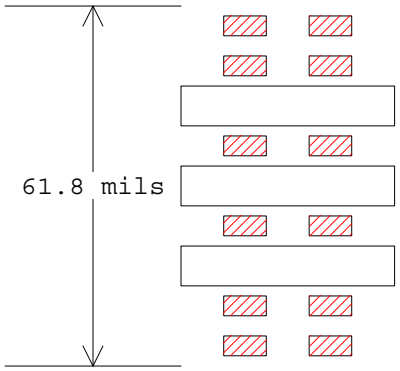
TEXAS INSTRUMENTS	COPPER LAYER NAME				SILKSCREEN		SOLDER MASK		PASTE MASK		ASSEMBLY		FAB DRAWING
	TOP 1	INNER 2	INNER 3	BOT 4	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT	
BOARD NO: HPA507 / REV: E6	LY1												FB

DATE:	FILENAME:	ENGINEER:	PCB DESIGNER:	MODIFIED DATE:	TIME STAMP:
06/15/2010	HPA507E6 bq76PL536EVM-3 Stack Design.PCB	Gordon Varney	Gordon Varney	08/10/2010	

Layer Stackup. Design: HPA507E6 bq76PL536EVM-3 Stack Design.hyp, Designer: Gordon Varney.

Number of layers: 9
Total thickness = 61.8 mils



NN	Layer Name	Type	Usage	Thickness mils, oz	Technology	Metal
1	Plating	Metal	Signal	1		Copper
2	Top	Metal	Signal	1		Copper
3	Substrate	Dielectric	Substrate	15	Prepreg	
4	Inner_Layer_2	Metal	Signal	2		Copper
5	Substrate	Dielectric	Substrate	21	Prepreg	
6	Inner_Layer_3	Metal	Signal	2		Copper
7	Substrate	Dielectric	Substrate	15	Prepreg	
8	Bottom	Metal	Signal	1		Copper
9	Plating	Metal	Signal	1		Copper