Optimizing DC/DC converter design for load transient performance, small size, or both!

Date:

Chris Glaser

Applications Engineer, SMTS

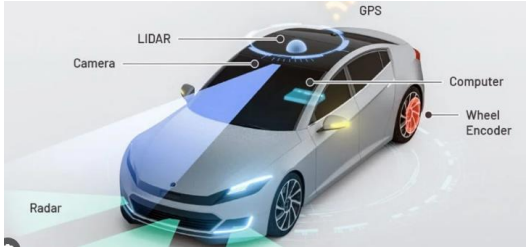
APP→SR→LVB→HC

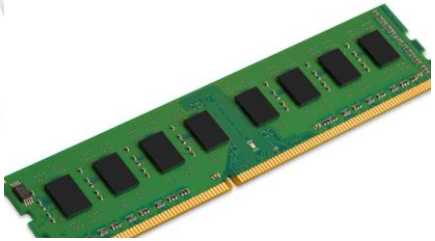
Agenda

- Introduction to DC/DC converter (integrated FETs) design with external compensation
- Design #1: optimized load transient performance
- Design #2: optimized for smallest size
- Design #3: optimized for smallest size with improved load transient performance using droop compensation and a power module
- Design summary
- Q&A

Processor power applications

High dynamic loads (load transients)





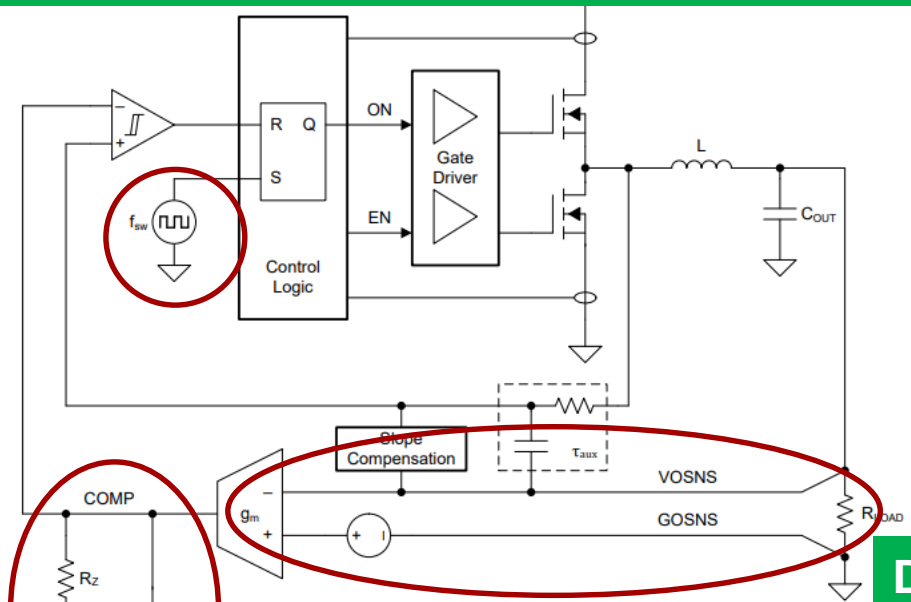
Static loads (no load transients)

All applications prefer to use the minimum output capacitance required → lower cost and smaller size

Fixed-frequency DCS-Control topology

Fast transient response with clock synchronization (link)

Fixed frequency (with an oscillator)



External compensation to optimize the transient response

Stackable (parallelable) for higher currents

Differential remote sense for excellent load regulation

Design summary (the end result)

Design	Goal	C_{OUT}	BW	Phase margin	Gain margin	Output ripple	Transient response
TPS62873 #1a 2.25MHz, 110nH	Transient	6 × 0603 4 × 0402	352kHz	28°	7dB	2.56mV p-p	31.9mV p-p
TPS62873 #1b 2.25MHz, 110nH	Transient	8 × 0603 4 × 0402	288kHz	37°	9dB	2.11mV p-p	31.7mV p-p
TPS62873 #2 2.25MHz, 110nH	Size	4 × 0603 2 × 0402	287kHz	48°	>20dB	3.20mV p-p	67.6mV p-p
TPSM8287B30 #3a 1.5MHz, 50nH	Transient	6 × 0603 4 × 0402	265kHz	56°	13dB	4.67mV p-p	39.4mV p-p
TPSM8287B30 #3b 1.5MHz, 50nH	Transient	6 × 0603 4 × 0402	272kHz	52°	12dB	4.67mV p-p	34.6mV p-p

All designs use the minimum C_{OUT} to meet the requirements

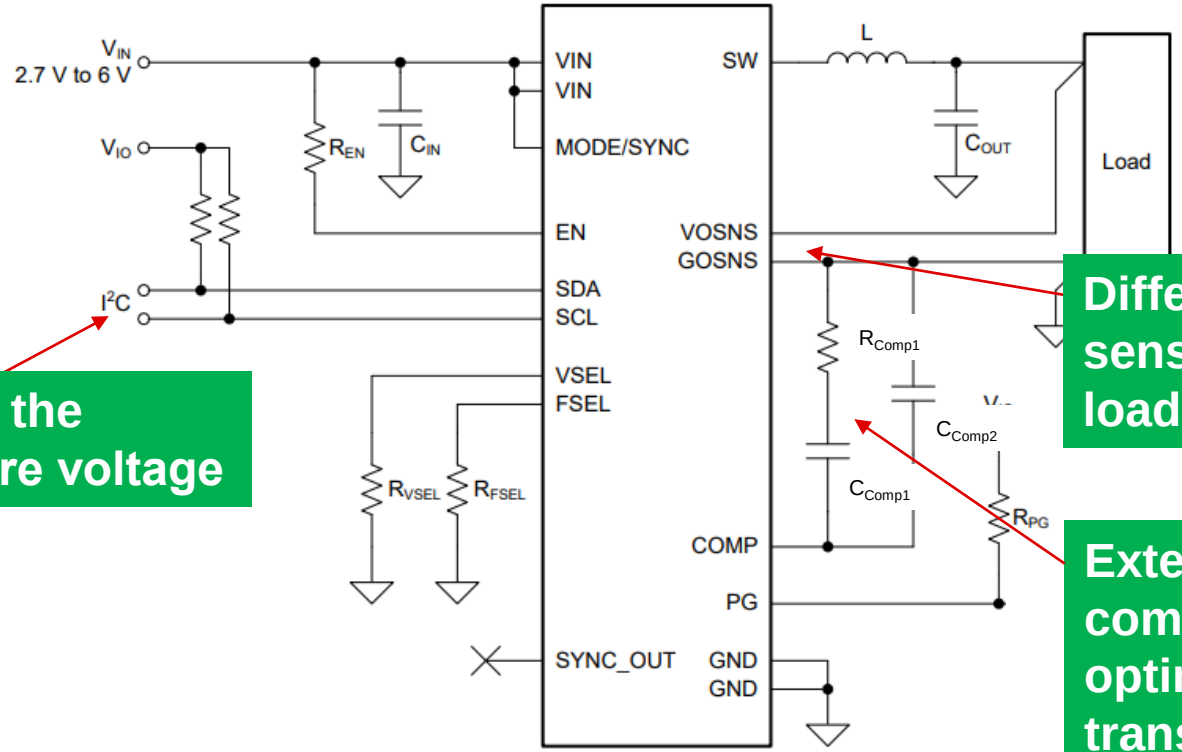
Design #1
Optimized load transient performance

Design #1 objective

- $3.3V_{IN}$ to $0.75V_{OUT}$ with ±3.3% total accuracy
  - Includes both AC (transient overshoot/undershoot, ripple) and DC accuracy (setpoint)
- 15A peak current, with ±7.5A (50%) load steps in 1µs
- Use the minimum amount of output capacitance required → smallest size and lowest cost

From the processor's specification for your specific use case

Typical application schematic with TPS62873 (15A)



I²C to fine-tune the processor's core voltage

Differential remote sense for excellent load regulation

External compensation to optimize the transient response

Circuit calculations – 2 options

D/S equations

10.2.1 Design Requirements

Table 10-1 lists the operating parameters for this application example.

Table 10-1. Design Parameters

Symbol	Parameter	Value
V_{IN}	Input voltage	3.3 V
V_{OUT}	Output voltage	0.75 V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±3.3%
TOL_{DC}	Output voltage tolerance of the TPS6287x (DC accuracy)	±1%
ΔI_{OUT}	Output current load step	±7.5 A
t_t	Load step transition time	1 µs
f_{SW}	Switching frequency	2.25 MHz
L	Inductance	110 nH
TOL_{IND}	Inductor tolerance	±20%
g_m	Error amplifier transconductance	1.5 mS
τ	Internal timing parameter	12.5 µs

Excel spreadsheet (link)

Latest version Version: 1.0.2 Release date: Mar 11, 2024

Downloads Supported products & hardware

TPSM8287AComponentCalculator.xlsx — 108 K

Design process

- List system parameters (V_{IN}, V_{OUT}, load step, L, f_{sw}, etc.)
- Type II compensation:
  - Calculate R_{Comp1} to meet load step → R_{Comp1} sets the required control loop gain
  - Calculate required minimum output capacitance to keep the loop stable → C_{OUT} decreases the loop bandwidth, which increases stability
  - Select specific capacitors
  - Select C_{Comp1} and C_{Comp2} to set pole and zero frequencies
- Build and test circuit

Using the Excel spreadsheet

123	Cells with this color are cells in which you must enter your application parameters.
123	Cells with this color are cells that display calculated values. Do not change the values in these cells.
123	Cells with this color are cells that contain fixed parameters. Do not change the values in these cells.

List system parameters

PARAMETER	SYMBOL	VALUE	UNIT	REMARKS
Number of Phases	#	1		Enter the number of TPSM8287Axx devices that are paralleled.
Input Voltage	V_{IN}	3.3	V	Enter the maximum input voltage.
Output Voltage	V_{OUT}	0.75	V	Enter the output voltage.
Load Current Step	$\Delta I_{OUT(step)}$	7.5	A	Enter the peak-to-peak load current step.
Maximum V_{OUT} Deviation	ΔV_{OUT}	2.3%		Enter the maximum allowable output voltage deviation during a load t…imum overall voltage t…e TPSM8287Axx device.
		17.3E-3	V	
Load Step Rise and Fall Time	t_r, t_f	1E-06	s	Enter the rise and fall time of the transient load step.
Error Amplifier Transconductance	g_m	1.5E-3	S	
Internal Timing Parameter	τ	12.5E-6	s	
Internal Timing Parameter Tolerance	TOL_{τ}	30%		
Switching Frequency	f_{SW}	2.25E+6	Hz	Enter the switching frequency: 1.5 MHz or 2.25 MHz.
Switching Frequency Tolerance	TOL_{fSW}	10%		
Inductance	L	110E-9	H	Enter the internal inductor value
Inductance Tolerance	TOL_{IND}	20%		
Maximum Bandwidth	BW_{max}	563E+3	Hz	
Recommended Bandwidth	BW	200E+3	Hz	
Target Bandwidth	BW_T	563E+3	Hz	Enter a target BW, between the values of the previous 2 cells. Values closer to 200 kHz are recommended for simpler designs.
Inductor Ripple Current	ΔI_L	2.3	A	This is the calculated ripple current in each inductor.
Total Inductor Current Step Change	$\Delta I_{OUT(max)}$	8.7	A	This is the total load step, once the inductor ripple current has been added to the load step current.

34.6mV window!

Calculate R_{Comp1}

Compensation Resistance (Calculated)	R_{Comp1}	1.82E+3	Ω	The is the minimum compensation resistance required to achieve the transient performance requirements.
Compensation Resistance (Used)	R_{Comp1}	2.00E+3	Ω	Enter the value of R_{Comp1} you will use. This value should be larger than the value calculated above.

- 2kΩ selected as a common value, above the calculated minimum

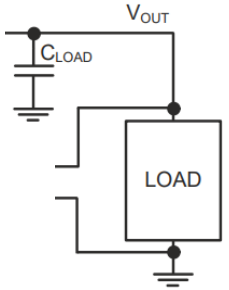
Calculate required minimum C_{OUT}

Minimum Output Capacitance (regulated case)	$C_{OUT(min)(reg)}$	177E-6	F	This is the minimum output capacitance required, assuming the loop remains in regulation under all conditions.
Minimum Output Capacitance (saturated case)	$C_{OUT(min)(sat)}$	123E-6	F	This is the minimum output capacitance required, assuming the loop saturates during a transient.
Minimum Output Capacitance (Calculated)	$C_{OUT(min)}$	177E-6	F	This is the minimum output capacitance required to achieve the specified transient performance. It is the maximum of the two values calculated above.
Minimum Output Capacitance (Used)	$C_{OUT(min)}$	180E-6	F	Enter the minimum capacitance used in the application. Its value must be greater than the minimum calculated output capacitance, taking into consideration, tolerance, temperature effects, DC bias, aging, etc.

$$C_{OUT(min)(reg)} = \left(\frac{\tau \times (1 + g_m \times R_Z)}{2 \times \pi \times \frac{L}{N\Phi} \times \frac{f_{SW}}{4}} \right) \left(1 + \sqrt{TOL_\tau{}^2 + TOL_{IND}{}^2 + TOL_{fSW}{}^2} \right)$$

tance

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}} \left(\frac{\frac{L}{N\Phi} \times \left(\Delta I_{OUT} + \frac{I_{L(PP)}}{2} \right)^2}{2 \times V_{OUT}} - \frac{\Delta I_{OUT} \times t_t}{2} \right) (1 + TOL_{IND})$$

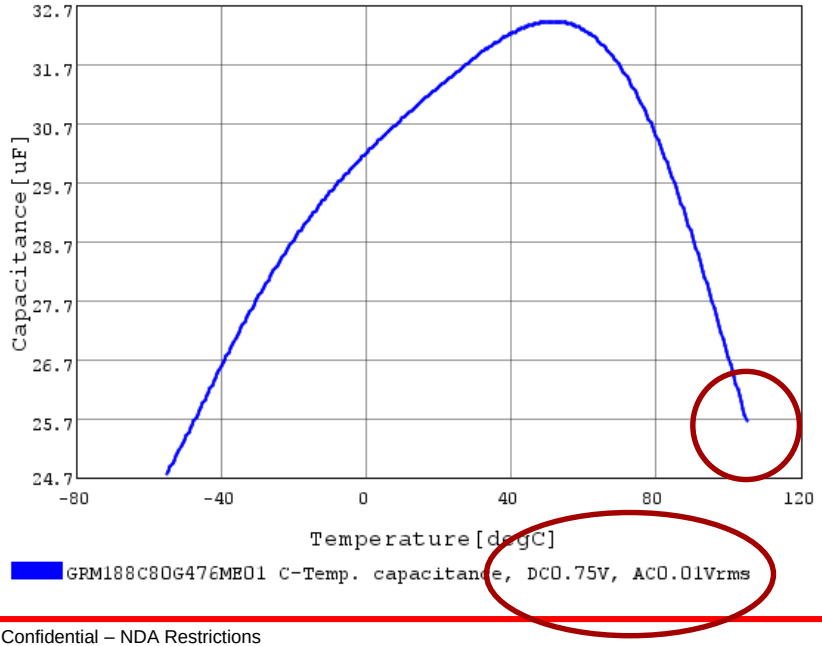


Select specific capacitors

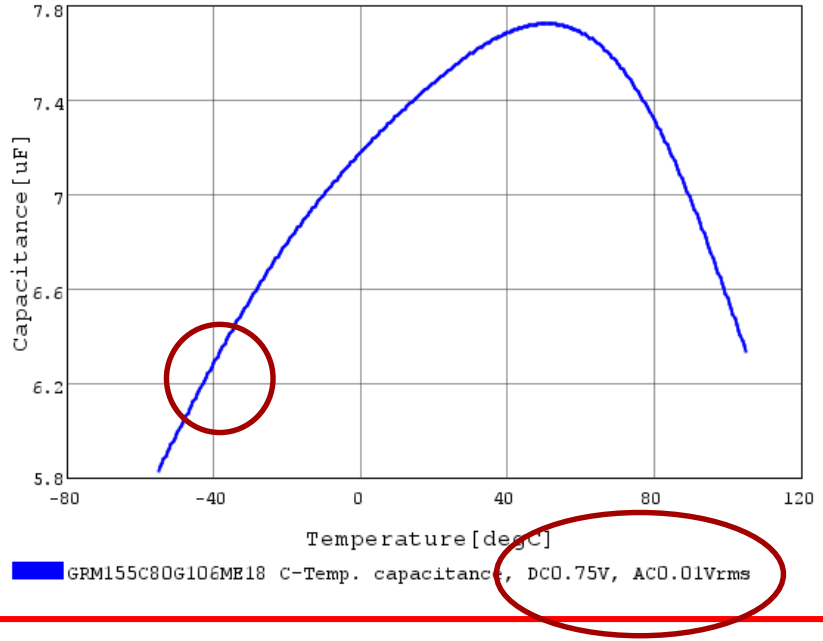
- Use GRM188C80G476ME01D (47µF) and GRM155C80G106ME18D (10µF)
- $C_{OUT\_IC} = 2 \times 47\mu F$
- $C_{LOAD} = 4 \times 47\mu F + 4 \times 10\mu F$
- Use capacitor vendor's simulation tool to estimate effective capacitance over DC bias, AC bias (ripple), and temperature

Effective capacitance simulations

GRM188C80G476ME01D



GRM155C80G106ME18D

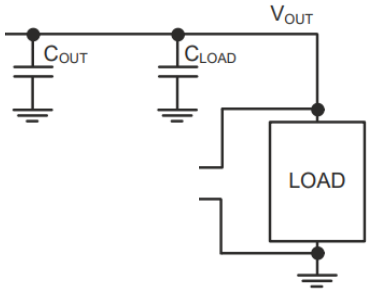


Select specific capacitors

C26 =6*0.0000257+4*0.0000062

	A	B	C	D	E
23	Minimum Output Capacitance (regulated case)	$C_{OUT(min)(reg)}$	177E-6	F	This is the minimum output capacitance required, assuming the loop remains in regulation under all conditions.
24	Minimum Output Capacitance (saturated case)	$C_{OUT(min)(sat)}$	123E-6	F	This is the minimum output capacitance required, assuming the loop saturates during a transient.
25	Minimum Output Capacitance (Calculated)	$C_{OUT(min)}$	177E-6	F	This is the minimum output capacitance required to achieve the specified transient performance. It is the maximum of the two values calculated above.
26	Minimum Output Capacitance (Used)	$C_{OUT(min)}$	179E-6	F	Enter the minimum capacitance used in the application. Its value must be greater than the minimum calculated output capacitance, taking into consideration, tolerance, temperature effects, DC bias, aging, etc.

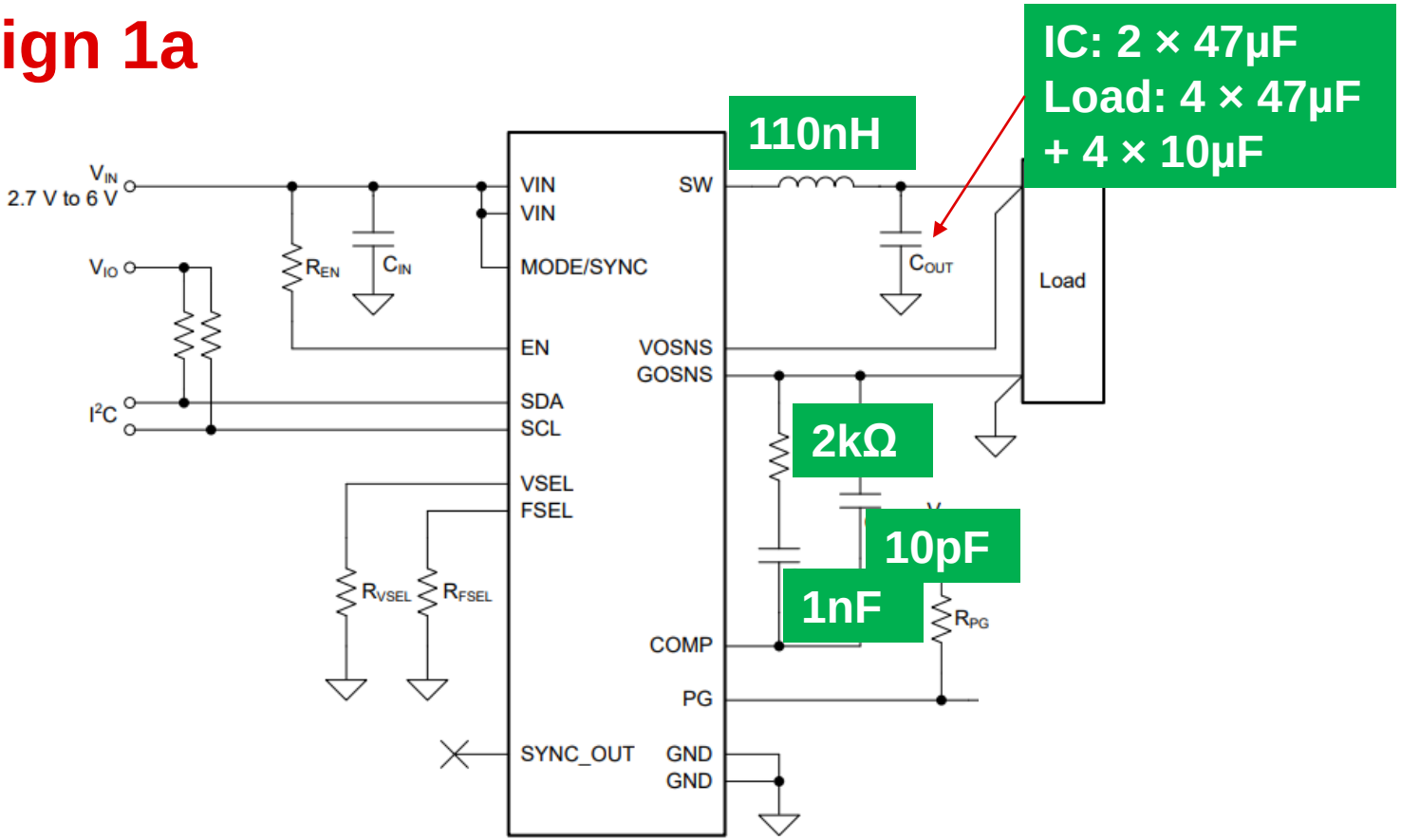
- 179µF of effective capacitance chosen
- Total $C_{OUT} = C_{OUT\_IC} + C_{LOAD}$
- $C_{LOAD} > 2 \times C_{OUT\_IC}$



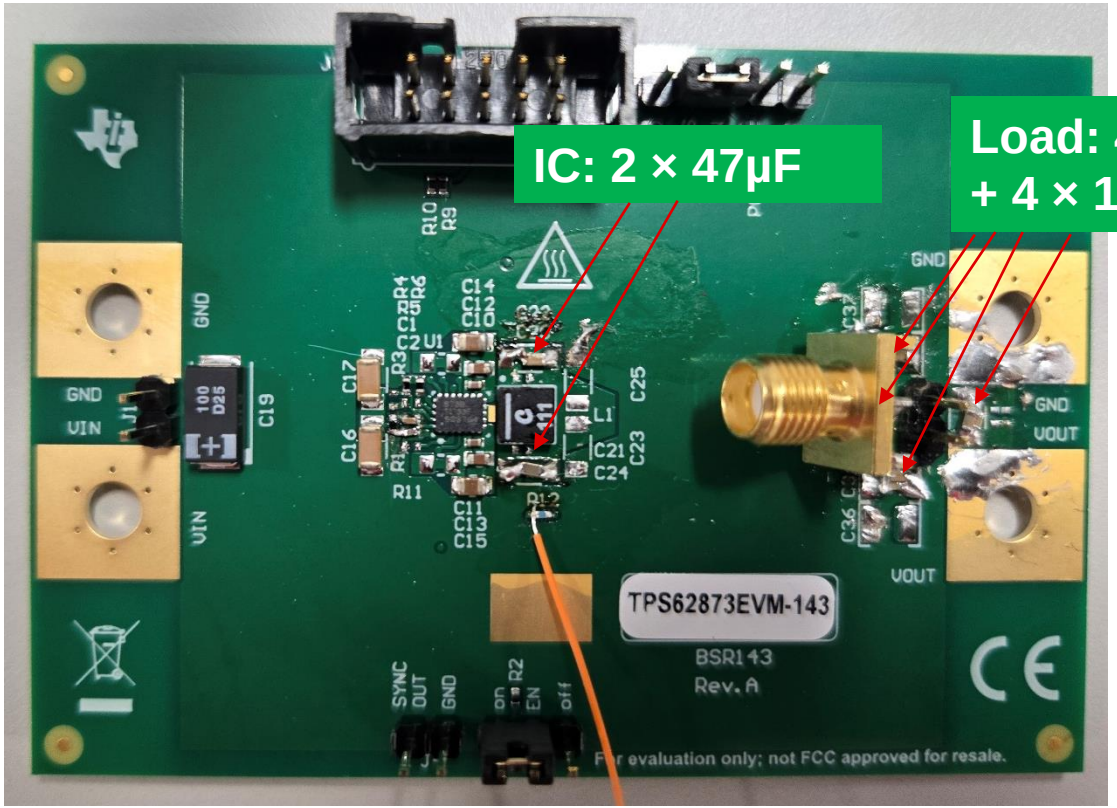
Select C_{Comp1} and C_{Comp2}

Inner Loop Cutoff Frequency	BW_{INNER}	101.0E+3	Hz	
Primary Compensation Capacitance (Calculated)	C_{Comp1}	1.1E-9	F	This is the calculated primary compensation capacitance value.
Primary Compensation Capacitance (Used)	C_{Comp1}	1.0E-9	F	Enter the value of C_{Comp1} you will use. This value should be the closest standard value to the value calculated above.
Secondary Compensation Capacitance	C_{Comp2}	10E-12	F	Enter the value of C_{Comp2} you will use. The purpose of this capacitor is to bypass high frequency noise away from the COMP pin. Its value is not critical, and 10 pF is suitable for most applications.
Secondary Compensation Capacitance Pole	f_{pole}	8.0E+6	Hz	This is the calculated frequency of the pole created by C_{Comp2}.
Bandwidth	BW	808E+3	Hz	This is the calculated bandwidth of the converter using the above component values.

Final design 1a



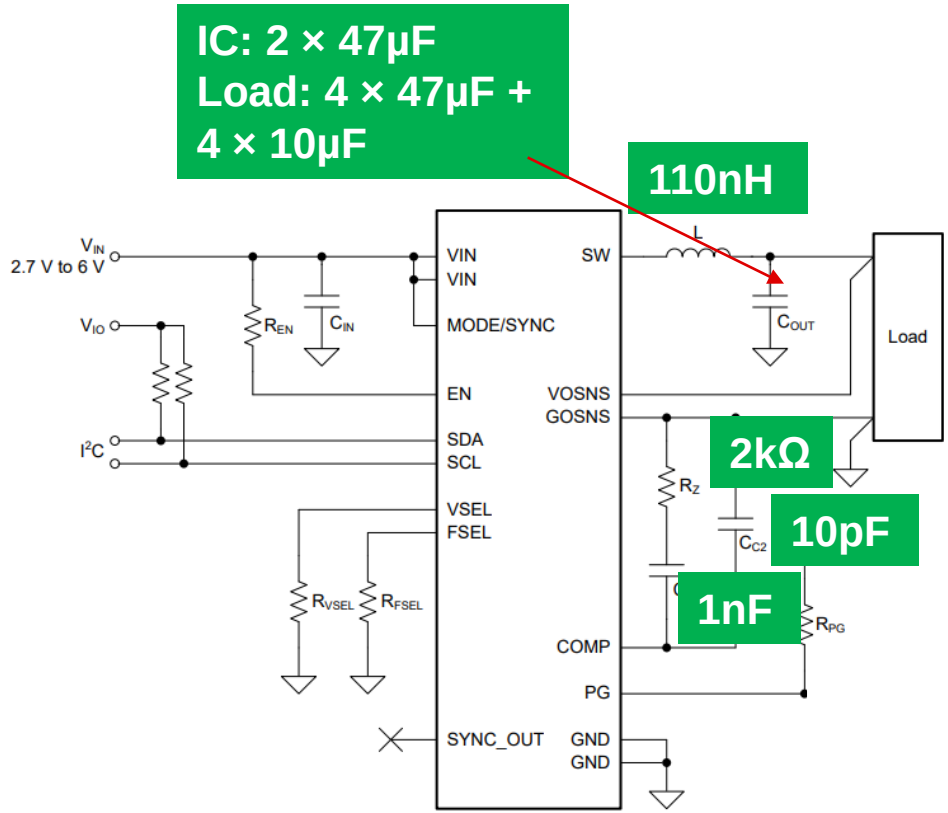
Final design 1



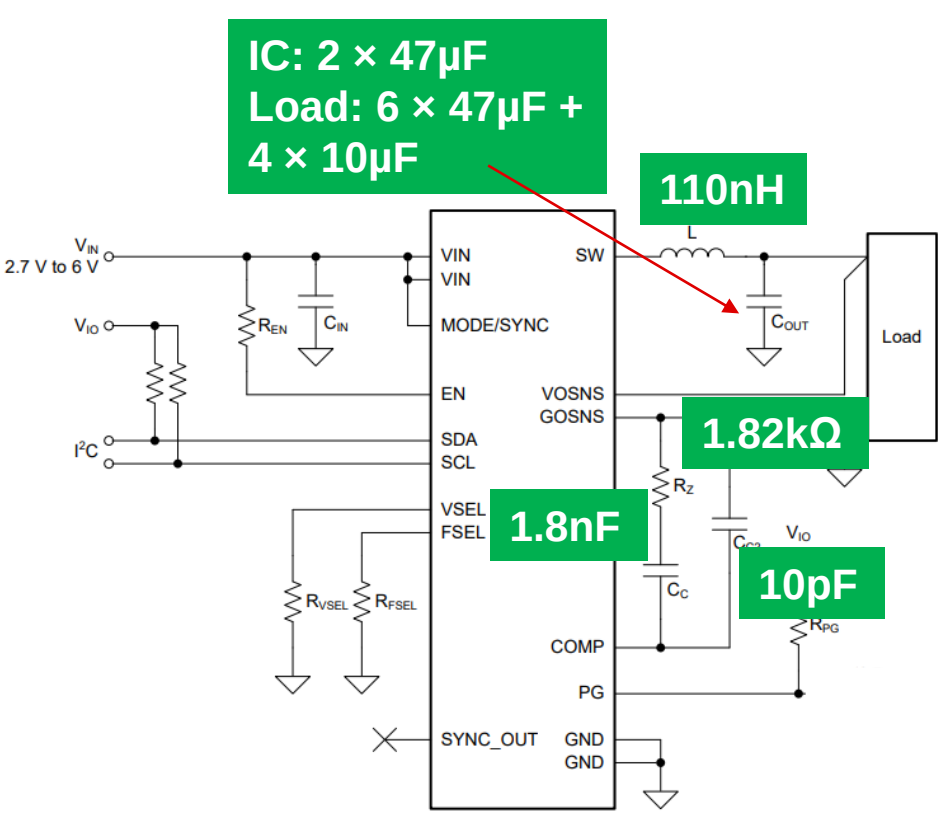
Design meets the performance objectives

- Design 1a meets requirements but still needs further adjustments → **Design 1b**
- Phase margin (28°) is low → more C_{OUT} and/or lower R_{Comp1}
- Design tweaks:
  - R_{Comp1} → 1.82kΩ
  - C_{LOAD} → add 2 × 47µF
  - C_{Comp1} → 1.8nF

Final design 1a



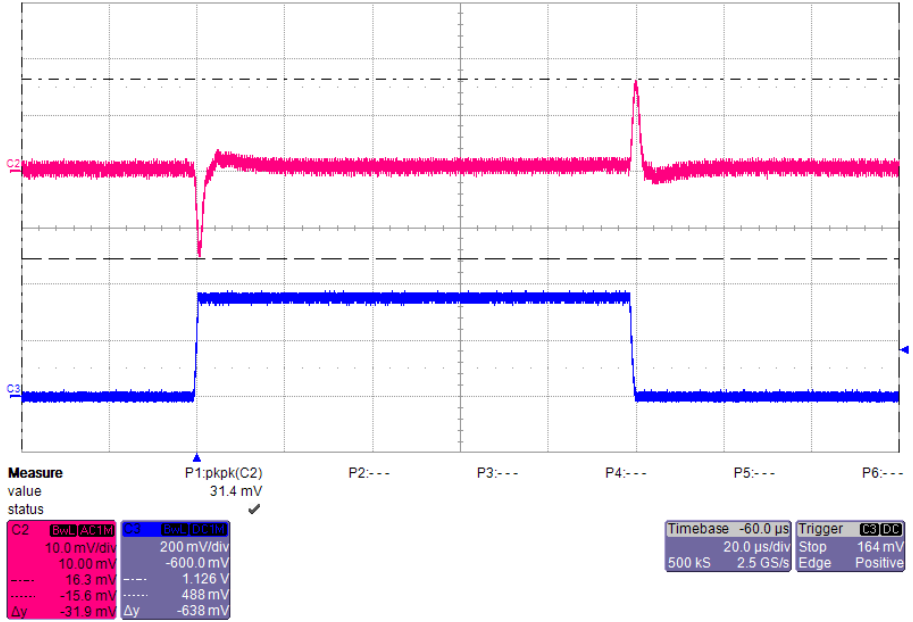
Final design 1b



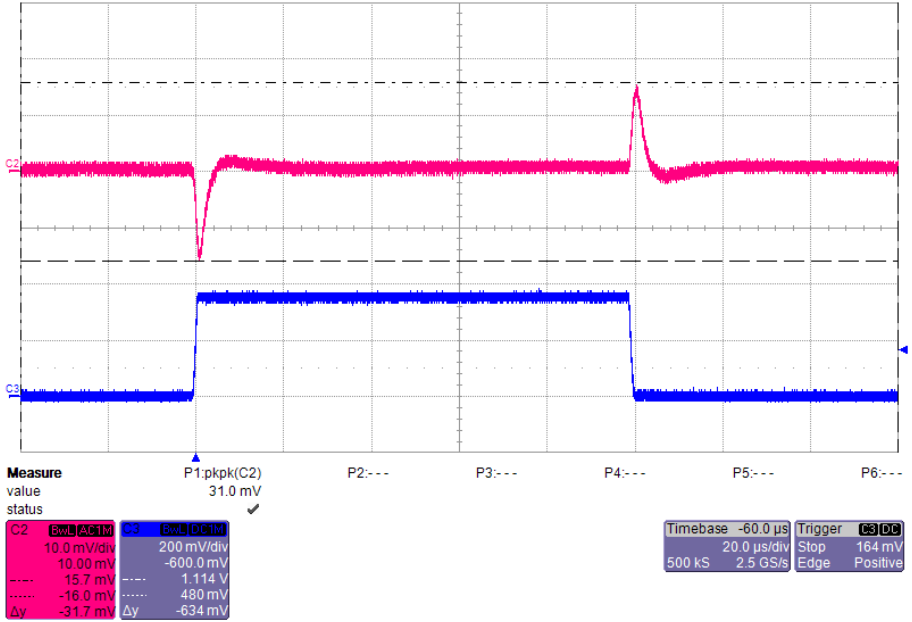
Load transient results

Vout (AC)
Iload (4A/div)

Final design 1a

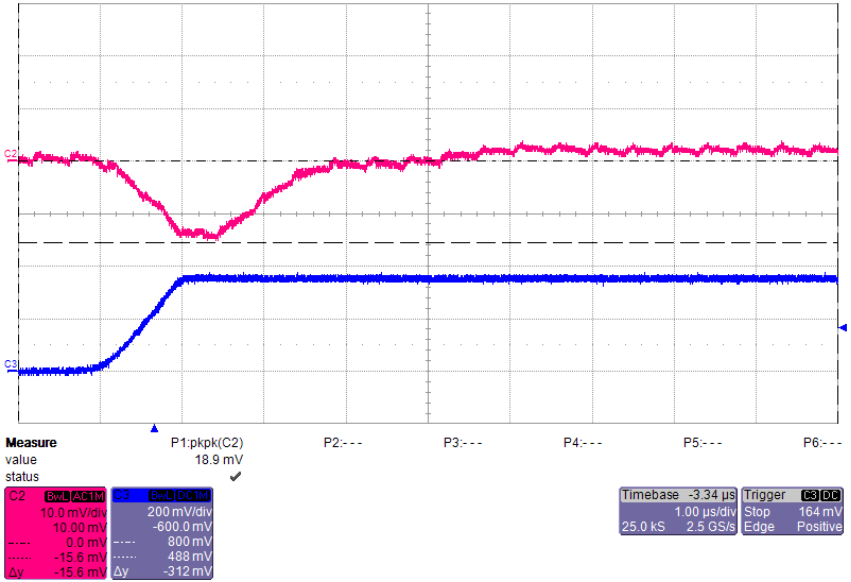


Final design 1b

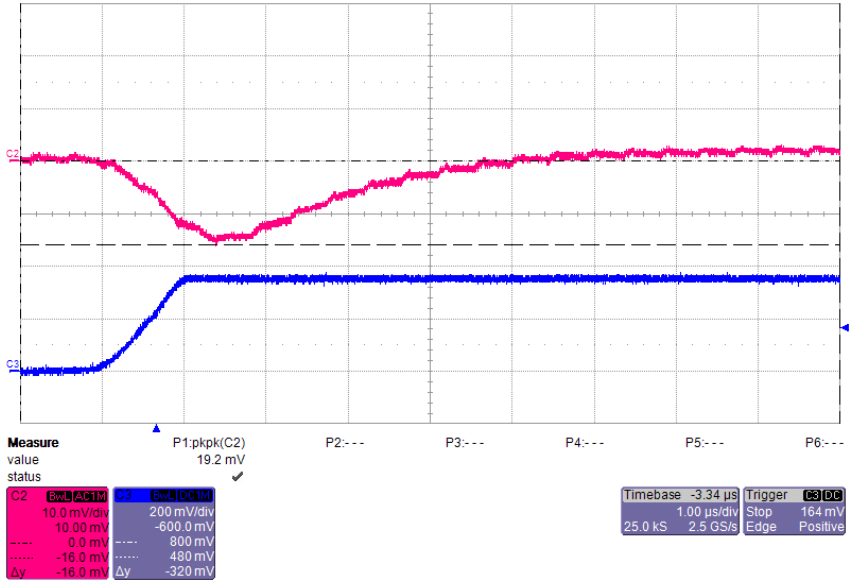


Load transient results - rising edge

Final design 1a

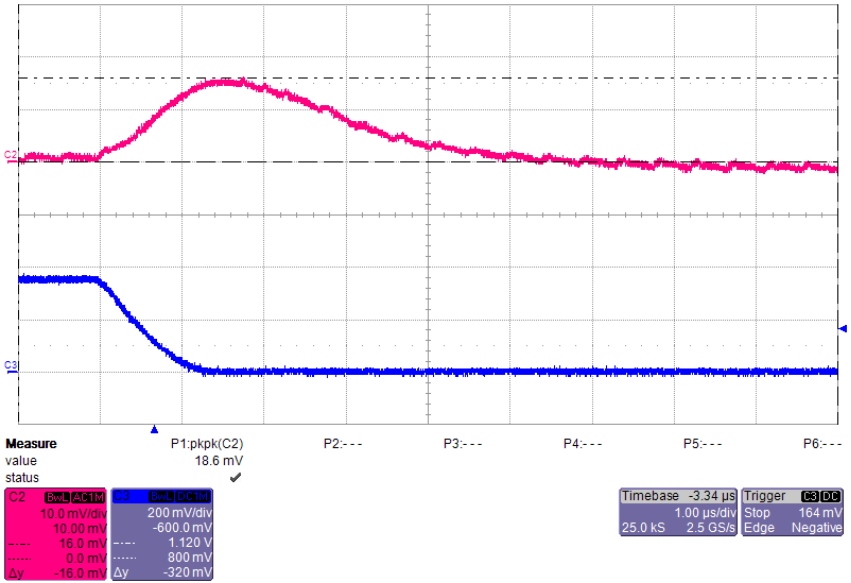


Final design 1b

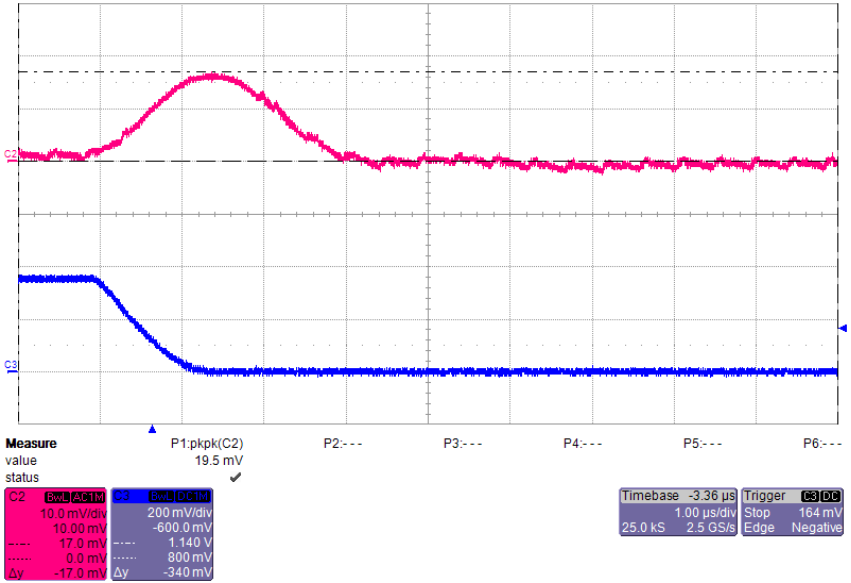


Load transient results - falling edge

Final design 1a

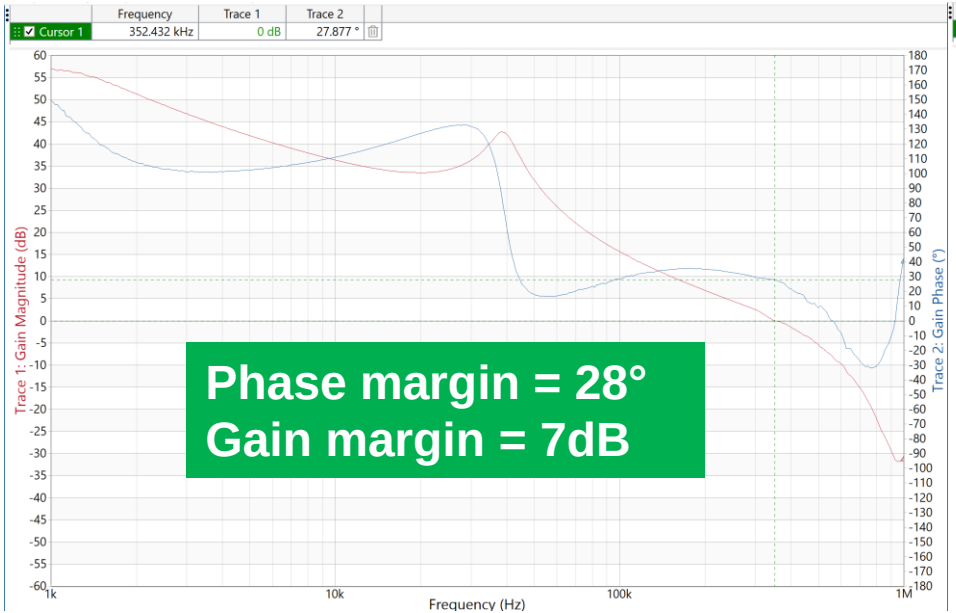


Final design 1b

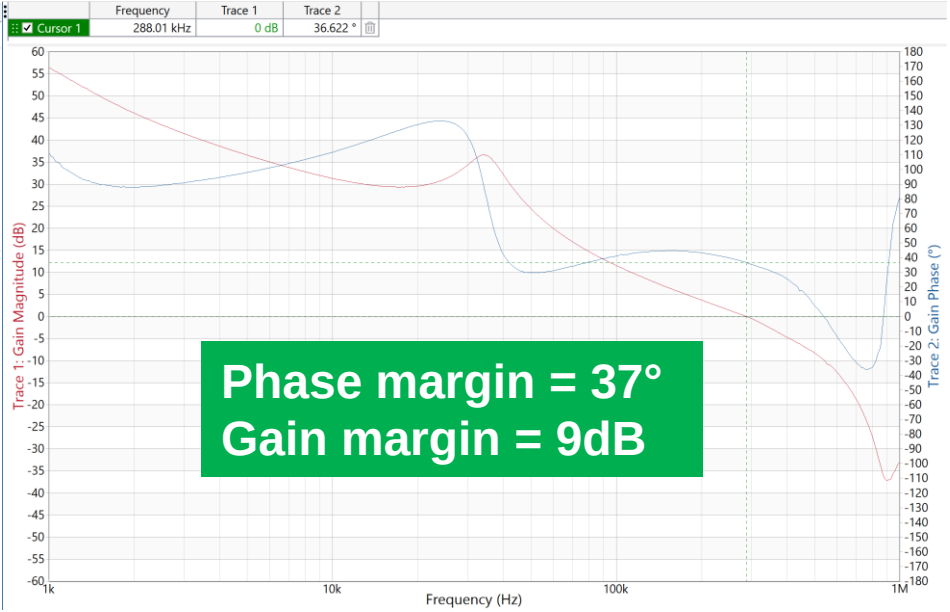


Bode plot (loop stability, 15A load)

Final design 1a

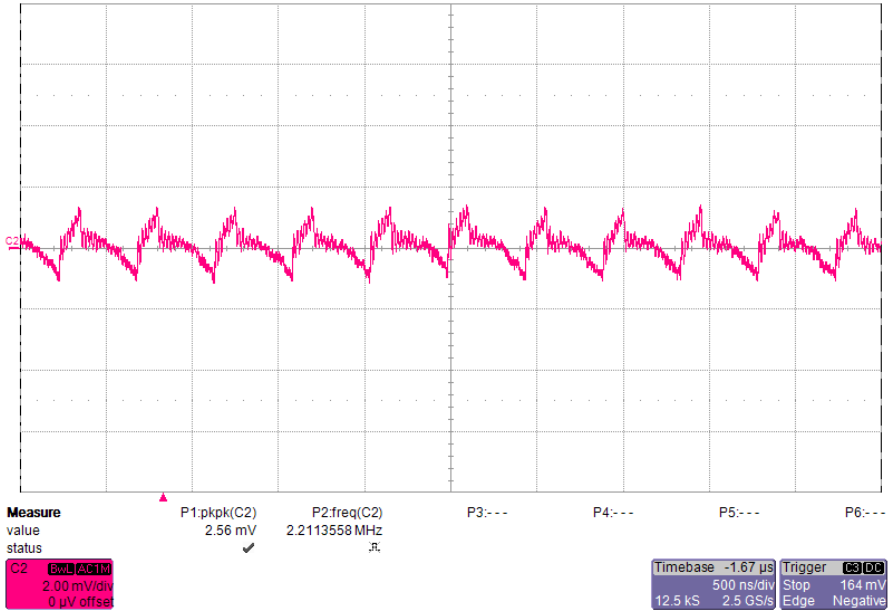


Final design 1b

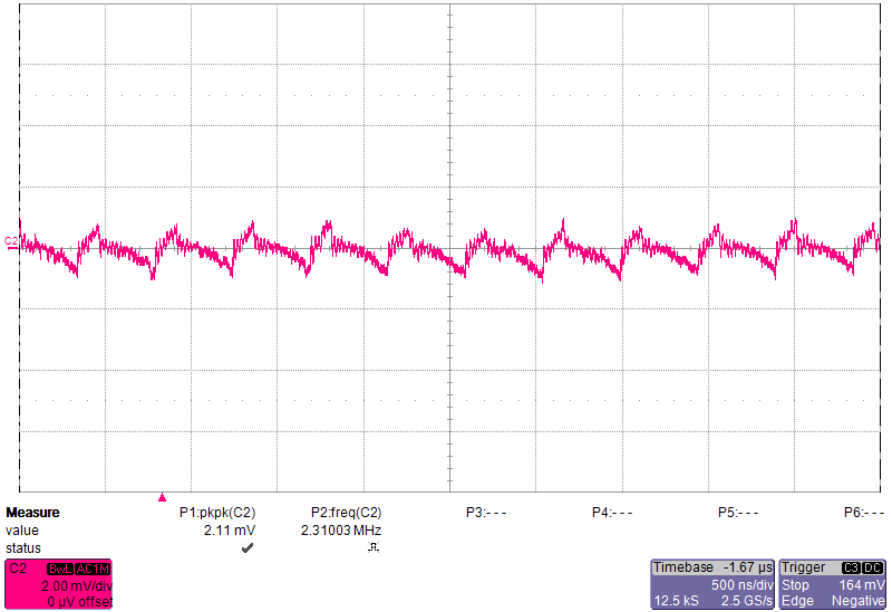


Output voltage ripple (15A load)

Final design 1a



Final design 1b



Design summary

- Design 1a:
  - Transient response: 31.9mVp-p
  - Ripple: 2.56mVp-p
  - Bode plot: 352kHz BW, 28° phase margin, 7dB gain margin
  - Output capacitors: 6 × 0603 + 4 × 0402
- Design 1b:
  - Transient response: 31.7mVp-p
  - Ripple: 2.11mVp-p
  - Bode plot: 288kHz BW, 37° phase margin, 9dB gain margin
  - Output capacitors: 8 × 0603 + 4 × 0402

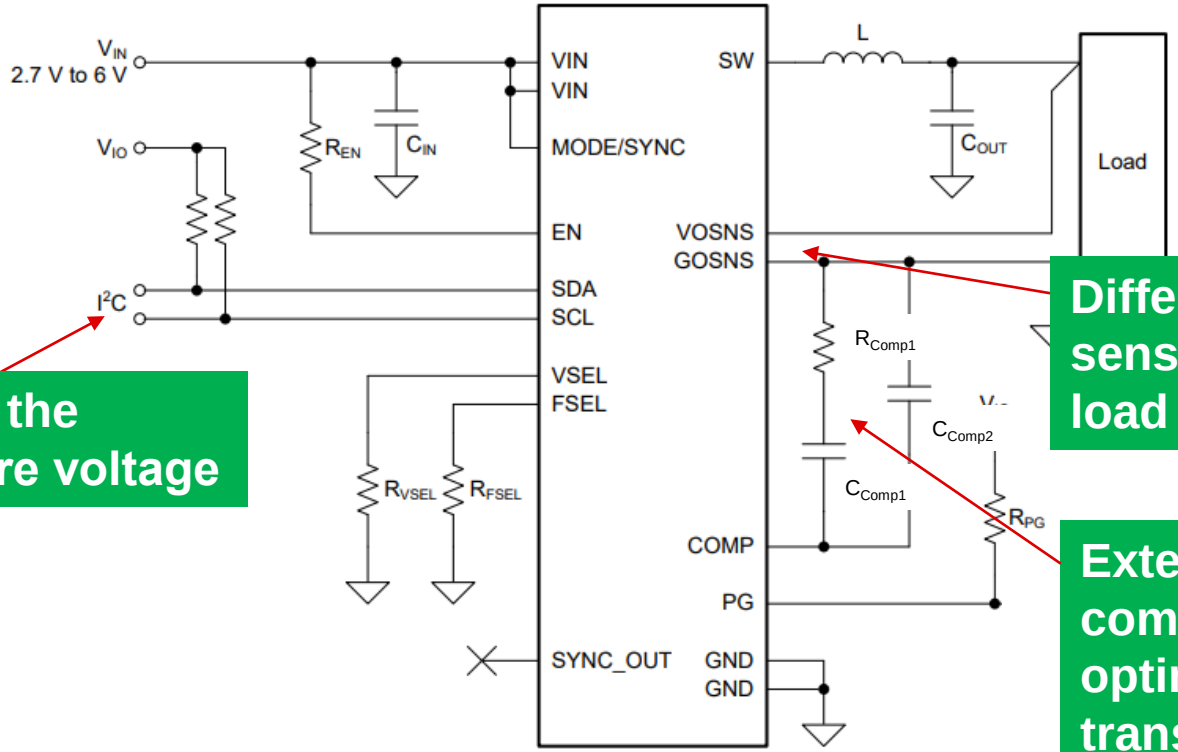
Q&A

Design #2
Optimized for smallest size

Design #2 objective

- $3.3V_{IN}$ to $0.75V_{OUT}$ with the smallest size
  - No transient response requirement
- 15A peak current
- Use the minimum amount of output capacitance required

Typical application schematic with TPS62873 (15A)



I²C to fine-tune the processor's core voltage

Differential remote sense for excellent load regulation

External compensation to optimize the transient response

Design process

- List system parameters (V_{IN}, V_{OUT}, L, f_{sw}, etc.)
- Type II compensation:
  - Select the output capacitors and compute their effective output capacitance
  - Calculate the maximum value of R_{Comp1} to require less than this much C_{OUT} → R_{Comp1} sets the required control loop gain
  - Select C_{Comp1} and C_{Comp2} to set pole and zero frequencies
- Build and test circuit

List system parameters

Set to a very low level

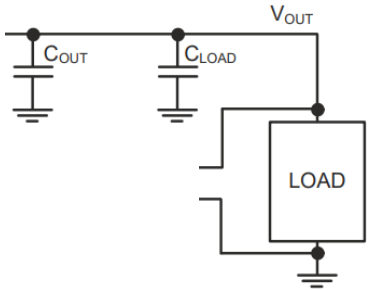
Set to a very high level

Same f_{sw}, L, and BW

PARAMETER	SYMBOL	VALUE	UNIT
Number of Phases	#	1	
Input Voltage	V_{IN}	3.3	V
Output Voltage	V_{OUT}	0.75	V
Load Current Step	$\Delta I_{OUT(step)}$	1	A
Maximum V_{OUT} Deviation	ΔV_{OUT}	5.0%	
		37.5E-3	V
Load Step Rise and Fall Time	t_r, t_f	1E-06	s
Error Amplifier Transconductance	g_m	1.5E-3	S
Internal Timing Parameter	τ	12.5E-6	s
Internal Timing Parameter Tolerance	TOL_{τ}	30%	
Switching Frequency	f_{SW}	2.25E+6	Hz
Switching Frequency Tolerance	TOL_{fSW}	10%	
Inductance	L	110E-9	H
Inductance Tolerance	TOL_{IND}	20%	
Maximum Bandwidth	BW_{max}	563E+3	Hz
Recommended Bandwidth	BW	200E+3	Hz
Target Bandwidth	BW_T	563E+3	Hz

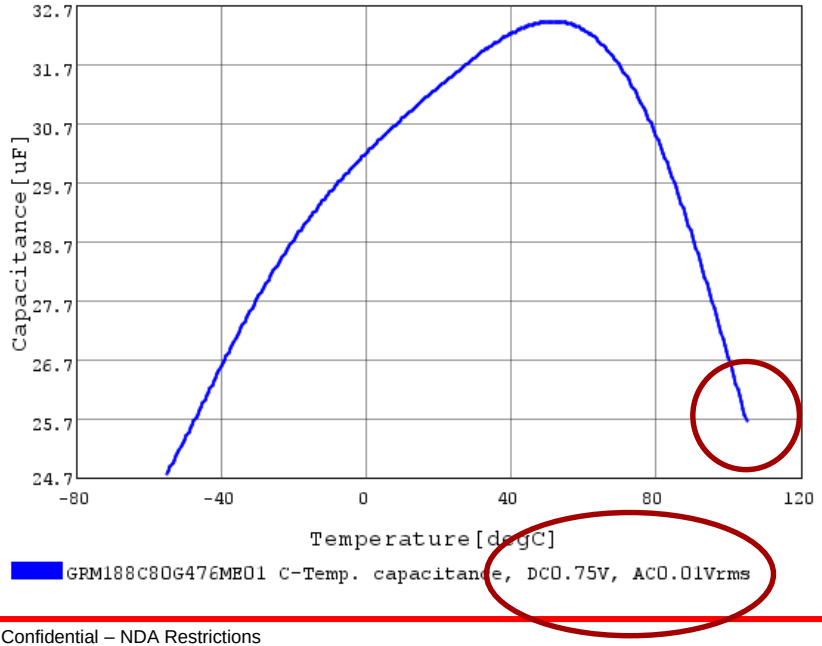
Select specific capacitors

- Use GRM188C80G476ME01D (47µF) and GRM155C80G106ME18D (10µF) and GRM188C81A226ME01D (22µF)
- $C_{OUT\_IC} = 2 \times 22\mu F$
- $C_{LOAD} = 2 \times 47\mu F + 2 \times 10\mu F$
- Use capacitor vendor's simulation tool to estimate effective capacitance over DC bias, AC bias (ripple), and temperature
- Total $C_{OUT} = C_{OUT\_IC} + C_{LOAD}$
- $C_{LOAD} > 2 \times C_{OUT\_IC}$

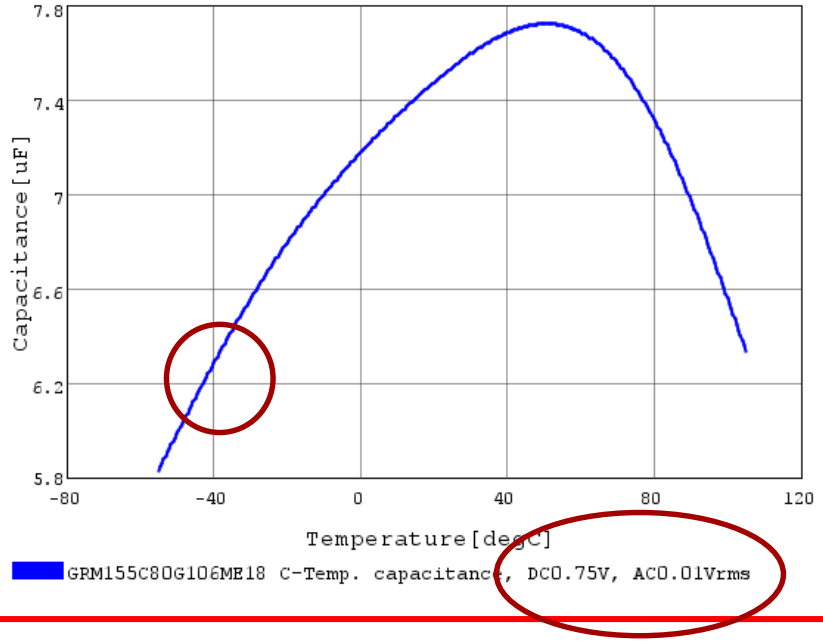


Effective capacitance simulations

GRM188C80G476ME01D

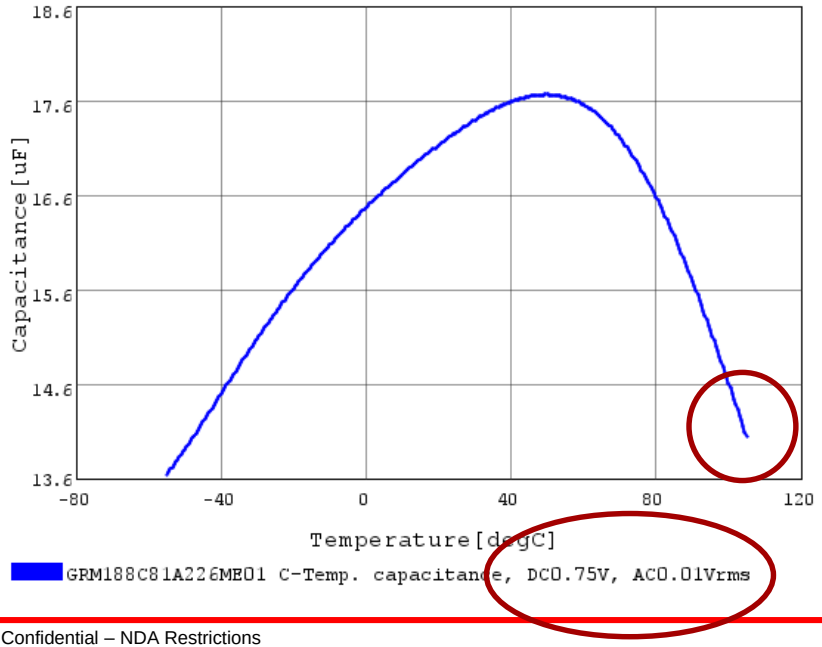


GRM155C80G106ME18D



Effective capacitance simulations

GRM188C81A226ME01D



Previous capacitors

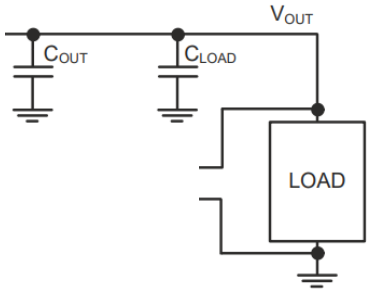
- GRM188C80G476ME01D = 25.7µF
- GRM155C80G106ME18D = 6.2µF

Select specific capacitors

C26 | =2*0.000014+2*0.0000257+2*0.0000062

	A	B	C	D	E
26	Minimum Output Capacitance (Used)	$C_{OUT(min)}$	92E-6	F	Enter the minimum capacitance used in the application. Its value must be greater than the minimum calculated output capacitance, taking into consideration, tolerance, temperature effects, DC bias, aging, etc.

- 92µF of <u>effective</u> capacitance chosen
- Total $C_{OUT} = C_{OUT\_IC} + C_{LOAD}$
- $C_{LOAD} > 2 \times C_{OUT\_IC}$



Calculate R_{Comp1}

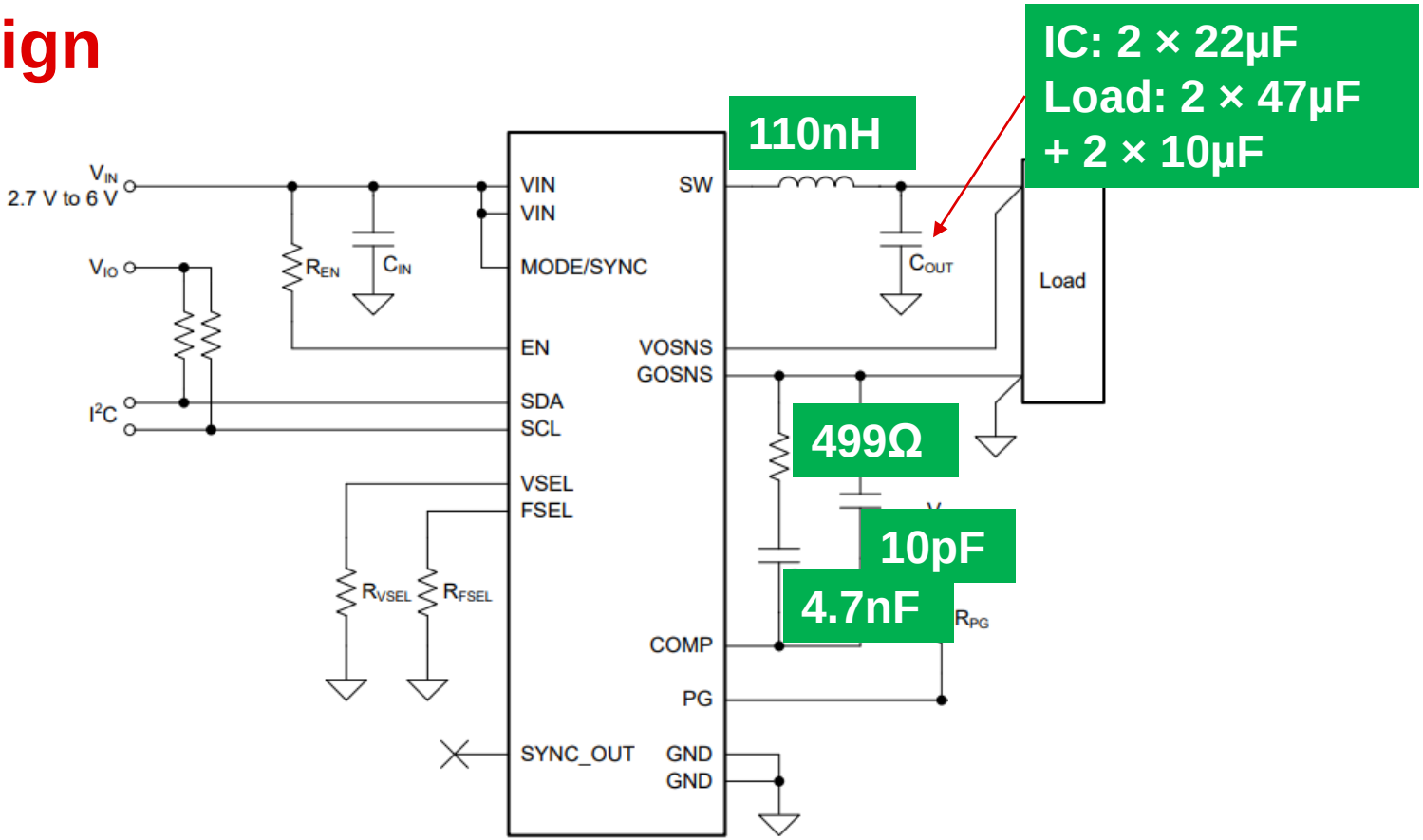
Compensation Resistance (Used)	R_{Comp1}	499.00E+0	Ω	Enter the value of R_{Comp1} you will use. This value should be larger than the value calculated above.
Minimum Output Capacitance (regulated case)	$C_{OUT(min)(reg)}$	77E-6	F	This is the minimum output capacitance required, assuming the loop remains in regulation under all conditions.
Minimum Output Capacitance (saturated case)	$C_{OUT(min)(sat)}$	-5E-6	F	This is the minimum output capacitance required, assuming the loop saturates during a transient.
Minimum Output Capacitance (Calculated)	$C_{OUT(min)}$	77E-6	F	This is the minimum output capacitance required to achieve the specified transient performance. It is the maximum of the two values calculated above.
Minimum Output Capacitance (Used)	$C_{OUT(min)}$	92E-6	F	Enter the minimum capacitance used in the application. Its value must be greater than the minimum calculated output capacitance, taking into consideration, tolerance, temperature effects, DC bias, aging, etc.

- Empirically select an R_{Comp1} that gives a recommended $C_{OUT(min)}$ about 20% below the entered $C_{OUT(min)}$
- Reducing R_{Comp1} reduces the recommended $C_{OUT(min)}$

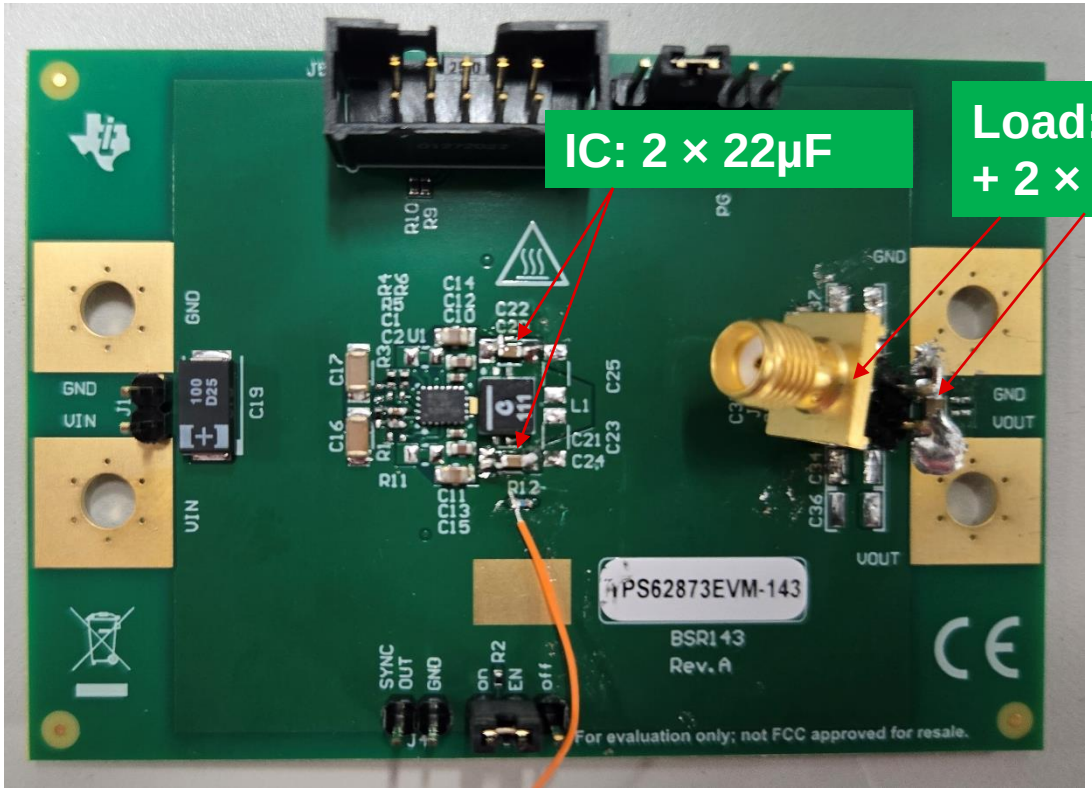
Select C_{Comp1} and C_{Comp2}

Inner Loop Cutoff Frequency	BW_{INNER}	197.0E+3	Hz	
Primary Compensation Capacitance (Calculated)	C_{Comp1}	4.8E-9	F	This is the calculated primary compensation capacitance value.
Primary Compensation Capacitance (Used)	C_{Comp1}	4.7E-9	F	Enter the value of C_{Comp1} you will use. This value should be the closest standard value to the value calculated above.
Secondary Compensation Capacitance	C_{Comp2}	10E-12	F	Enter the value of C_{Comp2} you will use. The purpose of this capacitor is to bypass high frequency noise away from the COMP pin. Its value is not critical, and 10 pF is suitable for most applications.
Secondary Compensation Capacitance Pole	f_{pole}	31.9E+6	Hz	This is the calculated frequency of the pole created by C_{Comp2}.
Bandwidth	BW	689E+3	Hz	This is the calculated bandwidth of the converter using the above component values.

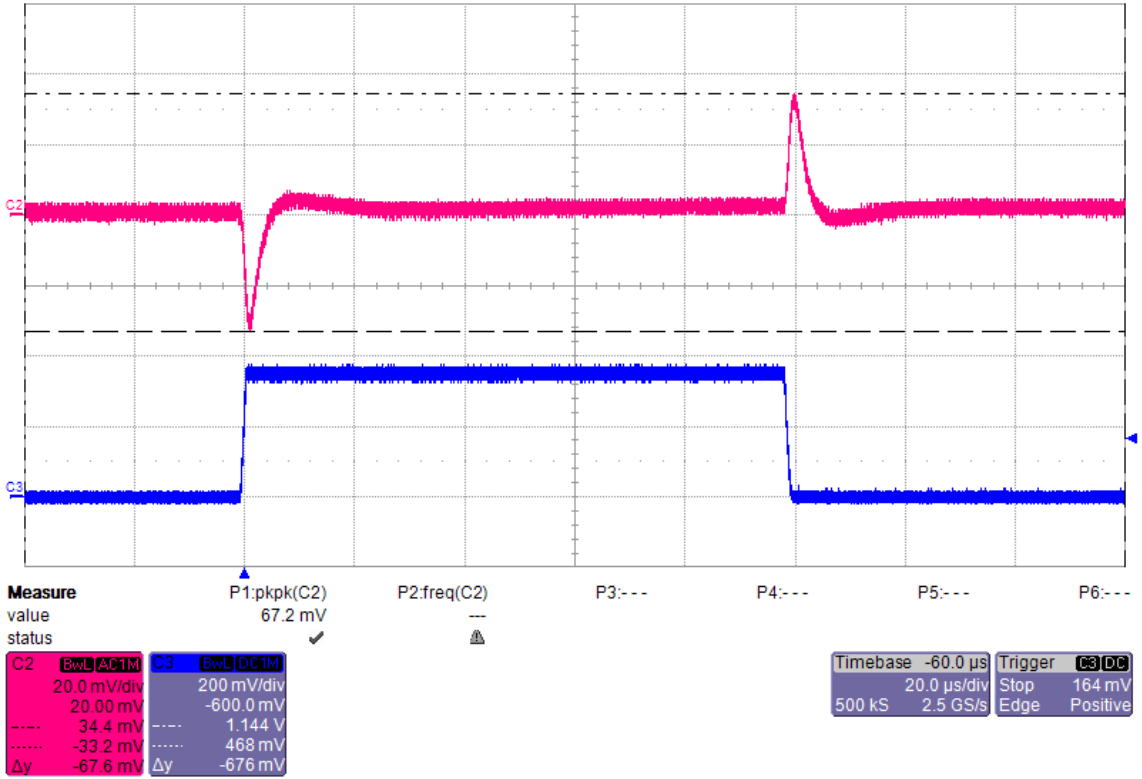
Final design



Final design

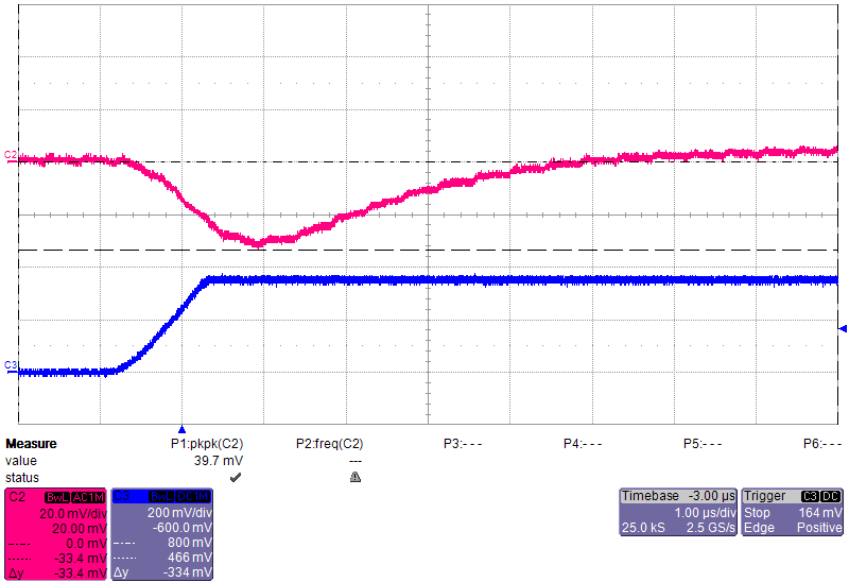


Load transient results

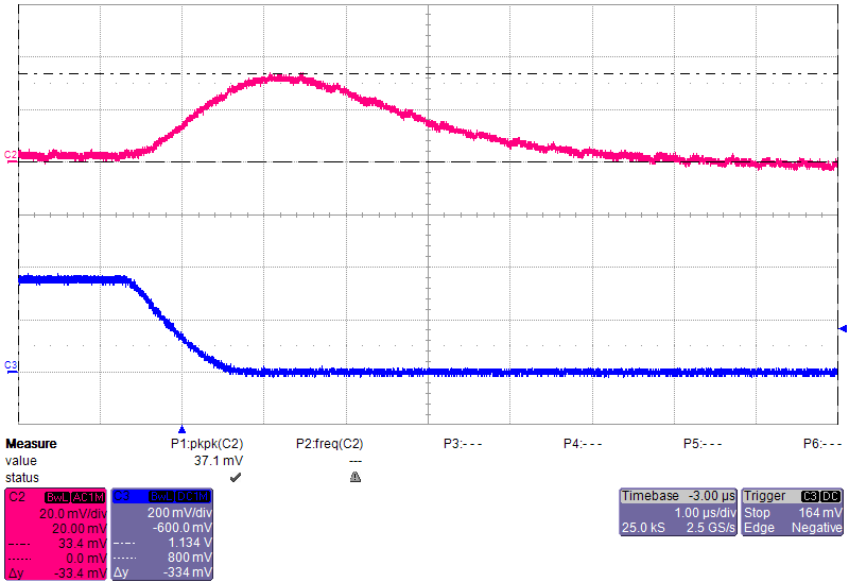


Load transient results

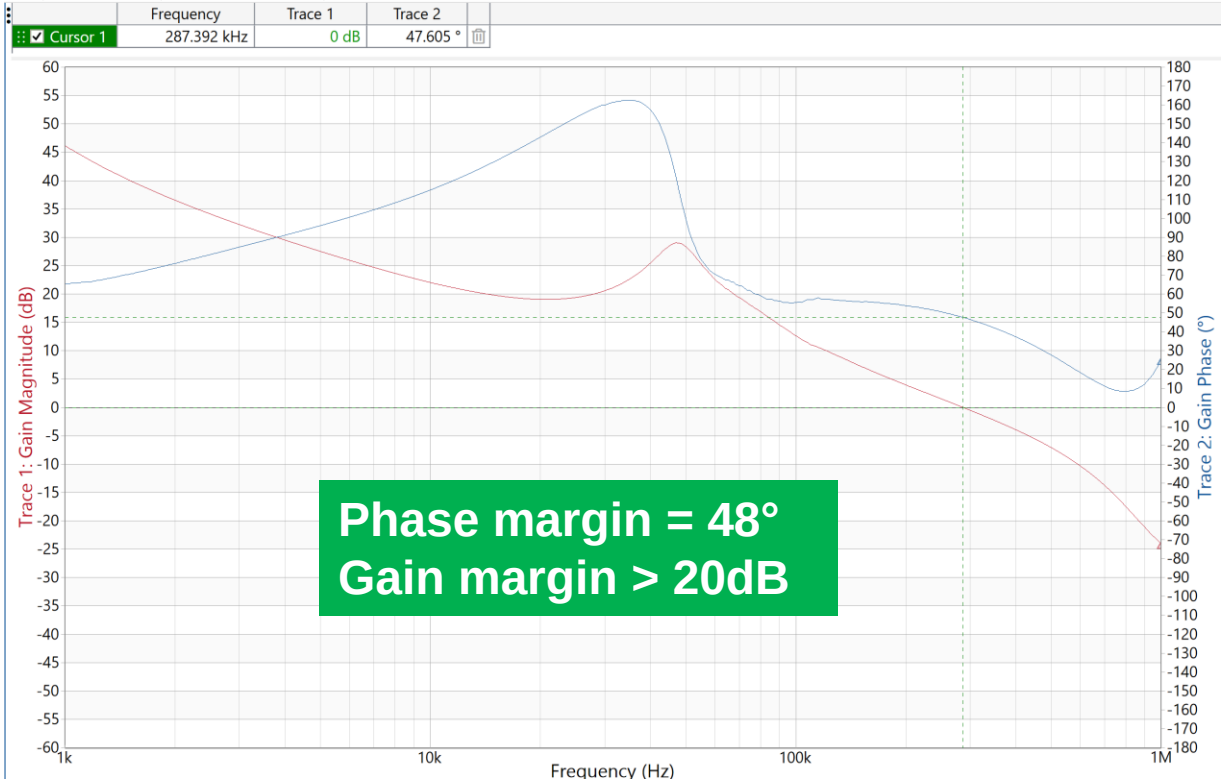
Rising edge



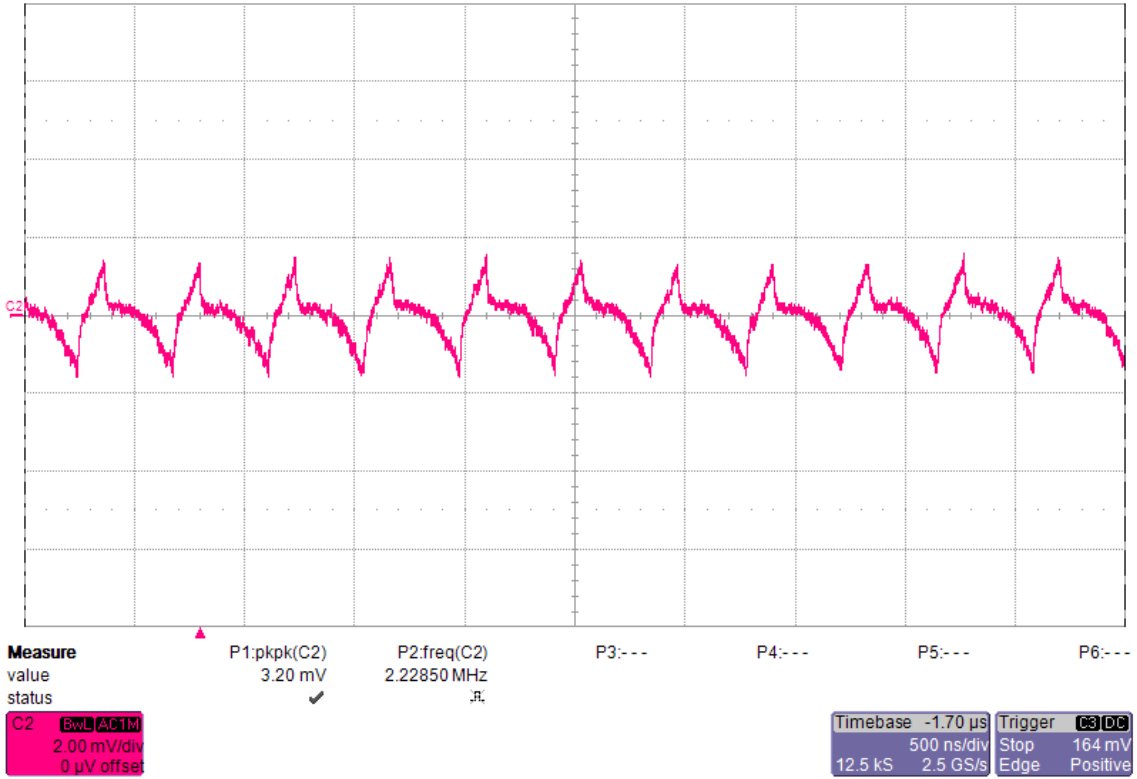
Falling edge



Bode plot (loop stability, 15A load)



Output voltage ripple (15A load)

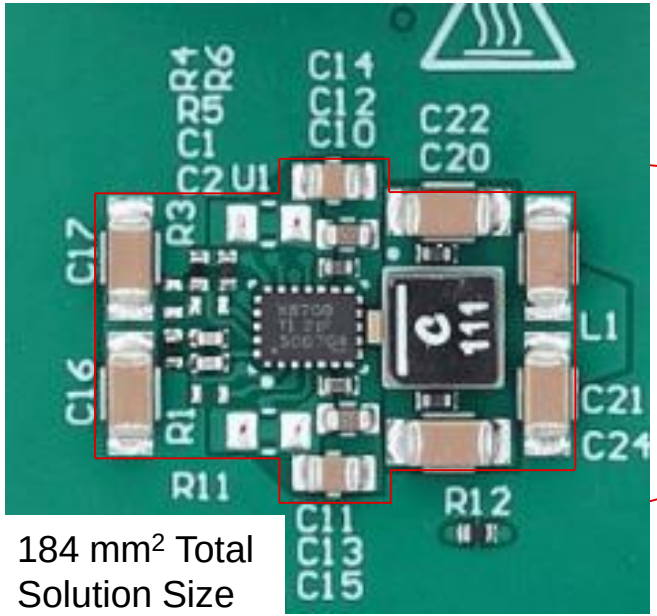


Design summary

- Design 2:
  - Transient response: 67.6mVp-p
  - Ripple: 3.20mVp-p
  - Bode plot: 287kHz BW, 48° phase margin, > 20dB gain margin
  - Output capacitors: 4 × 0603 + 2 × 0402

Power module gives a 58% smaller solution size

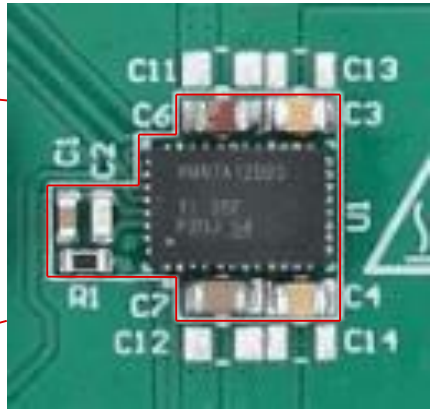
TPS62873EVM-143



184 mm^2 Total Solution Size

Component count: 19

TPSM8287A15BBHEVM



77 mm^2 Total Solution Size

Component count: 8

Q&A

Design #3

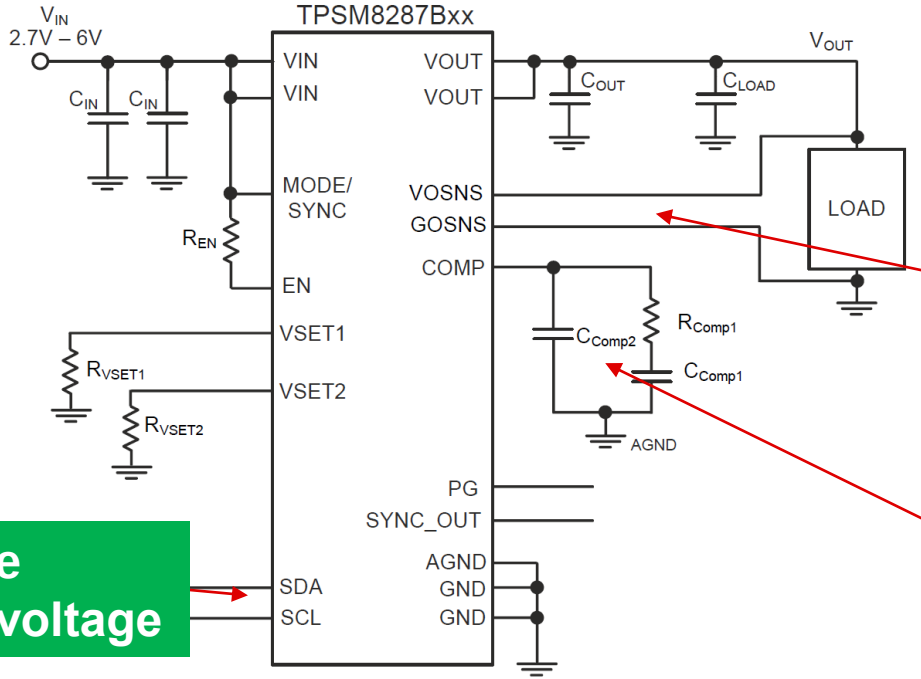
Optimized for smallest size &load transient performance

Using droop compensation and a power module

Design #3 objective

- $3.3V_{IN}$ to $0.75V_{OUT}$ with ±3.3% total accuracy
  - Includes both AC (transients, ripple) and DC accuracy (setpoint)
- 15A peak current, with ±7.5A (50%) load steps in 1µs
- Use the minimum amount of output capacitance required → smallest size and lowest cost

Typical schematic with TPSM8287B30 (30A)



TPSM8287Bxx Simplified Schematic

Differential remote sense for excellent load regulation

I²C to fine-tune the processor's core voltage

External compensation to optimize the transient response

Circuit calculations – 2 options

D/S equations

9.2.1 Design Requirements

The following table lists the operating parameters for this application example with the TPSM8287B30xx device.

Table 9-2. Design Parameters

SYMBOL	PARAMETER	VALUE
V_{IN}	Input voltage	2.7V – 6.0V
V_{OUT}	Output voltage	0.60V
TOL_{VOUT}	Output voltage tolerance allowed by the application	±5.0%
TOL_{DC}	Output voltage tolerance of the TPSM8287Bxx (DC accuracy)	±0.8%
$\Delta I_{OUT(step)}$	Output current load step	±3.0A
t_t	Load step transition time	1µs
f_{SW}	Switching frequency	1.5MHz
L	Integrated inductor	50nH
TOL_{IND}	Integrated inductor tolerance	±20%
g_m	Error amplifier transconductance	1.5mS
τ	Emulated current time constant	12.5µs
BW_f	Target loop bandwidth	200kHz
N_Φ	Number of paralleled devices (phases)	1
k_{BW}	Ratio of switching frequency to converter bandwidth (must be ≥ 4)	4

Excel spreadsheet (link)

Latest version Version: 1.0.0 Release date: Mar 7, 2025

Downloads Supported products & hardware

TPSM8287BComponentCalculator.xlsx — 110 K

Design process

- List system parameters (V_{IN}, V_{OUT}, load step, etc.)
- Type II compensation:
  - Calculate R_{Comp1} to meet load step → R_{Comp1} sets the required control loop gain
  - Calculate required minimum output capacitance to keep the loop stable → C_{OUT} decreases the loop bandwidth, which increases stability
  - Select specific capacitors
  - Select C_{Comp1} and C_{Comp2} to set pole and zero frequencies
- Build and test circuit

List system parameters

PARAMETER	SYMBOL	VALUE	UNIT	
Number of Phases	#	1		
Input Voltage	V_{IN}	3.3	V	
Output Voltage	V_{OUT}	0.75	V	
Load Current Step	$\Delta I_{OUT(step)}$	7.5	A	Enter the peak-to-peak load current step.
	V_{OUT}	2.5%		Enter the maximum allowable output voltage deviation during a load transient. For typical applications, use the maximum overall voltage tolerance minus 0.8% for the DC accuracy of the TPSM8287Bxx device.
		18.8E-3	V	
	t_f	1E-06	s	Enter the rise and fall time of the transient load step.
		1.5E-3	S	
	τ	12.5E-6	s	
	f_{SW}	1.50E+6	Hz	Enter the switching frequency (1.5 MHz nominal)
	ΔL_{fSW}	10%		
Inductance	L	50E-9	H	
Inductance Tolerance	TOL_{IND}	20%		
Maximum Bandwidth	BW_{max}	375E+3	Hz	
Recommended Bandwidth	BW	200E+3	Hz	
Target Bandwidth	BW_T	375E+3	Hz	Enter a target BW, between the values of the previous 2 cells. Values closer to 200 kHz are recommended for simpler designs.
Inductor Ripple Current	ΔI_L	7.7	A	This is the calculated ripple current in each inductor.
Total Inductor Current Step Change	$\Delta I_{OUT(max)}$	11.4	A	This is the total load step, once the inductor ripple current has been added to the load step current.

0.8% vs. 1% DC accuracy → more margin for load transient

50nH integrated inductor vs. 110nH external inductor → better load transient and higher ripple

1.5MHz vs. 2.25MHz frequency → lower BW and higher ripple

Calculate R_{Comp1}

Minimum Compensation Resistance (Calculated)	$R_{Comp1(min)}$	1,005	Ω	The is the minimum compensation resistance required to achieve the transient performance requirements.
Compensation Resistance (Used)	R_{Comp1}	1,000	Ω	Enter the value of R_{Comp1} you will use. This value should be larger than the value calculated above.

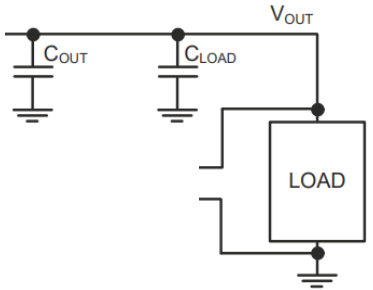
- 1kΩ selected as a common value, near the calculated minimum

Calculate required minimum C_{OUT}

Minimum Output Capacitance (regulated case)	$C_{OUT(min)(reg)}$	195E-6	F	This is the minimum output capacitance required, assuming the loop remains in regulation under all conditions.
Minimum Output Capacitance (saturated case)	$C_{OUT(min)(sat)}$	35E-6	F	This is the minimum output capacitance required, assuming the loop saturates during a transient.
Minimum Output Capacitance (Calculated)	$C_{OUT(min)}$	195E-6	F	This is the minimum output capacitance required to achieve the specified transient performance. It is the maximum of the two values calculated above.
Minimum Output Capacitance (Used)	$C_{OUT(min)}$	200E-6	F	Enter the minimum capacitance used in the application. Its value must be greater than the minimum calculated output capacitance, taking into consideration, tolerance, temperature effects, DC bias, aging, etc. The TPSM8287Bxx integrates an additional 14 µF of capacitance.

~200µF of effective capacitance chosen

- Need to pick specific capacitors to obtain this effective capacitance
- Total $C_{OUT} = C_{OUT\_IC} + C_{LOAD}$
- $C_{LOAD} > C_{OUT\_IC}$

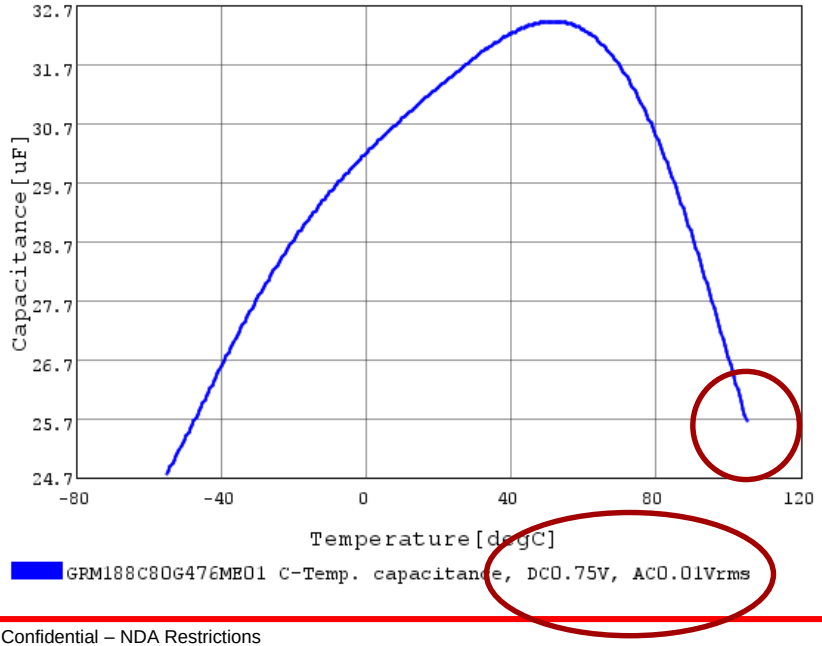


Select specific capacitors

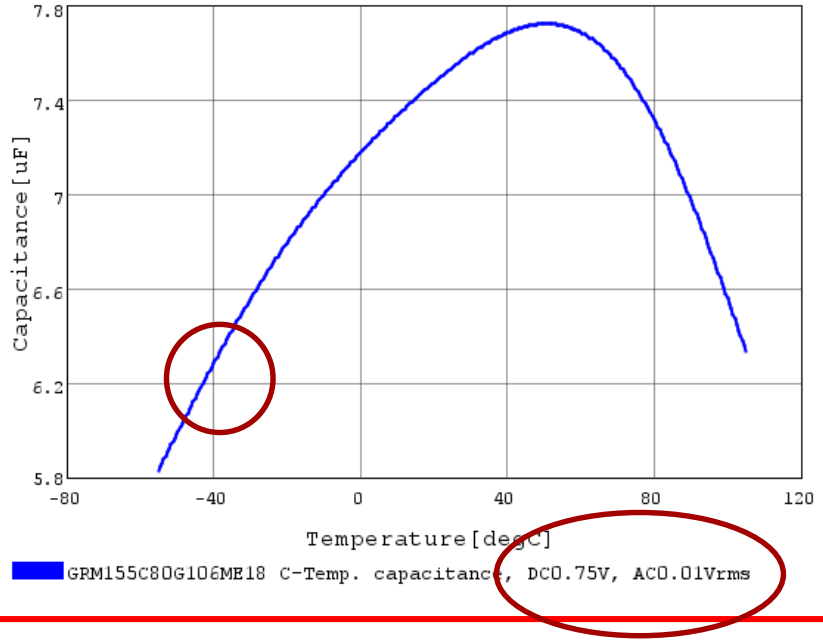
- Use GRM188C80G476ME01D (47µF) and GRM155C80G106ME18D (10µF)
- $C_{OUT\_IC} = 2 \times 47\mu F + 2 \times 7\mu F$ (internal C_{OUT})
- $C_{LOAD} = 4 \times 47\mu F + 4 \times 10\mu F$
- Use capacitor vendor's simulation tool to estimate effective capacitance over DC bias, AC bias (ripple), and temperature

Effective capacitance simulations

GRM188C80G476ME01D



GRM155C80G106ME18D

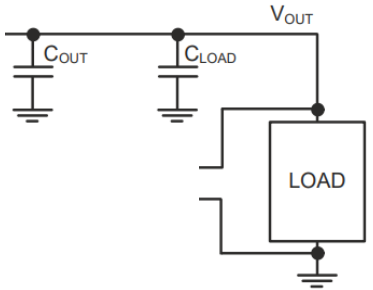


Select specific capacitors

C25 | =2*0.000007+6*0.0000257+4*0.0000062

	A	B	C	D	E
22	Minimum Output Capacitance (regulated case)	$C_{OUT(min)(reg)}$	195E-6	F	This is the minimum output capacitance required, assuming the loop remains in regulation under all conditions.
23	Minimum Output Capacitance (saturated case)	$C_{OUT(min)(sat)}$	35E-6	F	This is the minimum output capacitance required, assuming the loop saturates during a transient.
24	Minimum Output Capacitance (Calculated)	$C_{OUT(min)}$	195E-6	F	This is the minimum output capacitance required to achieve the specified transient performance. It is the maximum of the two values calculated above.
25	Minimum Output Capacitance (Used)	$C_{OUT(min)}$	193E-6	F	Enter the minimum capacitance used in the application. Its value must be greater than the minimum calculated output capacitance, taking into consideration, tolerance, temperature effects, DC bias, aging, etc. The TPSM8287Bxx integrates an additional 14 µF of capacitance.

- 193µF of effective capacitance chosen
- Total $C_{OUT} = C_{OUT\_IC} + C_{LOAD}$
- $C_{LOAD} > C_{OUT\_IC}$

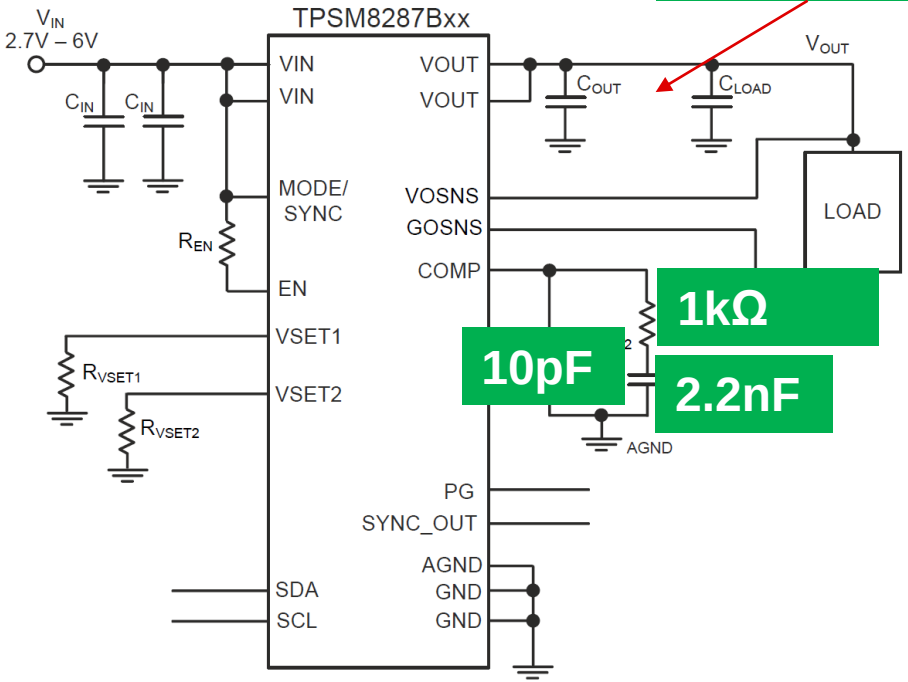


Select C_{Comp1} and C_{Comp2}

Output Voltage Ripple	$V_{p-p(max)}$	3.3E-3	V	The calculated maximum output voltage ripple, based on the minimum output capacitance value. The ripple will be slightly higher in the application, due to the ESR and ESL in the output capacitors.
Bandwidth	BW	309E+3	Hz	This is the calculated bandwidth of the converter using the above component values.
Primary Compensation Capacitance (Calculated)	C_{Comp1}	2.1E-9	F	This is the calculated primary compensation capacitance value.
Primary Compensation Capacitance (Used)	C_{Comp1}	2.2E-9	F	Enter the value of C_{Comp1} you will use. This value should be the closest standard value to the value calculated above.
Secondary Compensation Capacitance	C_{Comp2}	10E-12	F	Enter the value of C_{Comp2} you will use, if desired. The purpose of this capacitor is to bypass high frequency noise away from the COMP pin. Its value is not critical, and 10 pF is suitable for most applications.
Secondary Compensation Capacitance Pole	f_{pole}	15.9E+6	Hz	This is the calculated frequency of the pole created by C_{Comp2}.

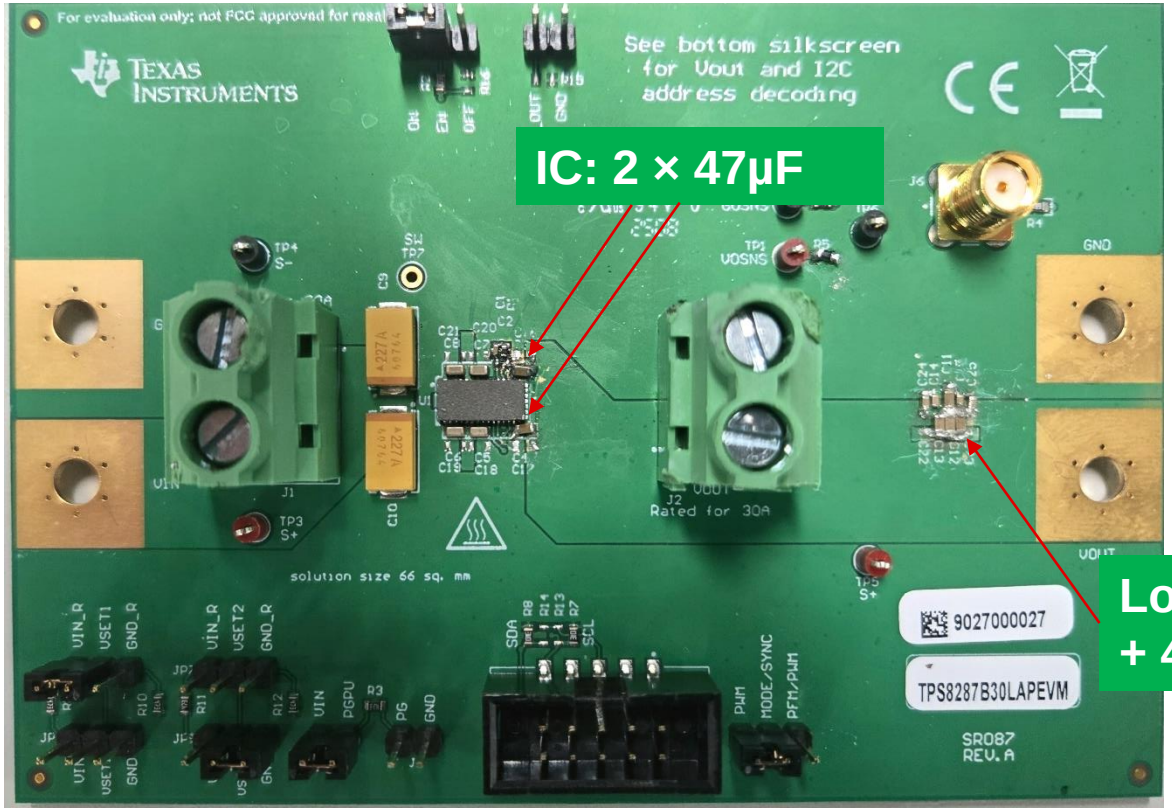
Final design 3a

IC: 2 × 47µF + 2 × 7µF (internal)
Load: 4 × 47µF + 4 × 10µF



TPSM8287Bxx Simplified Schemat

Final design



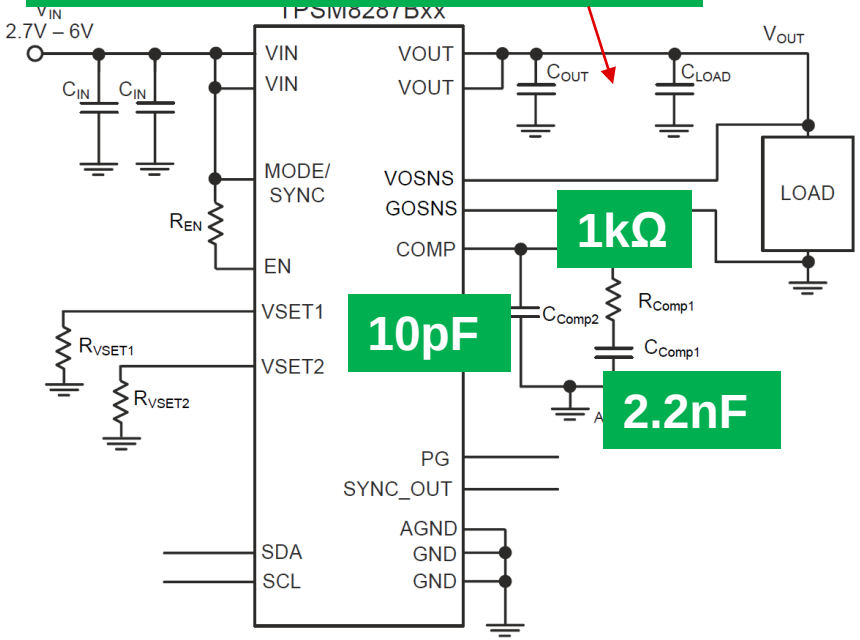
Design slightly misses the transient specification

- Droop compensation removed 6mV of the 8mV transient deviation gap
- 39.4mVp-p deviation during the load transient is still too large
  - 37.6mVp-p requirement

- Design 3a needs further adjustments → **Design 3b**
- Phase margin (56°) is high → increase gain → larger R_{Comp1}
- Design tweaks:
  - R_{Comp1} → 1.21kΩ

Final design 3a

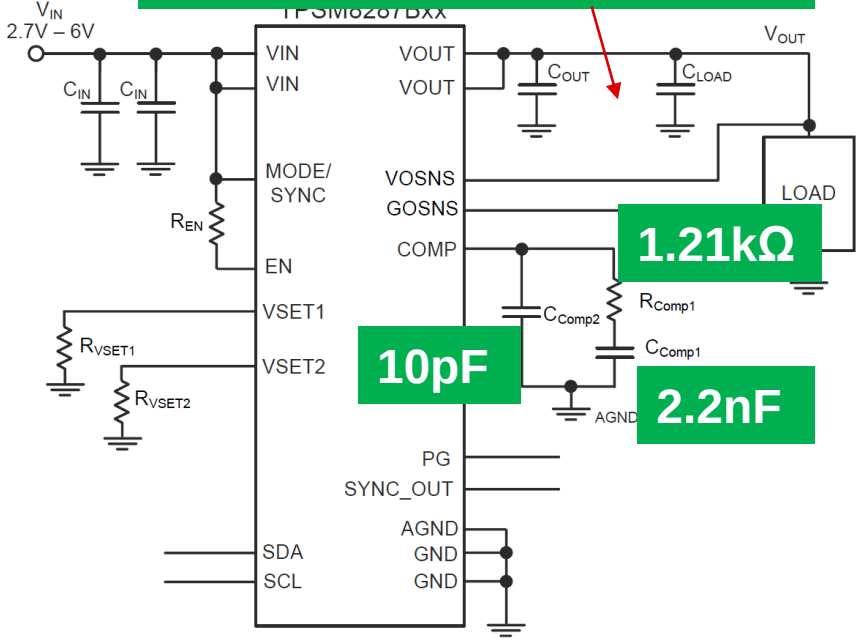
IC: 2 × 47µF + 2 × 7µF (internal)
Load: 4 × 47µF + 4 × 10µF



TPSM8287Bxx Simplified Schematic

Final design 3b

IC: 2 × 47µF + 2 × 7µF (internal)
Load: 4 × 47µF + 4 × 10µF

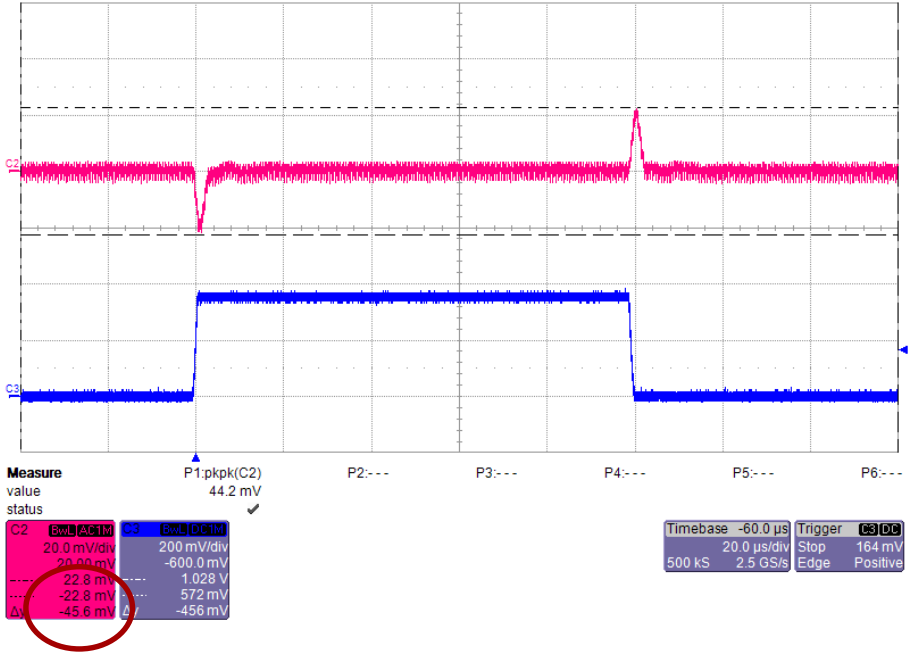


TPSM8287Bxx Simplified Schematic

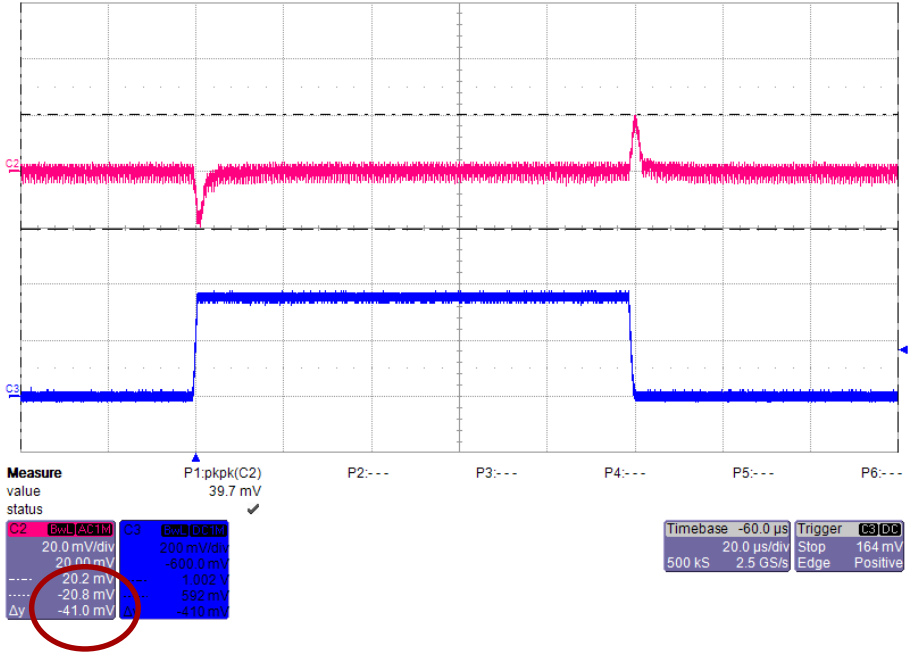
Load transient results

Vout (AC)
Iload (4A/div)

Final design 3a

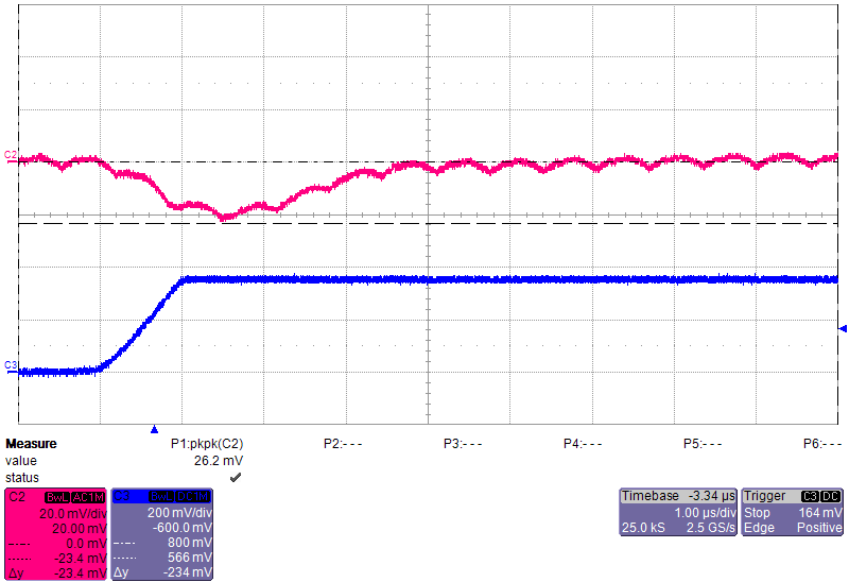


Final design 3b

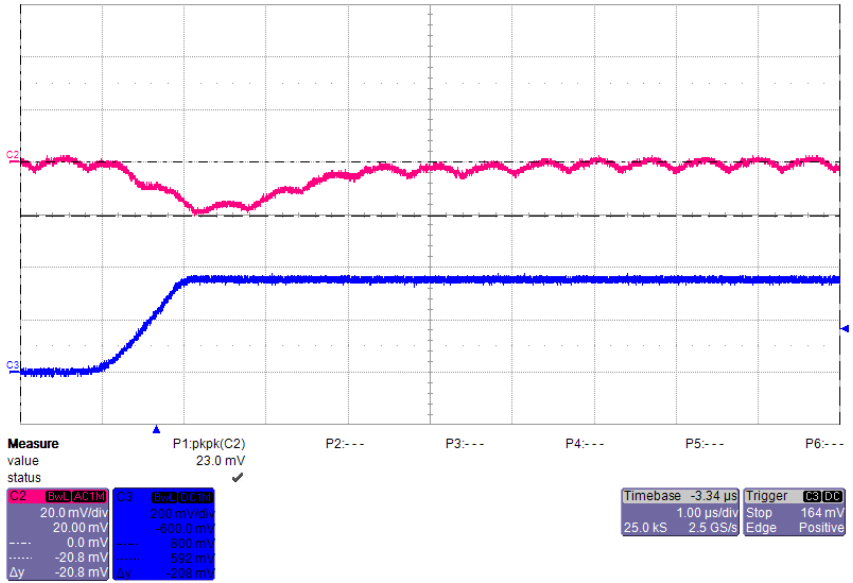


Load transient results – rising edge

Final design 3a

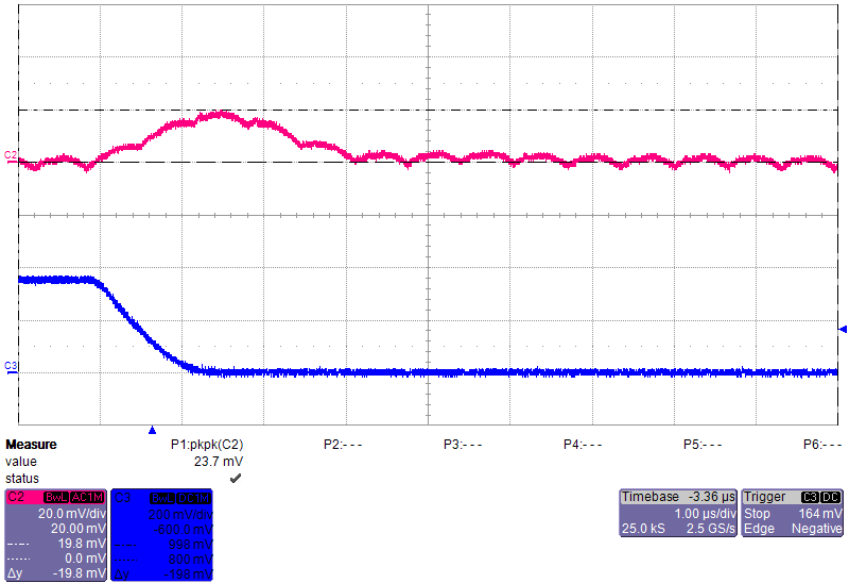


Final design 3b

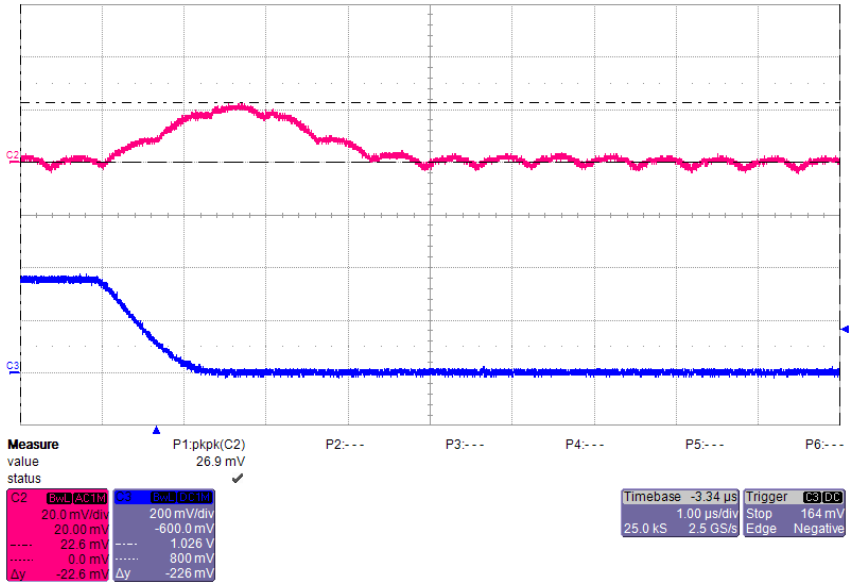


Load transient results – falling edge

Final design 3a



Final design 3b

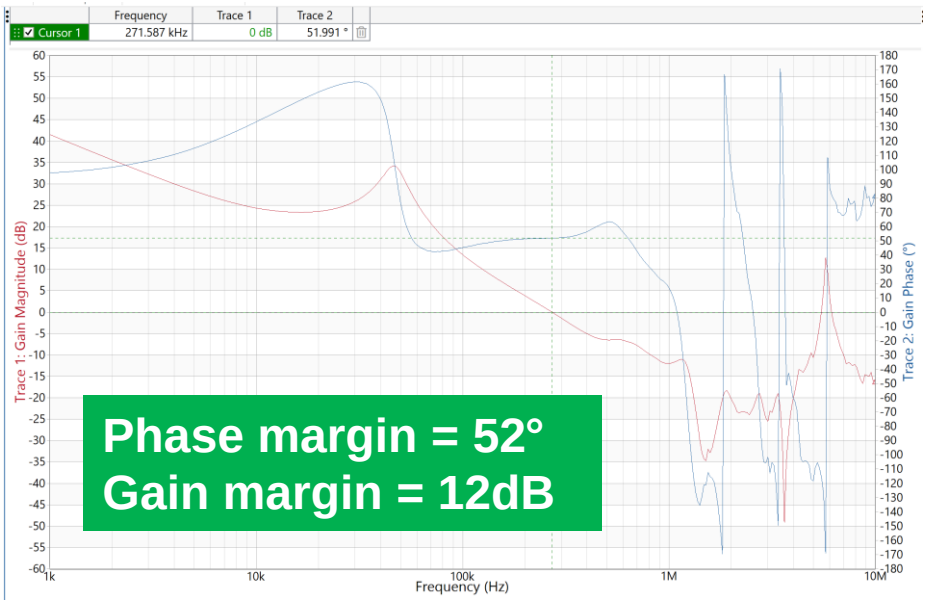


Bode plot (loop stability, 15A load)

Final design 3a

Phase margin = 56°
Gain margin = 13dB

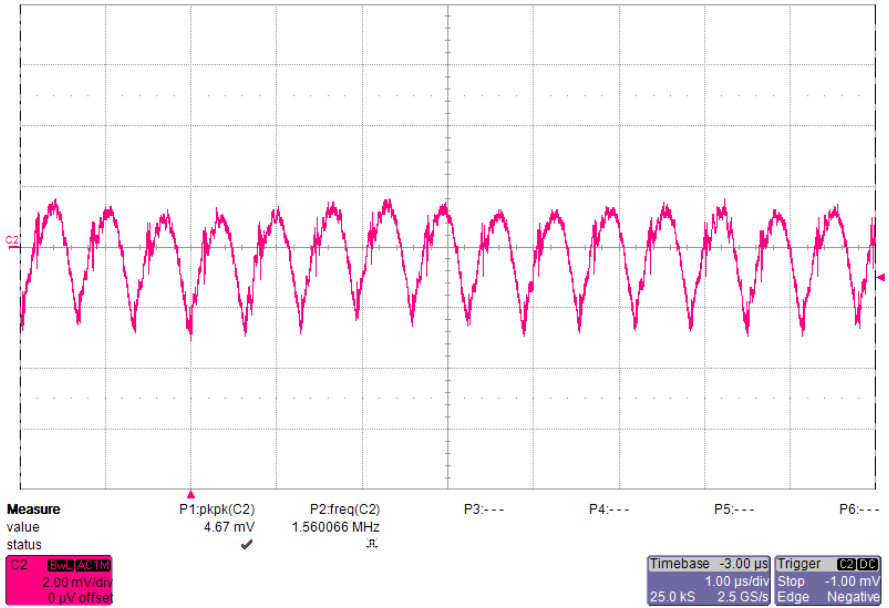
Final design 3b



Phase margin = 52°
Gain margin = 12dB

Output voltage ripple (15A load)

Final design 3a



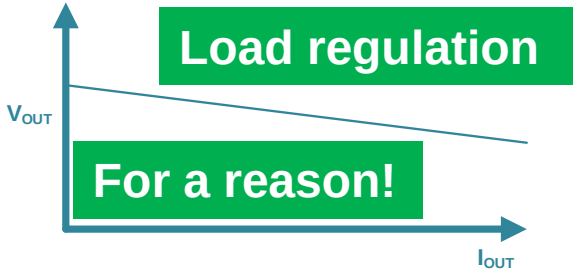
Final design 3b

Design misses the transient specification

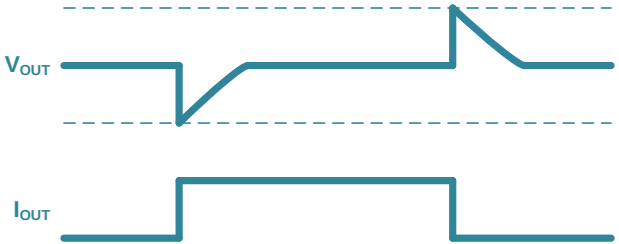
- 45.6mVp-p deviation during the load transient is too large
  - 37.6mVp-p requirement
- Enable droop compensation feature (via I^2C) to reduce the deviation

What is droop compensation?

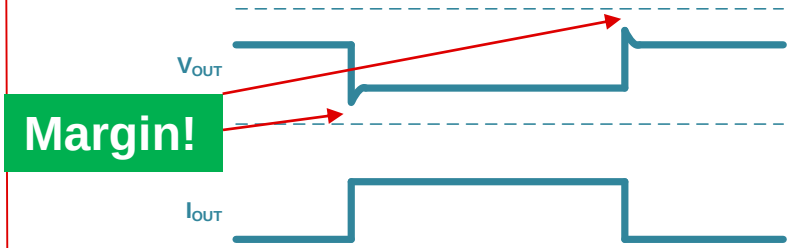
Load/line, adaptive voltage positioning (AVP), voltage droop



Normal



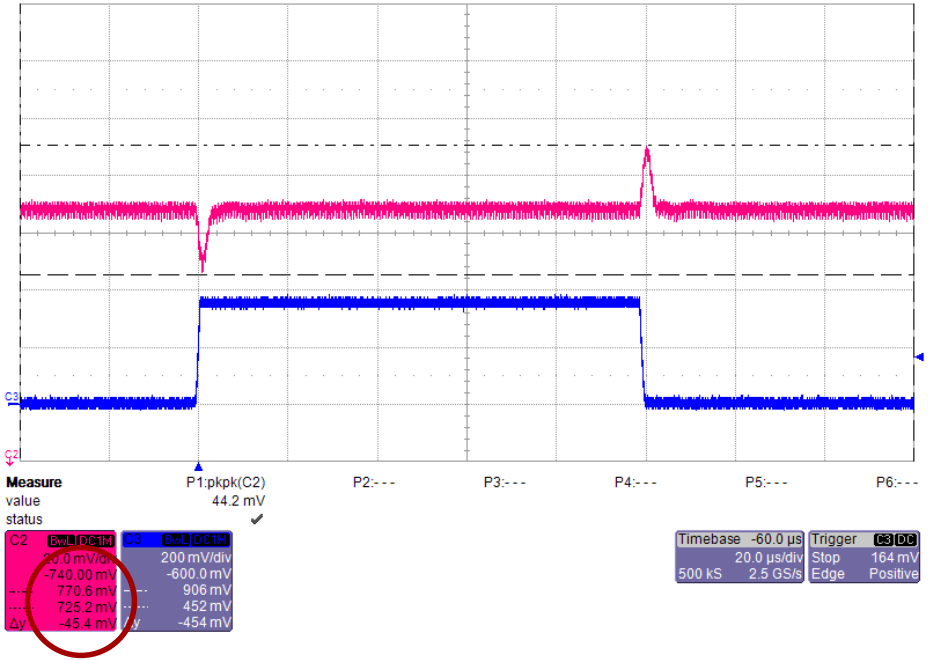
Droop Compensation



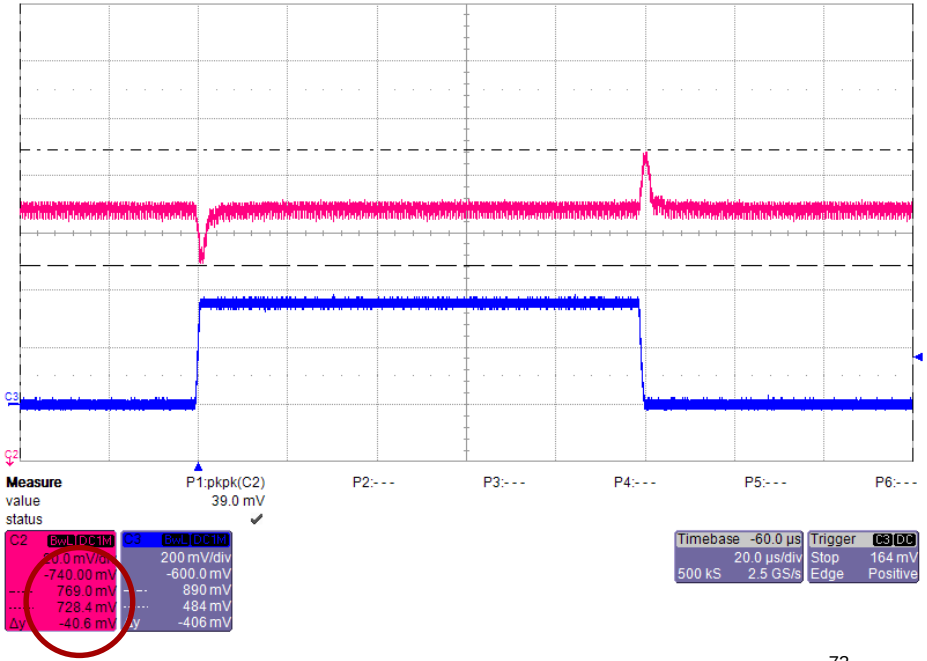
Load transient results

Vout (DC with a -740mV offset), Iload (4A/div)

Final design 3a



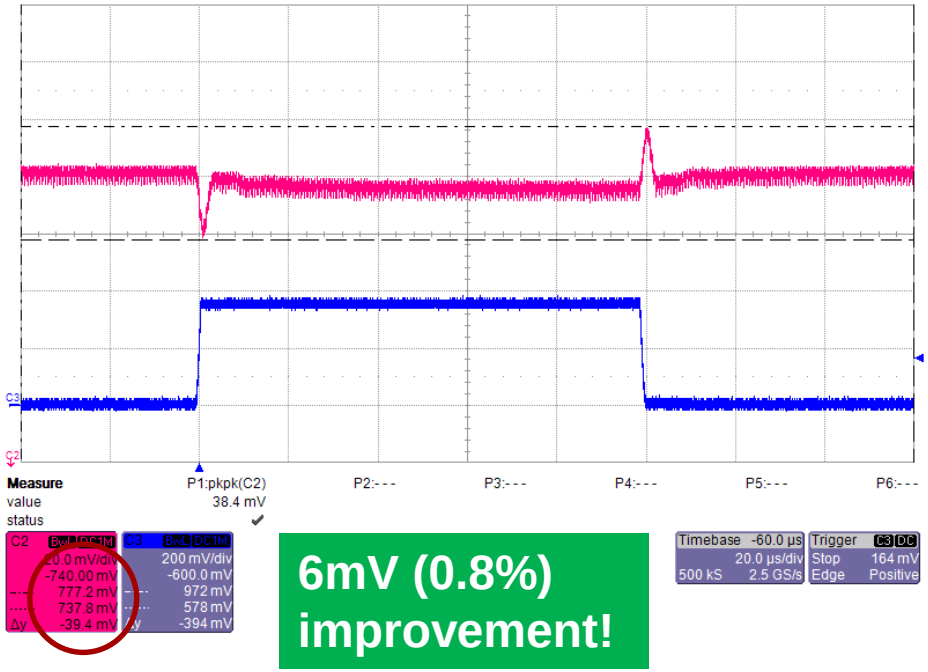
Final design 3b



Load transient results (droop compensation ON)

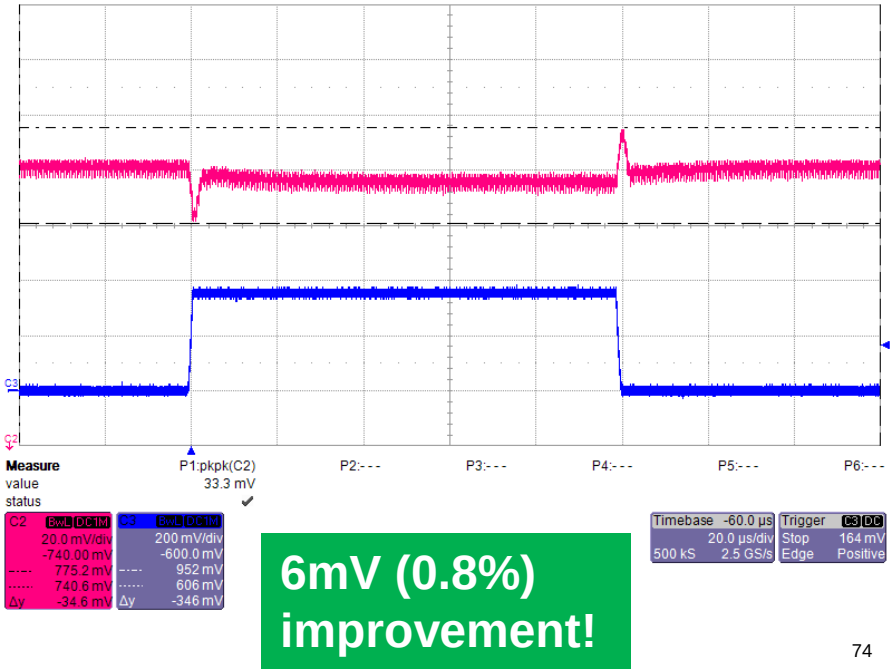
Vout (DC with a -740mV offset), Iload (4A/div)

Final design 3a



6mV (0.8%) improvement!

Final design 3b



6mV (0.8%) improvement!

Design summary

- Design 3a:
  - Transient response: 39.4mVp-p with droop compensation on
    - 45.4mVp-p with droop compensation off
  - Ripple: 4.67mVp-p
  - Bode plot: 265kHz BW, 56° phase margin, 13dB gain margin
  - Output capacitors: 6 × 0603 + 4 × 0402
- Design 3b:
  - Transient response: 34.6mVp-p with droop compensation on
    - 40.6mVp-p with droop compensation off
  - Ripple: 4.67mVp-p
  - Bode plot: 272kHz BW, 52° phase margin, 12dB gain margin
  - Output capacitors: 6 × 0603 + 4 × 0402

Q&A

Design summary (the end result)

Design	Goal	C_{OUT}	BW	Phase margin	Gain margin	Output ripple	Transient response
TPS62873 #1a 2.25MHz, 110nH	Transient	6 × 0603 4 × 0402	352kHz	28°	7dB	2.56mV p-p	31.9mV p-p
TPS62873 #1b 2.25MHz, 110nH	Transient	8 × 0603 4 × 0402	288kHz	37°	9dB	2.11mV p-p	31.7mV p-p
TPS62873 #2 2.25MHz, 110nH	Size	4 × 0603 2 × 0402	287kHz	48°	>20dB	3.20mV p-p	67.6mV p-p
TPSM8287B30 #3a 1.5MHz, 50nH	Transient	6 × 0603 4 × 0402	265kHz	56°	13dB	4.67mV p-p	39.4mV p-p
TPSM8287B30 #3b 1.5MHz, 50nH	Transient	6 × 0603 4 × 0402	272kHz	52°	12dB	4.67mV p-p	34.6mV p-p

All designs use the minimum C_{OUT} to meet the requirements

Summary

- Demanding processor core transients are met with the minimum amount of C_{OUT}
  - External compensation allows tuning of the control loop to the exact C_{OUT} and load transient
  - High DC accuracy, with differential remote sense, allows the most room for the transient deviation
  - Droop compensation supplies additional margin without requiring additional C_{OUT}
- Smallest size design yields <5 mVp-p output voltage ripple with < 100µF effective C_{OUT}

Q&A

Important notice and disclaimer

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.