Application Report
SLAA562–October 2012

PORT17 Guidance

ABSTRACT

MSP430 erratum PORT17 describes the behavior of certain MSP430 devices that can latch-up under specific conditions on the general-purpose I/O pins. This document describes the conditions that can cause the latch up, the affected devices and pins, and workarounds to prevent the latch up from occurring.

Due to the multiple factors that can cause the latch-up to occur, it is challenging to provide a single solution that fits all applications. The user is expected to analyze the requirements of each system and adapt a workaround or a combination of different steps to provide maximum robustness against latch-up.

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1 Introduction

Latch-up testing of MSP430 devices uses tests based on the JEDEC standard JESD78C and include a set of tests known as the I-Tests. These tests involve powering the device under test (DUT) and subjecting port pins to a trigger current that is polarized and characterized as per the test conditions mandated by the JEDEC standard. To pass the test, pins subject to the trigger current and any neighboring pins must not latch-up when a specific trigger current is applied.

For MSP430 devices that are affected by PORT17 erratum, subjecting specific pins to the high negative trigger current can cause a latch-up to occur in the neighboring pins. The list of affected devices, the trigger currents required to cause the latch-up, and the specific pins that are affected are listed in the following sections. Note that while the pins are subject to high current pulses as a part of routine stress tests, these conditions are outside the absolute maximum rating for device operation. One possible situation where a device may undergo similar (but not identical) exposure to such conditions is in the case of an ESD event. It is important to understand that the occurrence of latch-up is unlikely and manifests only under specific circumstances.

NOTE: For MSP430 devices that are affected by PORT17 erratum, only negative high-current triggers can cause latch-up. Latch-up does not occur for any value of positive high-current triggers.

2 Erratum: PORT17

Module: General Purpose I/O

Function: Certain pins when subject to negative high current pulses may cause latch-up in adjacent pins.

Description:

Pins subject to negative high current pulses may cause latch-up in adjacent pins. The latch-up condition exists only if the adjacent pin configurations also referred to as 'affected-pin' configuration are one of the following:

- GPIO input driven high by an external source
- GPIO output driven high with full drive strength or reduced drive strength settings
- Peripheral configuration where the peripheral drives pin high or causes pin to be driven high externally

The following affected-pin configurations will not sustain latch-up:

- GPIO input driven low
- GPIO output driven low
- Peripheral configuration where the peripheral drives pin low or causes pin to be driven low externally
- Peripheral configuration as LCD pin

Note that for affected-pin configurations with LCD functionality, the window of latch-up when the pin is driven being high still exists but is of extremely short duration and hence there is a low probability of latch-up occurrence.

Workaround:

All affected pins must be driven low when not in use. If the affected pins are not driven low, then connecting a series resistor of 330 Ω to limit the latch-up current is recommended.

3 Affected Devices: MSP430F663x, MSP430F563x, and MSP430F533x Families

MSP430F6638	MSP430F6436	MSP430F5635
MSP430F6637	MSP430F6435	MSP430F5634
MSP430F6636	MSP430F6433	MSP430F5633
MSP430F6635	MSP430F5338	MSP430F5632
MSP430F6634	MSP430F5336	MSP430F5635
MSP430F6633	MSP430F5335	MSP430F5631
MSP430F6632	MSP430F5333	MSP430F5630
MSP430F6631	MSP430F5638	
MSP430F6630	MSP430F5637	
MSP430F6438	MSP430F5636	

3.1 Trigger Pins

For devices affected by the erratum, the pins subjected to high trigger currents may cause latch-up in either one of the adjacent pins. For the remainder of this document, the pin under test that is subjected to the high negative current trigger pulse is referred to as the 'Trigger pin' and pins that are latched-up due to the proximity to the Trigger pin are referred to as the 'affected pins'. As an example in Figure 1, when pin 31 (P5.3/COM1/S42) on the F6638IPZ device is subject to a high negative current trigger due to an ESD event, it may result in the latch-up of the pins on either side of pin 31; that is, pin 30 or pin 32. In this case, pin 31 is referred to a "Trigger" pin and pins 30 and 32 are referred to as "Affected" pins.

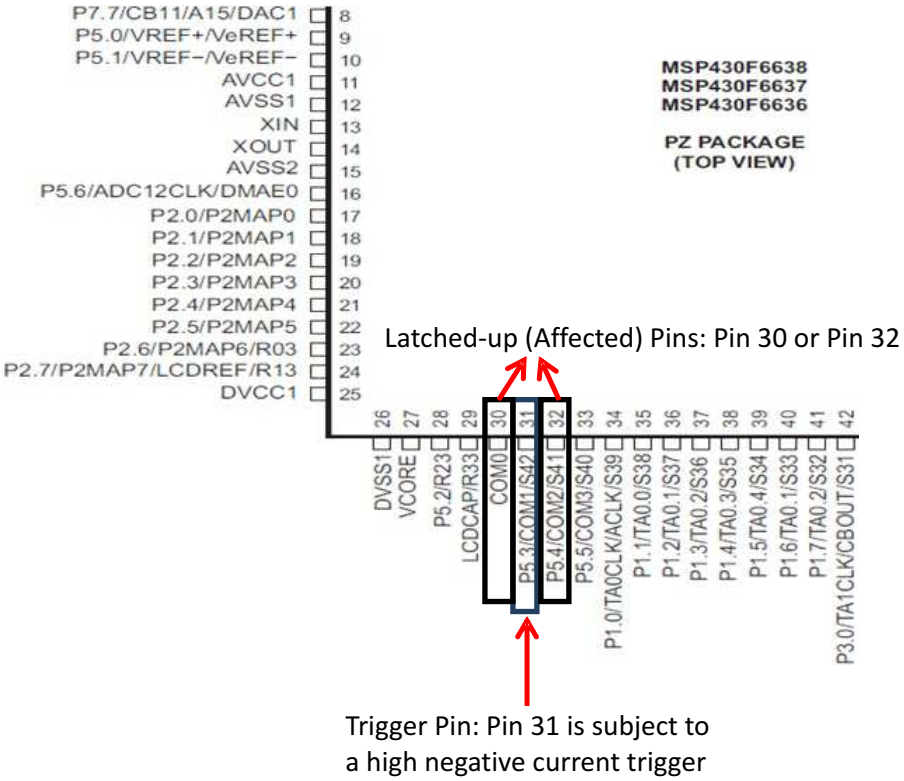

Figure 1. F6638 PZ package pinout showing an example of trigger pin and affected pins

Table 1, Table 2, and Table 3 list the Trigger pins that can cause latch-up in one or both neighboring pins (referred to as the Affected pin) for each package variant. The trigger current on the pin that is likely to cause latch-up is also highlighted. The tables are categorized as high, medium, and low trigger current categories based on the current required to cause a latch-up. Note that the affected pins need to have certain specific configurations to sustain the latch-up if it occurs. These configurations are explained in Section 4.1.

3.1.1 High-Current Triggers

The pins listed in Table 1 are categorized as low risk, because a very high trigger current is required to cause latch-up on an Affected pin. The actual trigger current for each trigger pin that results in a latch-up is also listed.

Table 1. F663x, F563x, and F533x device pins that cause latch-up when subject to high current triggers

Affected Pin Terminal Name	PZ Package Pin Number	ZQW Package Ball Designation	Trigger Current
COM0/DNC	30	J4	-95 mA
P1.0/TA0CLK/ACLK/S39	34	L5	-100 mA
P8.4/UCB1CLK/UCA1STE/S11	62	G11	-90 mA
P9.7/S0	75	D9	-90 mA

3.1.2 Medium-Current Triggers

The pins listed in Table 2 are categorized as medium risk, because a trigger current in the range of -30 mA to -40 mA is required to cause latch-up in an Affected pin. The actual trigger current for each trigger pin that results in a latch-up is also listed.

Table 2. F663x, F563x, and F533x device pins that cause latch-up when subject to medium current triggers

Affected Pin Terminal Name	PZ Package Pin Number	ZQW Package Ball Designation	Trigger Current
P5.3/COM1/S42	31	L4	-30 mA
P5.4/COM2/S41	32	M4	-35 mA
P5.5/COM3/S40	33	J5	-40 mA
P1.1/TA0.0/S38	35	M5	-40 mA
P1.2/TA0.1/S37	36	J6	-40 mA
P1.3/TA0.2/S36	37	H6	-40 mA
P1.4/TA0.3/S35	38	M6	-40 mA
P1.5/TA0.4/S34	39	L6	-40 mA
P1.6/TA0.1/S33	40	J7	-40 mA
P1.7/TA0.2/S32	41	M7	-40 mA
P3.0/TA1CLK/CBOUT/S31	42	L7	-40 mA
P3.1/TA1.0/S30	43	H7	-40 mA
P3.2/TA1.1/S29	44	M8	-40 mA
P3.3/TA1.2/S28	45	L8	-40 mA
P3.4/TA2CLK/SMCLK/S27	46	J8	-40 mA
P3.5/TA2.0/S26	47	M9	-40 mA
P3.6/TA2.1/S25	48	L9	-40 mA
P3.7/TA2.2/S24	49	M10	-40 mA
P4.0/TB0.0/S23	50	J9	-40 mA
P4.1/TB0.1/S22	51	M11	-40 mA
P4.2/TB0.2/S21	52	L10	-40 mA

Table 2. F663x, F563x, and F533x device pins that cause latch-up when subject to medium current triggers (continued)

Affected Pin Terminal Name	PZ Package Pin Number	ZQW Package Ball Designation	Trigger Current
P4.3/TB0.3/S20	53	M12	-40 mA
P4.4/TB0.4/S19	54	L12	-40 mA
P4.5/TB0.5/S18	55	L11	-40 mA
P4.6/TB0.6/S17	56	K11	-40 mA
P4.7/TB0OUTH/SVMOUT/S16	57	K12	-30 mA
P8.0/TB0CLK/S15	58	J11	-30 mA
P8.1/UCB1STE/UCA1CLK/S14	59	J12	-30 mA
P8.2/UCA1TXD/UCA1SIMO/S13	60	H11	-30 mA
P8.3/UCA1RXD/UCA1SOMI/S12	61	H12	-30 mA
P8.5/UCB1SIMO/UCB1SDA/S10	65	F11	-30 mA
P8.6/UCB1SOMI/UCB1SCL/S9	66	G9	-30 mA
P8.7/S8	67	E12	-30 mA
P9.0/S7	68	E11	-30 mA
P9.1/S6	69	F9	-30 mA
P9.2/S5	70	D12	-30 mA
P9.3/S4	71	D11	-30 mA
P9.4/S3	72	E9	-30 mA
P9.5/S2	73	C12	-30 mA
P9.6/S1	74	C11	-30 mA

3.1.3 Low-Current Triggers

The pins listed in Table 3 are categorized as high risk, because a trigger current in the range of -10 mA can cause latch-up in an Affected pin. The actual trigger current for each trigger pin that results in a latch-up is also listed.

Table 3. F663x device pin that causes latch-up when subject to low-current triggers

Affected Pin Terminal Name (F6xxx Only)	PZ Package Pin Number	ZQW Package Ball Designation	Trigger Current
LCDCAP/R33	29	M3	-6 mA

On F56xx and F53xx (non-LCD) devices, this pin is required to be configured as a digital ground pin (DVSS) and is hence not affected by the erratum.

On F66xx and F64xx devices that have the recommended 4.7-µF capacitor populated on the LCDCAP pin, the risk of current injection is very low, making this pin very unlikely to be affected by the erratum.

4 Causes for Latch-up and Prevention

In CMOS circuits, latch-up is caused by the creation of a parasitic silicon-controlled rectifier (SCR). To sustain the latch-up, a minimum current is required to hold the latched SCR in the ON state. This minimum current level is known as the holding current. Hence, a voltage pulse is required to trigger the SCR, and a holding current is required to sustain it.

On the F66xx devices and variants, the affected pins can be configured using specific settings that make them capable of sustaining the latch-up. These settings are described in the below sections.

There are two important factors to consider:

- To cause a latch-up the affected pin must be driven high either internally or externally.

- The latch-up is sustained only as long as the V/I relationship (that is, the holding current) is maintained by the affected port pin.

The following section discusses the affected pin configurations that might result in a latch-up.

4.1 Affected Pin Configurations That Sustain Latch-up

Any of the following affected-pin configurations can sustain a latch-up if a neighboring Trigger pin is subject to a high negative current trigger:

- GPIO input is driven high by an external source

  In this case, the external current source that is used to drive the pin high must be capable of sustaining the latch-up. If the source is current-limited to below the holding current, then this prevents the latch-up from occurring.

- GPIO output is driven high with reduced drive strength or full drive strength settings

  When any Affected pins are driven high internally, they can latch-up when the trigger pin is subject to a high negative current. Driving a pin high internally is done by setting the PxDIR and PxOUT registers to 1.

  As already mentioned, a certain minimum amount of current, the holding current, is required to sustain the latch-up. The device's ability to supply this holding current when the affected pin is driven high internally is directly dependent on the V/I characteristics of the pin. On the F66xx, F64xx, F56xx, and F53xx devices, the GPIO pins have two configurable drive strength settings – full and reduced. When configured with the full drive strength, setting the GPIO can sustain a high voltage level (V_{OH}) with larger sink currents. This makes it more likely to sustain a latch-up condition. When the pin is driven high with a reduced drive strength setting, it may be on the margin of being able to sustain the holding current, and latch-up may not occur.

  The V/I relationship must be evaluated on a per-device basis and is specified in the data sheet in the *Schmitt Trigger Inputs-General Purpose I/O* section.

- A peripheral or module drives the pin high, or the pin is driven high externally

  This case would be similar to (1) and if the module continually drives the pin high, it is possible for latch-to up occur.

The following section discusses the affected pin configurations that prevent or avoid latch-up.

4.2 Affected Pin Configurations That Avoid Latch-up

When affected pins are set up using any of the configurations described below, the pins cannot sustain a latch-up, because the voltage needed to trigger the SCR is not available.

- GPIO input is driven low
- GPIO output is driven low
- Peripheral or module drives the pin low, or the pin is driven low externally
- Peripheral configuration as LCD pin: Typically pins configured as LCD segments pin are driven high for brief time intervals. The probability that a high negative current strike on a neighboring pin is synchronized with the high interval on the LCD pin is very low. Hence this configuration option will most likely avoid latch-up or the latch-up will not continue longer than one LCD period, since intermediate or low voltage levels will not sustain the holding current.

4.3 Recommendations to Prevent Latch-up

Any one of the following recommendations can be used to prevent latch-up of the affected pin:

- Use pin configurations described in Section 4.2.
- For affected pins driven high internally, use software to periodically drive the pin low, thereby interrupting a possible latch-up condition or reducing the window of probability for latch-up to occur.
- For affected pins driven high externally, ensure that the external source is current-limited to provide only less than the holding current (<15 mA).
- Use a resistance of at least 330 Ω in series with affected pins to ensure that the minimum holding current is not sustainable. See Section 4.3.1 for more details on how the series resistance value affects latch-up.
- Drive all unused pins low or tie to GND.
- When an affected pin is configured as a peripheral pin (other than as an LCD segment pin), pins not in use can be temporarily configured as a GPIO and driven low.

4.3.1 Using a Series Resistance to Prevent Latch-up

To test the minimum holding current required to sustain the latch-up, bench tests were performed on multiple F6638 devices and the results are summarized in Table 4. It should be noted that temperature has an impact on the holding current, and an increase in temperature results in a reduced holding current. Hence the measurements were made at three different temperatures (25°C, 50°C, and 85°C). When measuring the holding current, a variable resistance was added in series to the affected GPIO to determine the maximum resistance at which latch-up is maintained. In other words, a higher resistance renders the latch-up condition unsustainable. Note that the data shown in Table 4 was collected across multiple units and different temperatures to provide a guidance estimate and must be regarded as such.

The results in Table 4 are sorted by temperature and three different trigger and affected-pin combinations are shown as examples.

Table 4. Bench test results at V_{CC} = 3.6 V with holding current for different pins and the series resistance values above which latch-up is not sustained

Temperature (°C)	Series Resistance (Ω)	V_{pin} (V)	Holding Current, I_{pin} (mA)
Trigger Pin = LCDCAP, Affected pin = P5.2			
25	130	1.4	17
50	190	1.3	12
85	310	1.1	8
Trigger Pin = P1.7, Affected Pin = P1.6			
25	130	1.4	17
50	190	1.3	12
85	320	1.2	8
Trigger Pin = P4.5, Affected Pin = P4.6			
25	130	1.4	17
50	200	1.3	12
85	330	1.2	8

Based on bench test results we can reach the following conclusions:

- To prevent latch-up across the temperature range of the device (-40°C to 85°C), a series resistance in the range of 300 to 350 Ω is needed in series with the affected GPIOs. For temperature-restricted applications (at room temperature), this value can be reduced to 150 Ω or less.
- The current required to hold the latch-up can vary from approximately 8 mA to approximately 17 mA across the temperature range of the device. Note that the V_{pin}/I_{pin} relationship must be maintained by the affected pin to sustain the latch-up.

5 Summary

The occurrence of PORT17 can be minimized by ensuring that the affected pins are either configured to avoid latch-up or by periodically changing the configuration to ensure that latch-up is not sustained. The most reliable method to avoid the occurrence of PORT17 is to prevent GPIOs from being subject to high negative current pulses (that is, prevent the occurrence of trigger currents on pins). This can be done by ensuring that the application is not subject to any condition that is outside of the device absolute maximum ratings and by undertaking proper ESD precautions. *MSP430 System-Level ESD Considerations* (SLAA530) gives a good overview on how to protect the device from ESD.

It must be noted that latch-up issues due to PORT17 are a rare occurrence and can only be brought about by a combination of both a high negative trigger current and specific affected pin configuration. Hence it is reasonable to assume that the probability of being affected is low and is significantly reduced when following the recommendations provided in this document.

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