6.8.1.1 ADC Electrical Data and Timing

Table 6-16. ADC Operating Conditions (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Input clock	5		50	MHz
Sample window duration	320			ns
Conversion range	V_{REFLO}		V_{REFHI}	V
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V
Input common mode voltage(1)	V_{REFCM} – 50		V_{REFCM} + 50	mV

(1) $V_{REFCM} = (V_{REFHI} + V_{REFLO})/2$

Table 6-17. ADC Characteristics (16-Bit Differential Mode)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC conversion cycles(1)		29.6		31	ADCCLKs
Power-up time				500	µs
Gain error		–64	±9	64	LSBs
Offset error(2)		–16	±9	16	LSBs
Channel-to-channel gain error			±6		LSBs
Channel-to-channel offset error			±3		LSBs
ADC-to-ADC gain error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
ADC-to-ADC offset error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
DNL(3)		> –1	±0.5	1	LSBs
INL		–3	±1.5	3	LSBs
SNR	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		86.9		dB
THD	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		–93.5		dB
SFDR	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		95.4		dB
SINAD	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		86.6		dB
ENOB	V_{REFHI} = 2.5 V, f_{in} = 10 kHz		14.1		bits
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 1 kHz		77		dB
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz		74		dB
ADC-to-ADC isolation (synchronous)(4)(5)			±4		LSBs
ADC-to-ADC isolation (asynchronous)(4)(6)			±TBD		LSBs

(1) See Section 6.8.1.1.2.
(2) Difference from conversion result 32768 when ADCINp = ADCINn = V_{REFCM}.
(3) No missing codes.
(4) Code deviation due to operation of multiple ADCs simultaneously.
(5) All ADCs operating with identical ADCCLK, S+H duration, and triggers.
(6) All ADCs operating with heterogenous ADCCLK, S+H duration, or triggers.

ADVANCE INFORMATION

Table 6-18. ADC Operating Conditions (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Input clock	5		50	MHz
Sample window duration	75			ns
Conversion range	V_{REFLO}		V_{REFHI}	V
V_{REFHI}	2.4	2.5 or 3.0	V_{DDA}	V
V_{REFLO}	V_{SSA}	0	V_{SSA}	V

Table 6-19. ADC Characteristics (12-Bit Single-Ended Mode)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC conversion cycles(1)		10.1		11	ADCCLKs
Power-up time				500	µs
Gain error		–8	±6	8	LSBs
Offset error		–4	±2	4	LSBs
Channel-to-channel gain error			±4		LSBs
Channel-to-channel offset error			±2		LSBs
ADC-to-ADC gain error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
ADC-to-ADC offset error	Identical V_{REFHI} and V_{REFLO} for all ADCs		±TBD		LSBs
DNL(2)		> –1	±0.5	1	LSBs
INL		–2	±1.0	2	LSBs
SNR	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		67.8		dB
THD	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		–78.4		dB
SFDR	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		79.2		dB
SINAD	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		67.7		dB
ENOB	V_{REFHI} = 2.5 V, f_{in} = 100 kHz		11.0		bits
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 1 kHz		60		dB
PSRR	V_{DDA} = 3.3-V DC + 200 mV Sine at 800 kHz		57		dB
ADC-to-ADC isolation (synchronous)(3)(4)			±1		LSBs
ADC-to-ADC isolation (asynchronous)(3)(5)			±TBD		LSBs

(1) See Section 6.8.1.1.2.
(2) No missing codes.
(3) Code deviation due to operation of multiple ADCs simultaneously.
(4) All ADCs operating with identical ADCCLK, S+H duration, and triggers.
(5) All ADCs operating with heterogenous ADCCLK, S+H duration, or triggers.