Notes:

1) Printed circuit board is controlled impedance.
2) Put multiple vias on Sonata's power pad for heat dissipation.
3) J6 and J8 to J19 are 2mm pitch and 0.8mm diameter.

DIFFERENTIAL PAIRS

PAGE 2 - 90 OHM
- PG2_GPIO42
- PG5_GPIO45

PAGE 3 - 90 OHM
- M3_USB0DM
- PG5_GPIO45

PAGE 7 - 100 OHM
- TX+
- TX-
- RX+
- RX-

SCHEMATIC CONTENTS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	Concerto DIMM-100 CC	4-13-2010	
B	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
C	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
D	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
E	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
F	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
G	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		

REVISION STATUS OF SHEETS

REV									
SH									
REV									
SH									
REV	G	A	A	A	A	G		NEXT ASSY	USED ON
SH	1	2	3	4	5	6		APPLICATION	

DWN	DATE
CHK	DATE
ENGR	DATE
ENGR-MGR	DATE
QA	DATE
MFG	DATE
RLSE	DATE

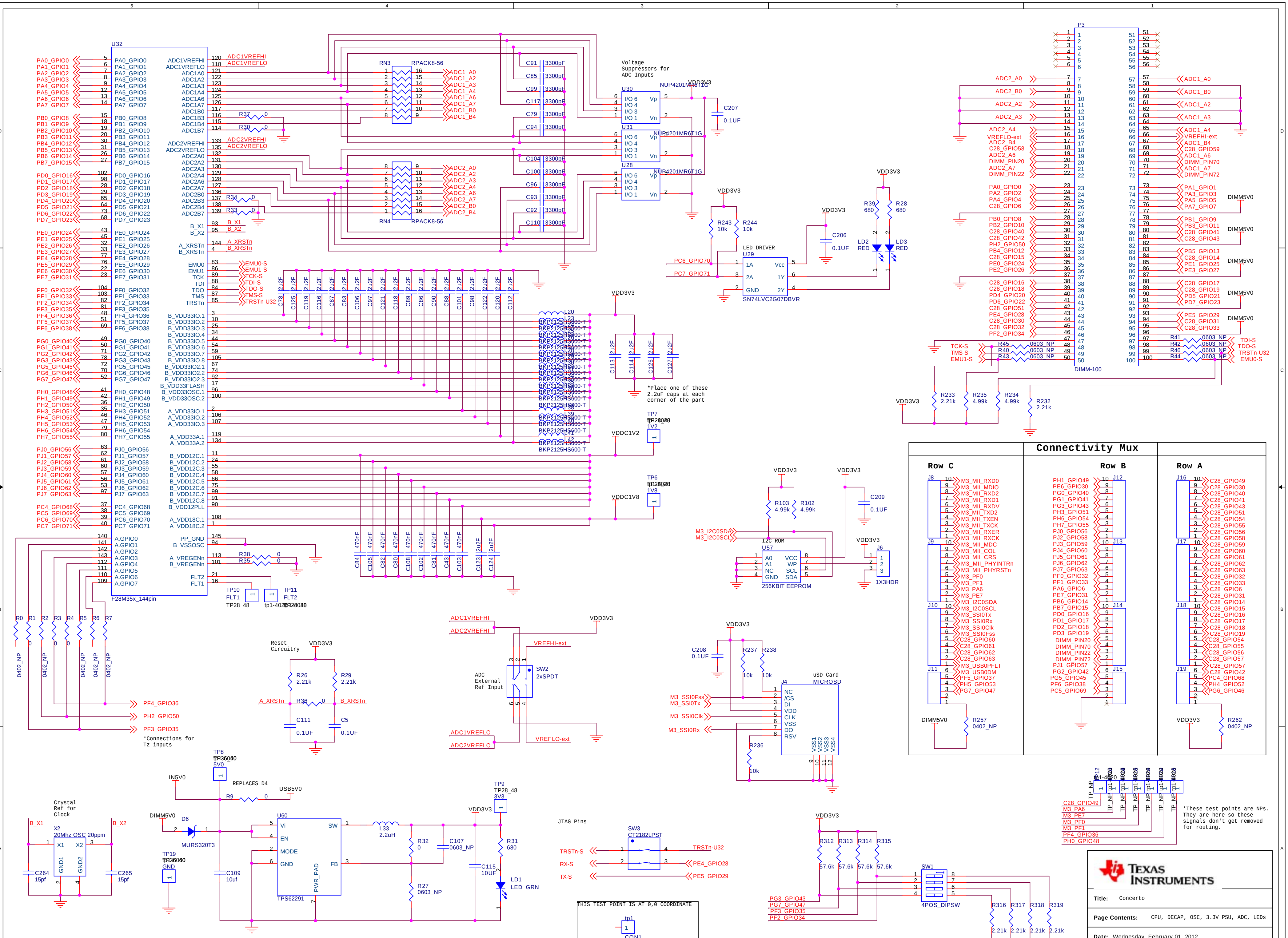
TEXAS INSTRUMENTS

Title: Cover Page

Page Contents: Layout info, schematic notes

Date: Wednesday, February 01, 2012

Rev: G | **Size:** B | **Sheet** 1 **of** 6



TEXAS INSTRUMENTS

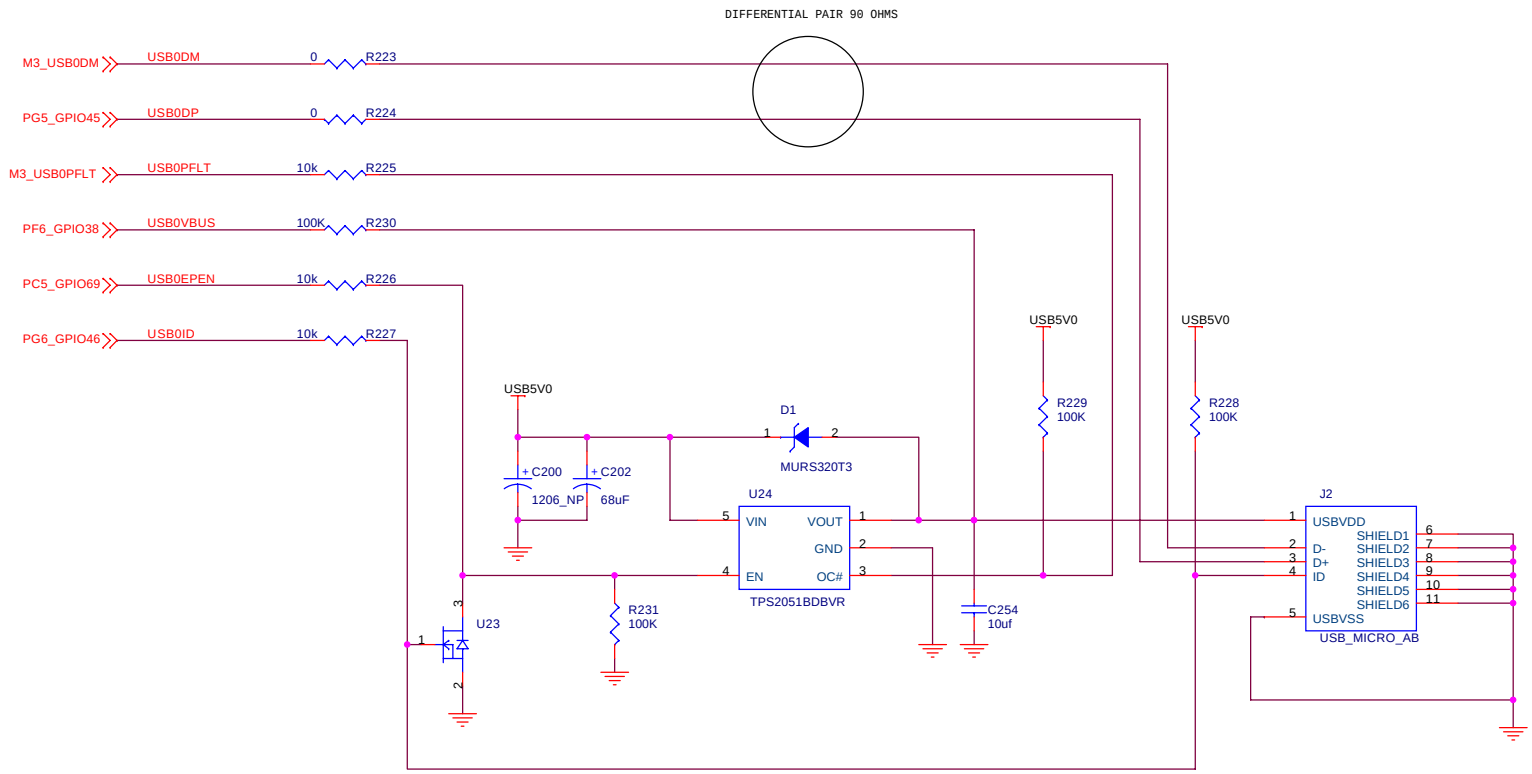
Title: Concerto

Page Contents: CPU, DECAP, OSC, 3.3V PSU, ADC, LEDs

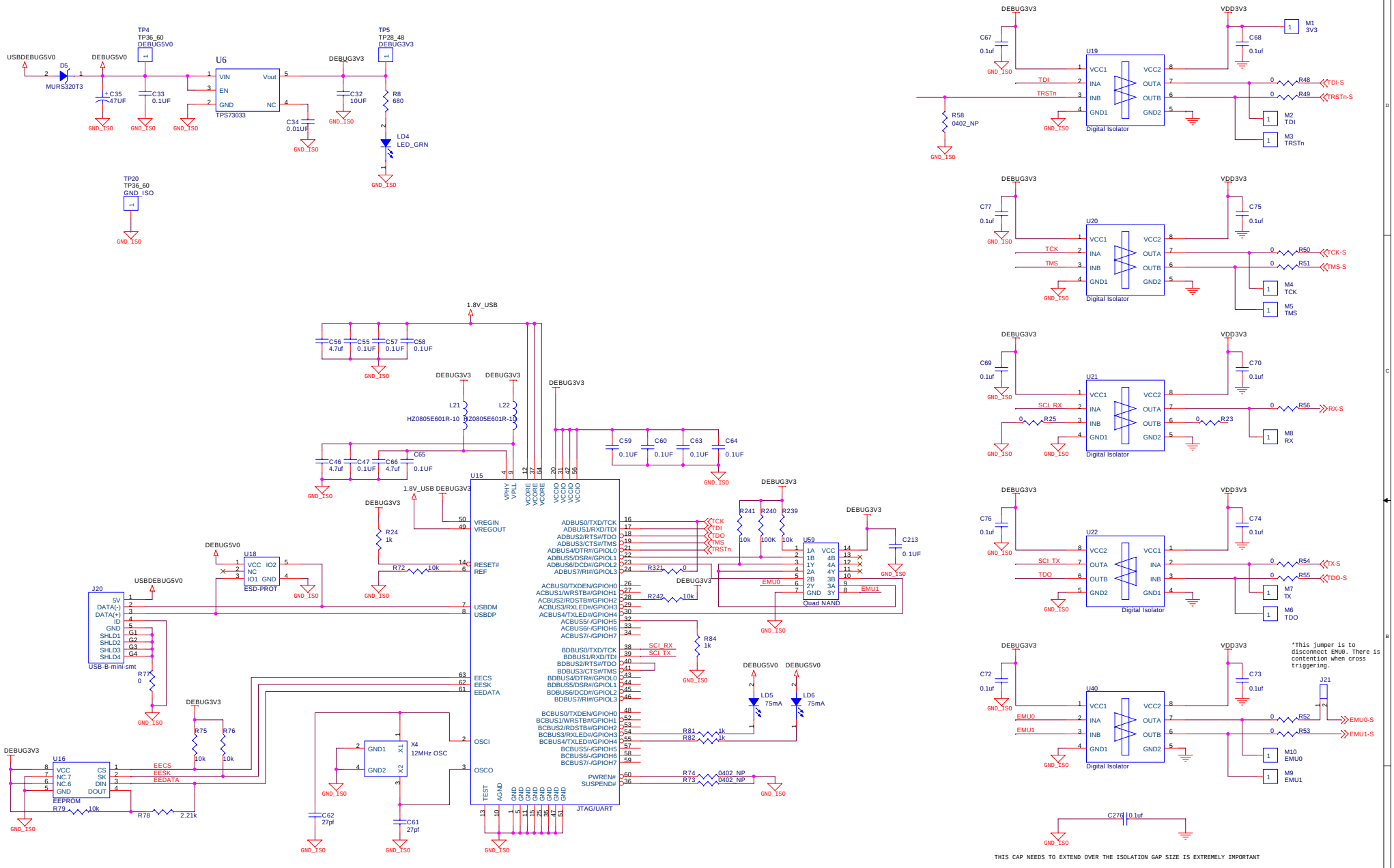
Date: Wednesday, February 01, 2012

Rev: B | Size: C | Sheet 2 of 6

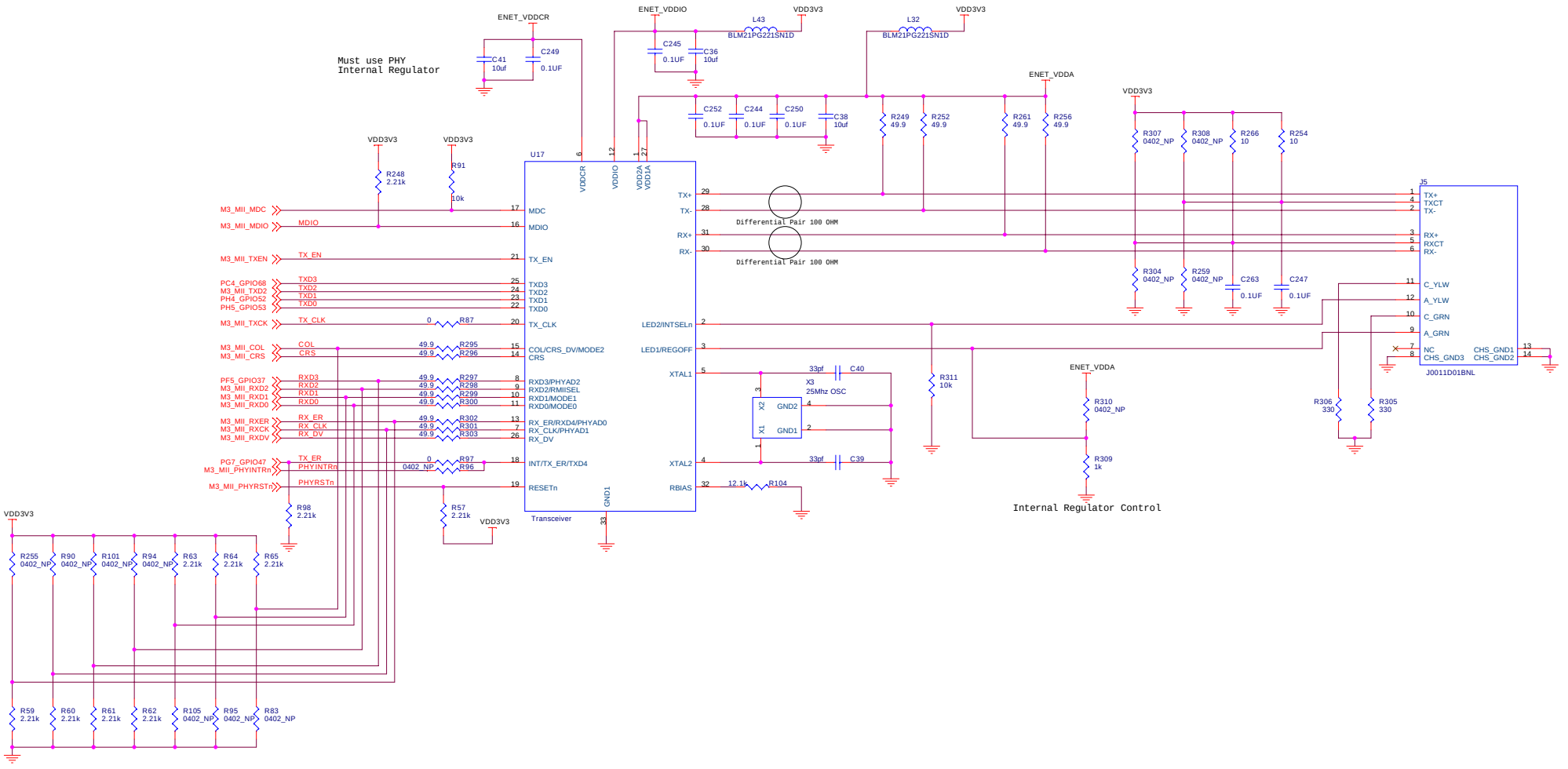
*Note: Pins 1 and 108 are 1.8-V Digital Logic Power Pins - no supply needed when using internal VREG18.
*Note: pins 11, 24, 55, 58, 66, 75, 99, 91, and 90 are 1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12.



Title: USB H/D		
Page Contents: USB uAB Conn, USB Device Power Switch		
Date: Wednesday, February 01, 2012		
Rev: B	**Size:** B	**Sheet** 3 **of** 6



Title:	ISO JTAG USB
Page Contents:	USB-to-JTAG, digital iso, serial debug
Date:	Wednesday, February 01, 2012
Rev: B	**Size:** C — **Sheet** 4 **of** 6



Title:	PHY #1 + MAG (SMSC)
Page Contents:	MII connections for external PHY
Date:	Wednesday, February 01, 2012
Rev: B	Size: C
Sheet 5 of 6	

Rev B - changes:

1) R96 is now NP
2) R97 is now populated
3) Added a pull-down (R98) on TX_ER (PG7_GPIO47)
4) Added 10k pull-ups (R243 and R244) on PC6_GPIO70 and PC6_GPIO70 so the LEDs are off by default.
5) Renamed headers to be sequential
6) Added a GND TP on the ISO (TP19) and non-ISO (TP20) sides
7) Switched around the analog signal mapping.
8) Changed the ref des for the LEDs and switches to match other boards.
9) Increased input cap to the DC-DC (C109) from 4.7uF to 10uF.
10) Changed the ADC to DIMM signals and added A.GPIO loop back for Tz inputs

ASSY Rev C - changes:

PWB REVISION C

ASSY Rev D - changes:

PRODUCTION RELEASE

PWB REVISION C

ASSY Rev E - changes:

CHANGE ADC CAPACITOR VALUES

PWB REVISION C

ASSY F - changes:

CONVERTED LAYOUT AND SCHEMATIC TO ALLEGO FOOTPRINTS

INCREASED OPTO ISOLATION

PROTOTYPE RUN ONLY

PWB REVISION D

ASSY G - RELEASE 2.00

UPDATED SILKSCREEN CHANGES ON ASSY F PROTOTYPE TO CORRECT MISTAKES

TEXAS INSTRUMENTS

Title:	CONCERTO DIMM 100
Page Contents:	REVISIONS
Date:	Wednesday, February 01, 2012
Rev: G	**Size:** C **Sheet** 6 **of** 6