

Notes:

- 1) Printed circuit board is controlled impedance.
- 2) Put multiple vias on Sonata's power pad for heat dissipation.
- 3) J6 and J8 to J19 are 2mm pitch and 0.8mm diameter.

DIFFERENTIAL PAIRS

PAGE 2 - 90 OHM

PG2\_GPIO42  
PG5\_GPIO45

PAGE 3 - 90 OHM

M3\_USB0DM  
PG5\_GPIO45

PAGE 7 - 100 OHM

TX+  
TX-  
  
RX+  
RX-

SCHEMATIC CONTENTS

- SH01 - TITLE
- SH02 - CONCERTO
- SH03 - USB H/D
- SH04 - ISO JTAG USB
- SH05 - PHY #1 + MAG (SMSC)
- SH06 - REVISION HISTORY

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	Concerto DIMM-100 CC	4-13-2010	
B	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
C	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
D	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
E	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
F	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		
G	Concerto DIMM-100 CC SEE LAST PAGE FOR CHANGES		

REVISION STATUS OF SHEETS							DWN	DATE
REV							CHK	DATE
SH							ENGR	DATE
REV							ENGR-MGR	DATE
SH							QA	DATE
REV	G	A	A	A	A	G	MFG	DATE
SH	1	2	3	4	5	6	RLSE	DATE
							APPLICATION	
							NEXT ASSY	USED ON

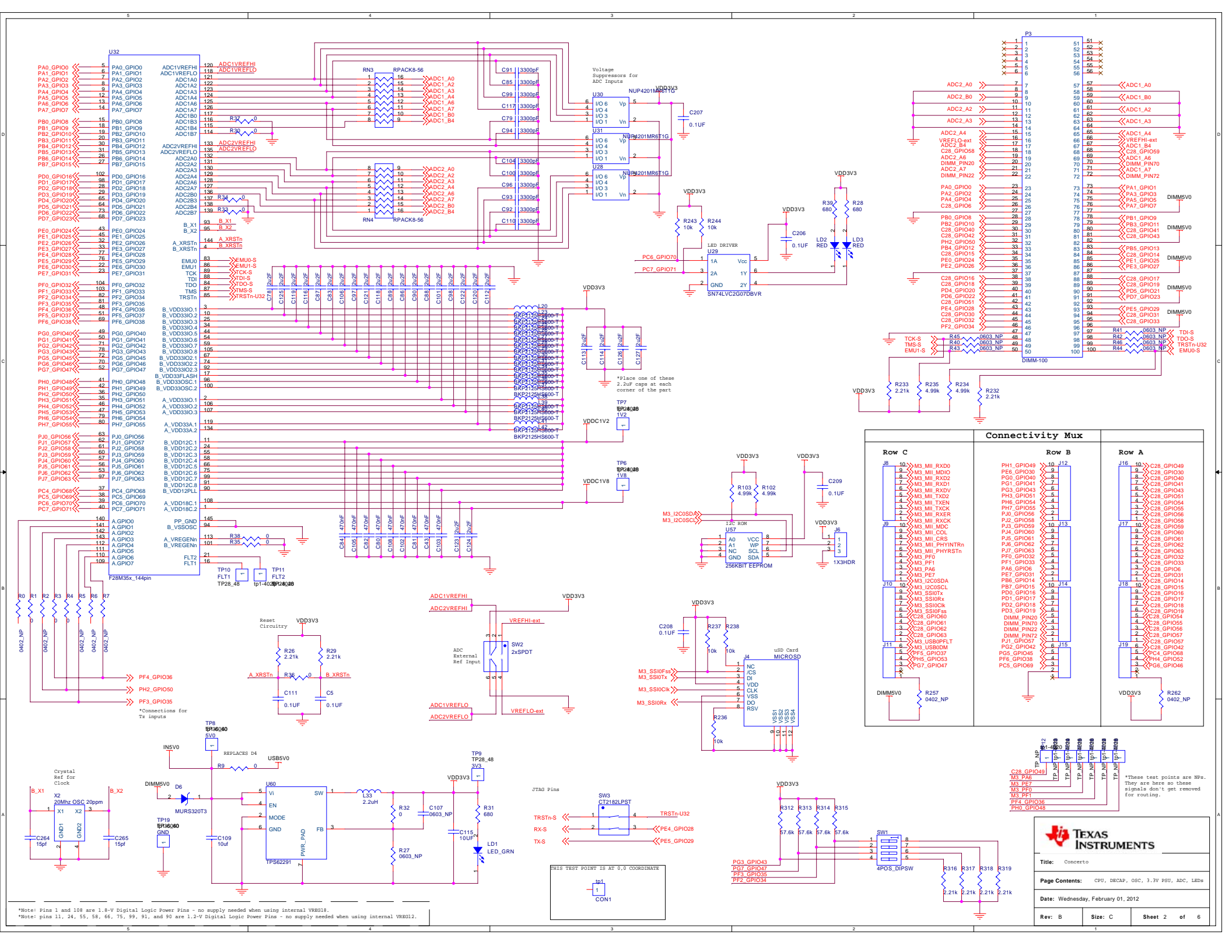


Title: Cover Page

Page Contents: Layout info, schematic notes

Date: Wednesday, February 01, 2012

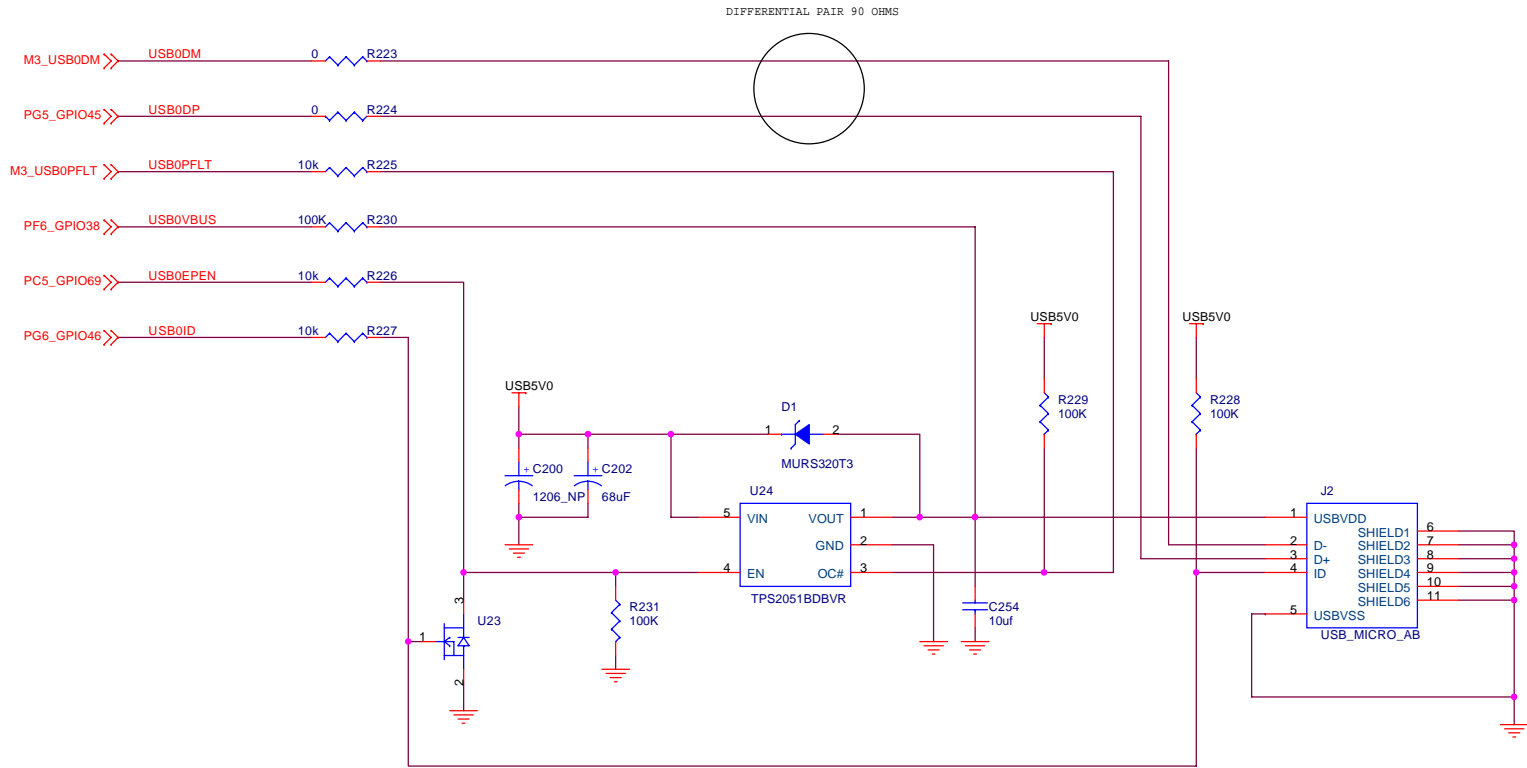
Rev: G      Size: B      Sheet 1 of 6



\*Note: Pins 1 and 108 are 1.8-V Digital Logic Power Pins - no supply needed when using internal VREG18.  
 \*Note: pins 11, 24, 55, 58, 66, 75, 99, 91, and 90 are 1.2-V Digital Logic Power Pins - no supply needed when using internal VREG12.

Row C	Row B	Row A
J8 10	PH1_GPIO4	C28_GPIO49
9	PE6_GPIO30	C28_GPIO30
8	PG0_GPIO40	C28_GPIO40
7	PC1_GPIO41	C28_GPIO41
6	PG3_GPIO43	C28_GPIO43
5	PH3_GPIO51	C28_GPIO51
4	PH6_GPIO54	C28_GPIO54
3	M3_MII_TXCN	C28_GPIO55
2	M3_MII_TXCK	C28_GPIO56
1	M3_MII_RXER	C28_GPIO58
10	M3_MII_RXCK	C28_GPIO59
9	M3_MII_MDC	C28_GPIO60
8	M3_MII_C0L	C28_GPIO61
7	M3_MII_CRS	C28_GPIO62
6	M3_MII_PHYINTRn	C28_GPIO63
5	M3_MII_PHYRSTn	C28_GPIO64
4	M3_PFD	C28_GPIO65
3	M3_PFI	C28_GPIO66
2	M3_PAE	C28_GPIO67
1	M3_PET	C28_GPIO68
10	M3_12CSDA	C28_GPIO69
9	M3_12CSCL	C28_GPIO70
8	M3_SSI0TX	C28_GPIO71
7	M3_SSI0RX	C28_GPIO72
6	M3_SSI0FS	C28_GPIO73
5	C28_GPIO80	C28_GPIO74
4	C28_GPIO81	C28_GPIO75
3	C28_GPIO82	C28_GPIO76
2	TMS28_GPIO83	C28_GPIO77
1	M3_SBDPFLT	C28_GPIO78
10	PG2_GPIO42	C28_GPIO79
9	PH5_GPIO37	C28_GPIO80
8	PH4_GPIO38	C28_GPIO81
7	PH3_GPIO39	C28_GPIO82
6	PG7_GPIO47	C28_GPIO83



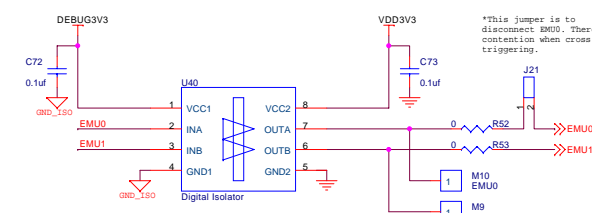
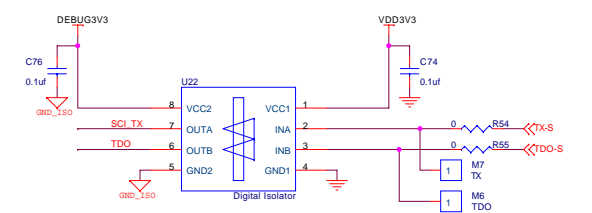
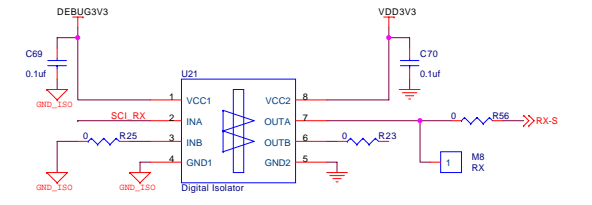
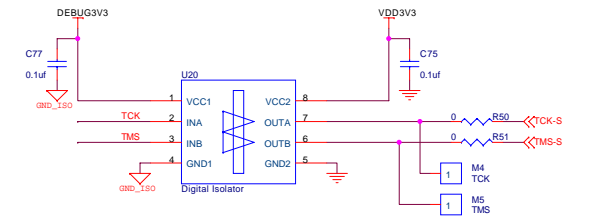
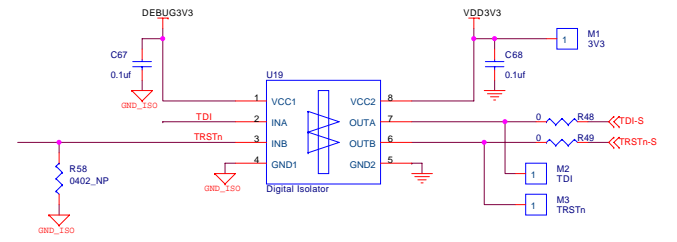
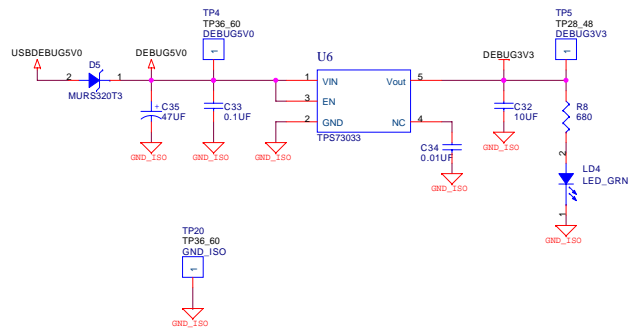


Title: USB H/D

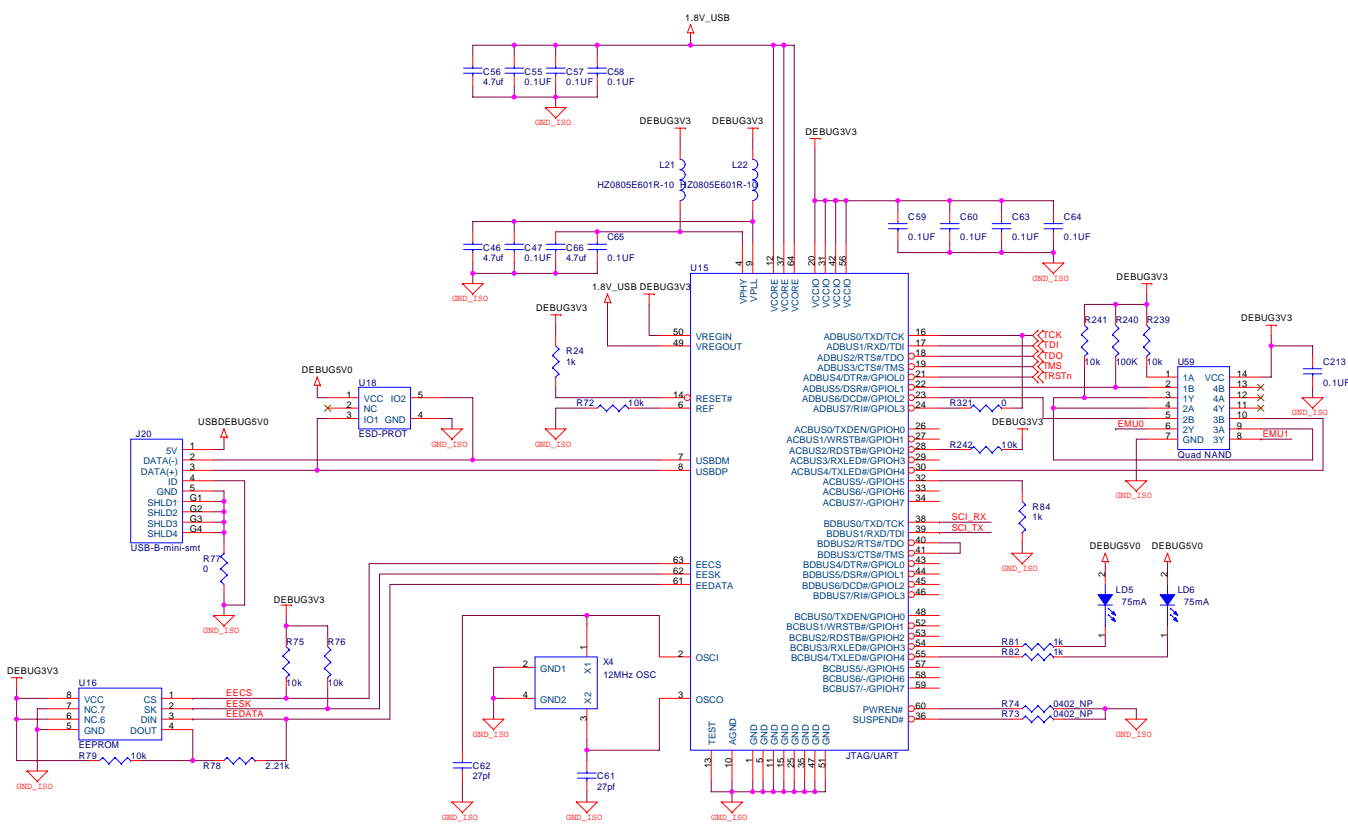
Page Contents: USB uAB Conn, USB Device Power Switch

Date: Wednesday, February 01, 2012

Rev: B      Size: B      Sheet 3 of 6



THIS CAP NEEDS TO EXTEND OVER THE ISOLATION GAP SIZE IS EXTREMELY IMPORTANT





Rev B - changes:

- 1) R96 is now NP
- 2) R97 is now populated
- 3) Added a pull-down (R98) on TX\_ER (PG7\_GPIO47)
- 4) Added 10k pull-ups (R243 and R244) on PC6\_GPIO70 and PC6\_GPIO70 so the LEDs are off by default.
- 5) Renamed headers to be sequential
- 6) Added a GND TP on the ISO (TP19) and non-ISO (TP20) sides
- 7) Switched around the analog signal mapping.
- 8) Changed the ref des for the LEDs and switches to match other boards.
- 9) Increased input cap to the DC-DC (C109) from 4.7uF to 10uF.
- 10) Changed the ADC to DIMM signals and added A.GPIO loop back for Tz inputs

ASSY Rev E - changes:

CHANGE ADC CAPACITOR VALUES

PWB REVISION C

ASSY Rev C - changes:

PWB REVISION C

ASSY F - changes:

CONVERTED LAYOUT AND SCHEMATIC TO ALLEGO FOOTPRINTS

INCREASED OPTO ISOLATION

PROTOTYPE RUN ONLY

PWB REVISION D

ASSY Rev D - changes:

PRODUCTION RELEASE

PWB REVISION C

ASSY G - RELEASE 2.00

UPDATED SILKSCREEN CHANGES ON ASSY F PROTOTYPE TO CORRECT MISTAKES