Letters

A Modified Dual-Output Interleaved PFC Converter Using Single Negative Rail Current Sense for Server Power Systems

Serkan Dusmez, Shamim Choudhury, Manish Bhardwaj, and Bilal Akin

***Abstract*—The interleaved PFC topologies have been widely used since they allow for smaller components, improved thermal performance, better transients, and reduced current ripple. In this letter, conventional two-phase interleaved universal input PFC topology is modified to obtain dual independent outputs for server applications, which minimizes the transient effects of interleaving legs on each other through two split dc buses. A new digital control method using only one current sensor located on the negative dc rail is proposed to control the dual-output interleaved PFC converter. Double-loop digital control of two interleaving stages is implemented using a single low-cost microcontroller (TMS320F28027-PiccoloA). In the proposed control technique, the control circuitry, input voltage, and current sensing circuits are shared between two PFC power stages, which minimize the size and the cost of the design significantly.**

***Index Terms*—AC–DC conversion, digital control, interleaved converter, power factor correction (PFC), server power supply.**

I. Introduction

THE boost-type power factor correction (PFC) circuit, consisting of a diode bridge followed by a dc–dc boost converter [1]–[3], is the widely preferred state-of-art converter topology used in the front-end PFC stage in server power supplies. For dual-output server power supplies, two independent PFC converters followed by step-down converters can be utilized; however, this would result in high cost and size. Instead, both the PFC stage and the second stage dc/dc converter can be split into multiphases, by which the phases can be interleaved for better system performance [4]–[11]. This technique brings several advantages for high-power systems. Since the power is processed by multiple converters, and the current of each converter is halved, the conduction losses for each MOSFET, given by I^2R, are reduced by a factor of four. In addition, the amplitude of the overshoots during the transients can be reduced, and better transient response can be achieved. However, if the second stage dc–dc converters are connected in parallel to the same dc link, the transients of the first converter affect the operation of the second converter or vice versa as they share the same dc bus [12]–[14]. In order to alleviate the mutual interference during transients, the traditional interleaved PFC stage is modified to have two independent dc links as shown in Fig. 1.

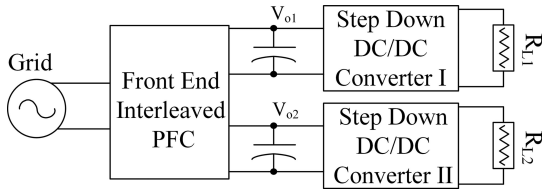

Fig. 1. Modified dual-output interleaved PFC converter.

With the advent of low-cost, high-performance microcontrollers (MCUs), new approaches to power converter control are possible [15]–[18]. MCU-based digital control eliminates control complexities and difficulties in realization of the control for interleaved PFC circuits, while providing power supply designers a tool for flexible control design, high-frequency operation, improved performance, and increased system integration [18]. The extended computation capability of such MCUs allows implementation of sophisticated nonlinear control algorithms, integrate multiple converter control into the same processor, and optimize the total system cost. The advantages of a digitally controlled interleaved dual output topology over the conventional topology controlled by two analog PFC controllers operated without phase shift can be summarized as follows: 1) lower input current ripple due to ripple cancellation effect even if two output voltages are different, 2) two smaller inductors in comparison to one bulky inductor for a given input current ripple criteria, 3) reduced zero crossing distortions as digital implementation is more flexible in implementing advanced techniques such as introducing an offset signal to the current feedback signal, 4) less number of feedbacks and associated analog signal conditioning circuits, and 5) autotuning of controller coefficients with respect to load and line voltage.

The digital control of the PFC boost converter as well as the interleaved converter has been explored in [9] and [10]. Following similar digital control approach for the modified dual-output PFC stage would require two inductor current sensors. This paper proposes a cost-effective method to control two-phase interleaved PFC stages with dual independent outputs by only sensing the negative rail current through a current sense

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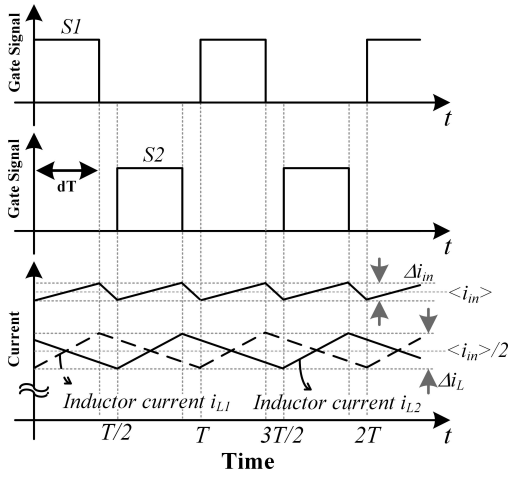


Fig. 2. Interleaved PFC converter waveforms.

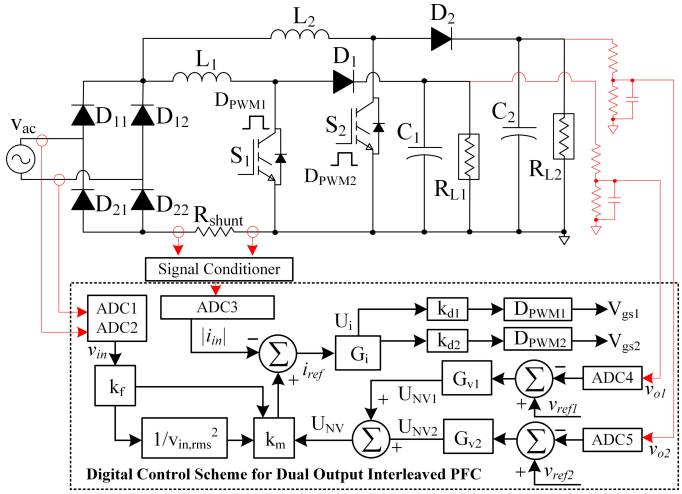


Fig. 3. Topology and digital control scheme of the dual-output PFC.

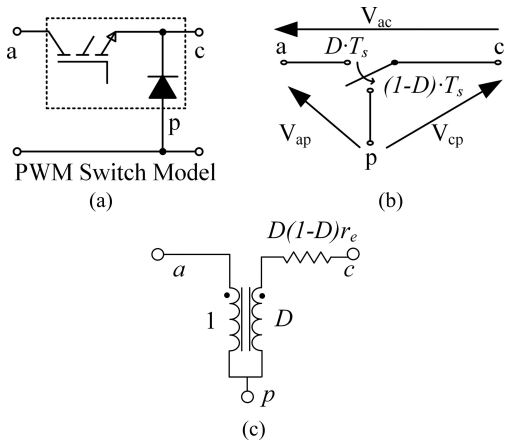


Fig. 4. PWM switch modeling. (a) Three-terminal model. (b) Invariant relationships. (c) Switch model for a fixed duty ratio.

resistor. The overall control algorithm is embedded in a single-low-cost MCU (TMS320F28027-PiccoloA).

II. Dual-Output PFC Power Stage

A. Interleaved Dual-Output PFC Circuit

The design of the PFC boost power stage is well known [15]. The main design challenge arises in the semiconductor selection and magnetics design. In high-power continuous conduction mode (CCM) designs, the boost diode operates under severe conditions. If the boost diode turn-off current can be decreased, both the stress on the diode and the electromagnetic interference performance can be significantly improved. In this regard, interleaving technique allows much higher inductor ripple current thereby resulting in the lower diode current at the instant of turn-off. Although the high ripple current usually exhibits the disadvantage of increased filter requirements and higher peak current stress, these disadvantages can be alleviated thanks to the interleaving technique. The input current has lower ripple than its equivalent single stage due to the ripple current cancellation effect.

The switching scheme of the two-phase interleaved converter is given in Fig. 2. The control of the interleaved converter is based on shifting the phase of S_1 with respect to S_2 such that, in case two interleaving legs are operated in the CCM for the same output voltage, the ripples cancel out each other either completely or to some extent depending on the duty cycle ratio. However, it should be noted that for applications with different output voltages, and hence, different duty ratios, the improvement in the input current ripple would be less depending on the steady-state duty ratios of interleaving legs.

The basic circuit schematic, including the feedbacks and digital control scheme for two independent PFC outputs, is shown in Fig. 3. Each phase is employed to generate independent output voltages through separate output voltage sensing circuits and voltage control loops. Though the voltage loops are separate, only one current sensing resistor on the negative rail is used to control the total current drawn by the two PFC stages. In case two completely independent PFC circuits are utilized, each PFC stage would require four feedback signals (ac line voltage, ac neutral voltage, dc bus voltage, and PFC inductor current) for complete control of its voltage and current. As illustrated in Fig. 3, the proposed method requires a total of five signals sensing instead of eight in order to control two PFC stages. Thus, the proposed digital scheme allows controlling multiple PFC stage outputs with reduced number of signal sensing. Here, the ac voltage and line voltages are sensed through two pair of voltage-dividing resistors to avoid OPAMP. The output of the diode rectifier could have been sensed; however, the small capacitance across it would cause distortion in the signal.

In Fig. 3, the voltage loop controllers are G_{v1} and G_{v2} and the current loop controller is G_i. The individual duty ratio values are calculated from the voltage controller outputs and the combined pulse width modulation (PWM) duty as

$$d_1 = d\frac{U_{NV1}}{U_{NV1}+U_{NV2}} \tag{1}$$

$$d_2 = d\frac{U_{NV2}}{U_{NV1}+U_{NV2}}. \tag{2}$$

Here, d represents the combined PWM duty calculated from single-current controller output U_i, which is used to calculate

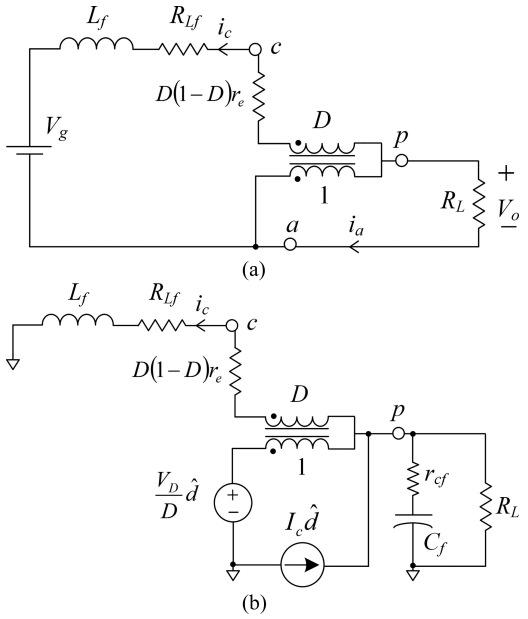


Fig. 5. Converter circuit models. (a) DC characteristics. (b) Control to output transfer function.

PWM duty of the individual PFC modules, d_1 and d_2. Equations (1) and (2) are represented by k_{d1} and k_{d2} gains in the figure.

B. DC and Small-Signal Modeling

A boost PFC rectifier is an equivalent of a dc–dc boost converter which is fed by a rectified voltage source. In order to model this boost converter, switch and diode pair is treated as a three-terminal switch, which allows quantifying the invariant relationships between the terminal currents and voltages. This model, illustrated in Fig. 4(a), is referred as the PWM switch model [19]. The terminal designations a, p, and c refer to active, passive and common, respectively. Fig. 4(b) presents the following invariant relationships:

$$i_a(t) = \begin{cases} i_c(t), & 0 \le t \le DT_s \\ 0, & DT_s < t \le T_s \end{cases} \tag{3}$$

$$v_{cp}(t) = \begin{cases} v_{ap}(t), & 0 \le t \le DT_s \\ 0, & DT_s < t \le T_s \end{cases}. \tag{4}$$

These relationships are valid for all essential PWM converters such as buck, boost, and buck/boost. With these equations and relations, the PWM switch can be modeled for a fixed duty ratio as in Fig. 4(c). If the duty ratio is perturbed, the response of the converter to perturbations in the duty ratio can be observed

$$\hat{i}_a = D\hat{i}_c + \hat{d}_a I_c. \tag{5}$$

$$\hat{v}_{cp} = D(\hat{v}_{ap} + I_c r_e(1-\hat{d}) - \hat{i}_c r_e(1-D)) + \hat{d}(V_{ap} - I_c r_e(1-D)) \tag{6}$$

where r_e is a general function which is equal to $r_{Cf}||R_L$, representing the output capacitor ESR and load resistor, R_L.

TABLE I
EXPERIMENTAL DESIGN PARAMETER

Component	Rating
Output Power *(P_o)*	375Wx2
Input Voltage *(V_{ac_rms})*	90-264V
Rated DC Bus Voltage *(V_{o1}=V_{o2})*	370V
Max. DC Bus Voltage *($1/K_{d1}$=$1/K_{d2}$)*	510V
Max. Input Voltage *(V_{ac_max})*	404V
Min. Input Voltage *(V_{ac_min})*	113V
Max. Input Current *($1/K_s$)*	19.8A
Boost Inductors *(L_1=L_2)*	150µH
DC Link Capacitors *(C_1=C_2)*	300µF
Efficiency Low/High Line	94%-96%
Switching Frequency *(f_{sw})*	200kHz
Current Loop Sampling Freq. *(f_i)*	100kHz
Voltage Loop Sampling Freq. *(f_v)*	50kHz

Reorganizing (6) to express $\hat{v}_{ap}$ yields

$$\hat{v}_{ap} = \frac{\hat{v}_{cp}}{D} + \hat{i}_c r_e(1-D) - V_D\frac{\hat{d}}{D} \tag{7}$$

where

$$V_D = V_{ap} + I_c r_e(1-2D). \tag{8}$$

Equations (6) and (8) contain the dc characteristics and small-signal model information of the PWM switch. The equivalent circuit models to extract dc characteristics and control to output transfer function of a boost converter are given in Fig. 5. From Fig. 5(b), the control to inductor current transfer function can be found as follows:

$$G_{id}(s) = \frac{\hat{i}_L}{\hat{d}} = \frac{V_o}{R_L(1-D)(1+r_{\rm eq})} \frac{(1-D)Z_{fo} + (2D-1)r_e + R_L(1-D)(1+r_{\rm eq})}{r_e D(1-D) + Z_{fi} + (1-D)^2 Z_{fo}} \tag{9}$$

$$r_{\rm eq} = \frac{r_{Lf}}{R_L(1-D)^2}\frac{r_e D}{R_L(1-D)} \tag{10}$$

$$Z_{fo} = \frac{R_L r_{Cf} C_f s + R_L}{R_L C_f s + r_{Cf} C_f s + 1} \tag{11}$$

$$Z_{fi} = r_{Lf} + sL_f. \tag{12}$$

C. Current and Voltage Loops

The current loop transfer function including the current compensator can be expressed in general form as in (13). Here, $G_i, G_{id,n}, G_{dly}$, and G_{fltr} represent the s-domain plant models for current compensator, power stage, computation delay, and low-pass filter, respectively. The low-pass filter is used to attenuate the frequencies greater than the Nyquist frequency such that sampling of the aliasing components of the signal is avoided. K_i is the current compensator gain, $K_{id,n}$ is the dc gain of the power stage, K_M is the modulation gain, $K_{d,n}$ represents gain used to calculate duty cycle, and K_s is the current scaling gain.

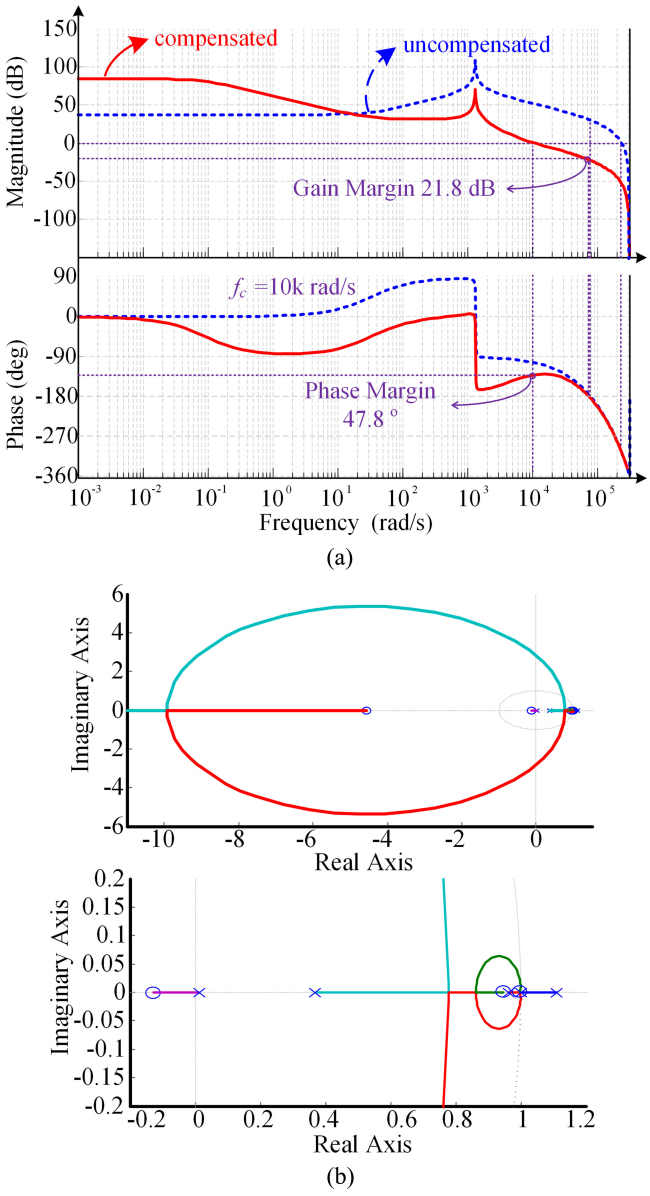


Fig. 6. Analysis of the current loop stage. (a) Bode diagrams of the compensated and uncompensated discrete time transfer functions. (b) Root locus plot of the closed-loop discrete system (overall and zoom-in profiles).

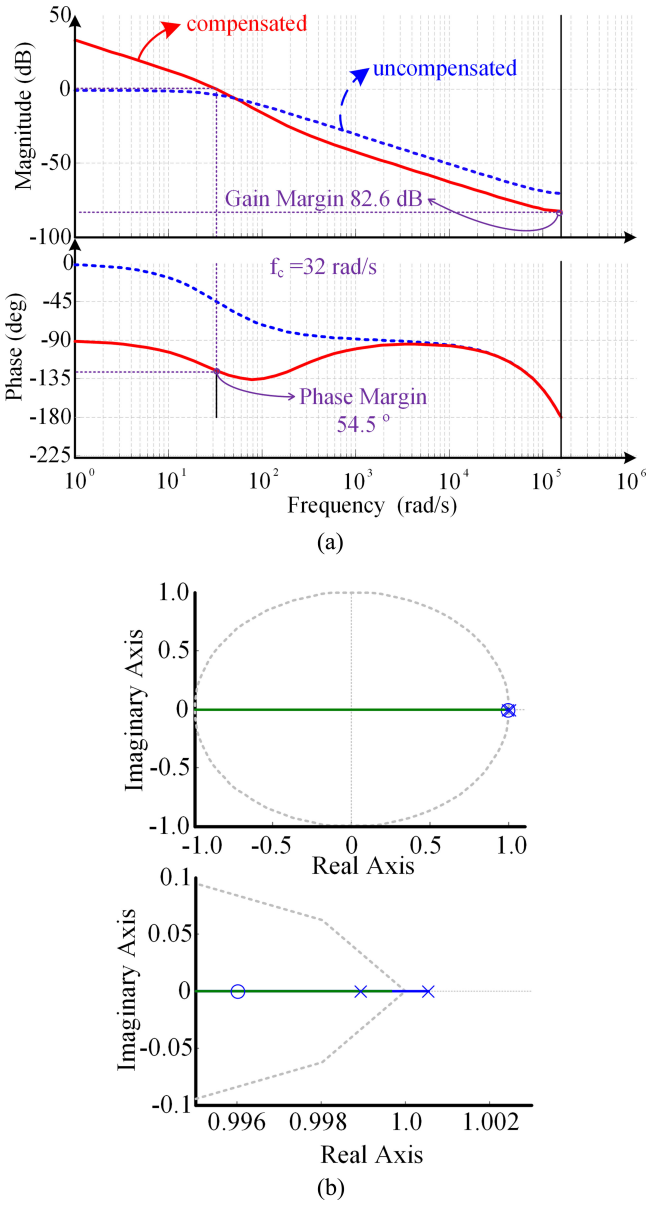


Fig. 7. Analysis of the voltage loop stage. (a) Bode diagrams of the compensated and uncompensated discrete time transfer functions. (b) Root locus plot of the closed-loop system (overall and zoom-in profiles).

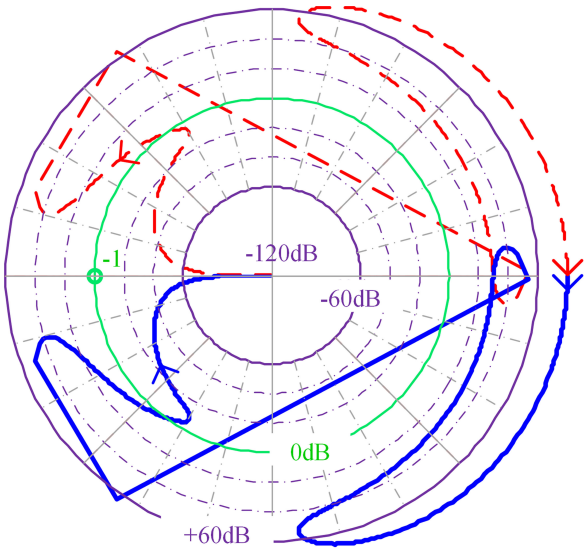
When the parameters of the converters are identical, the current compensator can be designed for a single power stage transfer function under full load. This also allows using combined duty cycle *d(s)*, instead of individual duty cycles $d_1(s)$ and $d_2(s)$, as $d(s) = d_1(s) + d_2(s)$. With this simplification, the current loop transfer function can be expressed as (14). Once the current loop is closed, each voltage loop power stage transfer function can be calculated as

$$T_{i,\mathrm{comp}}(s) = K_i G_i(s) \times K_s \left(K_{id,1} K_{d,1} G_{id,1}(s) + K_{id,2} K_{d,2} G_{id,2}(s)\right) \times K_M \times G_{\mathrm{dly}}(s) \times G_{\mathrm{fltr}}(s) \tag{13}$$

$$T_{i,\mathrm{comp}}(s) = K_i \frac{s/\omega_{zi} + 1}{s/\omega_{pi} + 1} \times K_{id} G_M K_s \frac{e^{-sT_d}(s/\omega_{zid} + 1)}{(s/\omega_{pid1} + 1)(s/\omega_{pid2} + 1)(s/\omega_f + 1)} \tag{14}$$

$$T_{v,n}(s) = \frac{K_m K_{d,n}}{K_f K_s} \times \left[\frac{V_{\mathrm{ac\,min}}}{V_{\mathrm{ac\,max}}}\right]^2 \frac{Z_{f,n}}{V_{o,n}} \tag{15}$$

where $Z_{f,n}$ represents the equivalent impedance of the parallel branch consisting of the bus capacitor, the PFC stage output impedance, and the load impedance; K_m and K_f denote $V_{\mathrm{ac\_max}}/V_{\mathrm{ac\_min}}$ and input voltage scaling factor $1/V_{\mathrm{ac\_max}}$, respectively [18].



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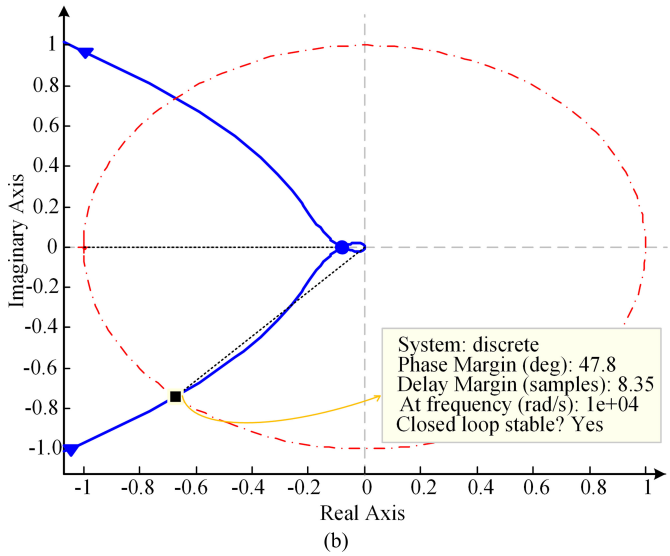
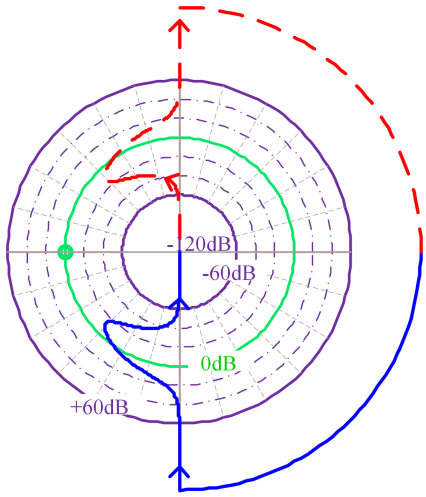


(b)

Fig. 8. Nyquist plot of the current loop for stability analysis. (a) Logarithmic form. (b) Zoom-in profile.



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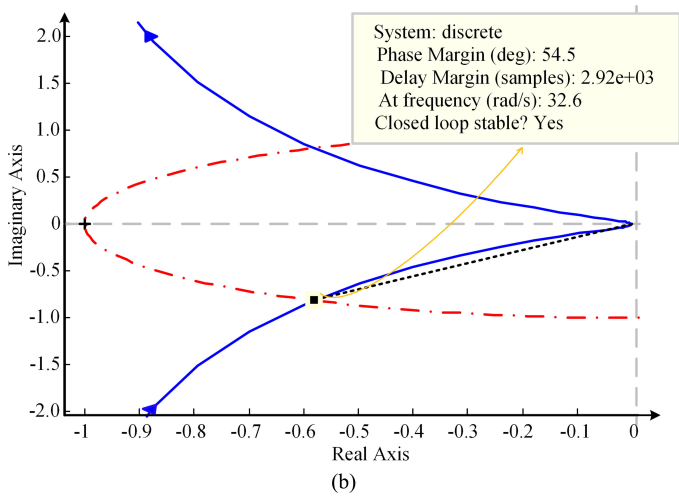


(b)

Fig. 9. Nyquist plot voltage loop for stability analysis. (a) Logarithmic form. (b) Zoom-in profile.

III. Design and Digital Implementation of the Controller

The system parameters used in the experiments are summarized in Table I. In this case, the corner frequency of this low-pass filter is chosen as 80 kHz. It should be noted that the chosen sampling scheme results in a computation delay of about half the sampling time, i.e., the computation delay is $T_d = T_{si}/2$. The parasitic elements r_{Cf} and r_{Lf} are set to zero for the sake of simplicity.

A. Compensator Design for Current and Voltage Loops

With given parameters in Table I, the current loop transfer function, $G_{id}(s)G_{\rm dly}(s)G_{\rm fltr}(s)$, can be expressed as (16).

The controller is first designed in continuous time and then converted to discrete domain using Z-transform. To decrease the gain at higher frequencies, and provide sufficient phase margin, a lag compensator that achieves a bandwidth of 10 krad/s, phase margin of 51°, and gain margin of 29.1 dB is designed in the continuous time domain. To achieve steady-state error of 0.01%, $T_i(s)$ is compensated with a gain of 206.8. The transfer function of the lag compensator in s-domain can be expressed as

$$T_i(s) = 48.35\frac{e^{-5\times10^{-6}s}(s/32.9+1)}{s^3/(1.414\times10^{11})+s^2/(1.767\times10^{6})+s/(4.587\times10^{4})+1} \tag{16}$$

$$G_i(s) = 206.8\frac{s/5599+1}{11.11s+1}. \tag{17}$$

The transfer function of the lag compensator in z-domain, discretized by the Tustin method, can be expressed as

$$G_i(z) = \frac{1.0576z-1}{309.5233z-309.5230}. \tag{18}$$

The bode diagrams of the compensated and uncompensated systems are presented for discrete time in Fig. 6(a). The controller is designed in the continuous time domain; however,

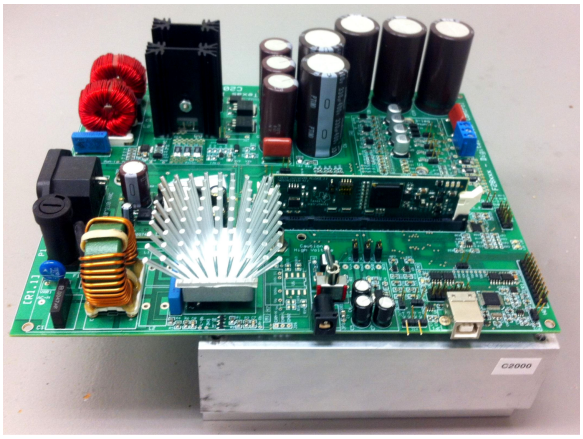


Fig. 10. Photo of the designed prototype.

bode and root locus plots are presented for discrete-time domain, which provides insightful information on the closed-loop system. The discrete-time bode plot exhibits a phase margin of 47.8° and gain margin of 21.8 dB, where the crossover frequency remains the same as in the continuous time domain. The difference is due to the approximation made during the continuous to discrete time conversion of the controller. In addition, the placement and trajectory of poles and zero of the closed-loop discrete function are given in Fig. 6(b). These diagrams are important to analyze the movement of the roots as well as determine the relative stability.

The voltage loop compensators are calculated separately according to the required dc bus voltages. With respect to the design specifications, the continuous transfer function of the voltage loop stage can be expressed as

$$T_{v1}(s) = \frac{1}{0.0304s + 1}. \tag{19}$$

The voltage loop compensator is adjusted to obtain a phase margin of 54° at a crossover frequency of 30 rad/s, and is found as

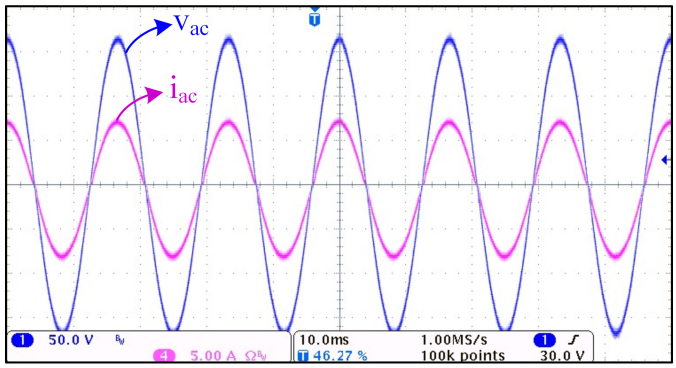
$$G_{v1}(s) = \frac{0.25s + 50}{s}. \tag{20}$$

The voltage compensator is approximated to discrete time with a sampling frequency of 50 kHz using the Tustin method, which is found as

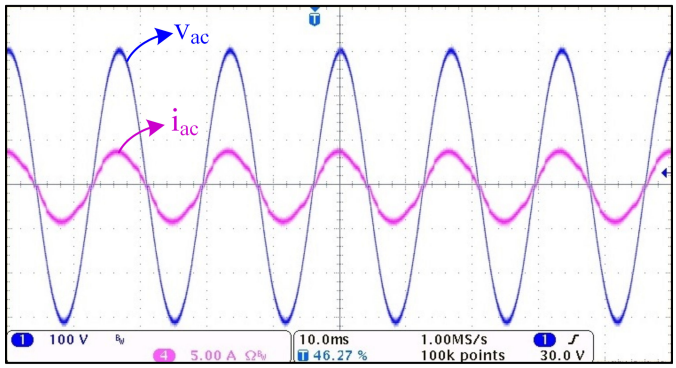
$$G_{v1}(z) = \frac{0.2505z - 0.2495}{z - 1}. \tag{21}$$

The bode plots to observe the cutoff frequency and the phase margin of the compensated system in discrete time, and the zero-pole placement to observe the movement of zero and poles are given in Fig. 7 . The second PFC stage continuous time transfer function $T_{v2}(s)$ and voltage compensator $G_{v2}(s)$ are calculated in a similar manner. Likewise, the designed controller can be approximated to discrete-time using the Tustin method.

To analyze the stability of the closed-loop system, the Nyquist diagrams are plotted for both voltage and current open-loop transfer functions of the compensated system in discrete time, as given in Figs. 8 and 9, respectively. The Nyquist plots for the



(a)



(b)

Fig. 11. Experimental results of the input voltage and the input current. (a) $V_{\mathrm{in,rms}} = 120$V [50 V/div], [5 A/div]. (b) $V_{\mathrm{in,rms}} = 220$V [100 V/div],[5 A/div].

current and voltage loops are plotted both in logarithmic form, and in-zoom profile. From these plots, the following conclusions are derived for both current and voltage loops: 1) there are no poles in the right-half-plane (RHP) of an open loop; 2) there is no net encirclements around –1 point; 3) there are no poles in RHP of the closed-loop system; and 4) there are no closed-loop poles on the imaginary axis. Therefore, it can be concluded that both closed-loop systems are asymptotically stable.

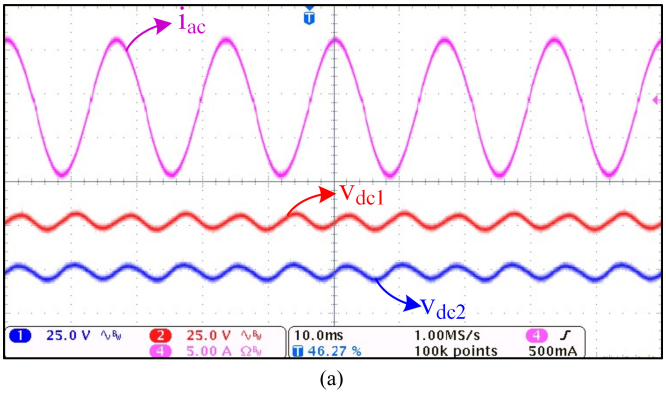
B. Experimental Results

The digital controllers in the discrete time domain have the following form:

$$G_d(z) = \frac{U(z)}{E(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 - a_1 z^{-1} - a_2 z^{-2}} \tag{22}$$

where *U(z)* is the controller output and *E(z)* denotes the error. The recursive form of the compensator can be expressed by the difference equation as (23) [20].

The designed digital controller is implemented in the software and embedded in TMS320F28027-PiccoloA. A 750-W universal input interleaved PFC converter prototype, shown in Fig. 10, has been designed and tested to prove the proposed dual-output concept with negative rail dc current sensing. The experimental results showing the input voltage and current waveforms at 635 W are shown in Fig. 11. The converter has been tested under both low and high lines, which maintains output dc bus voltages



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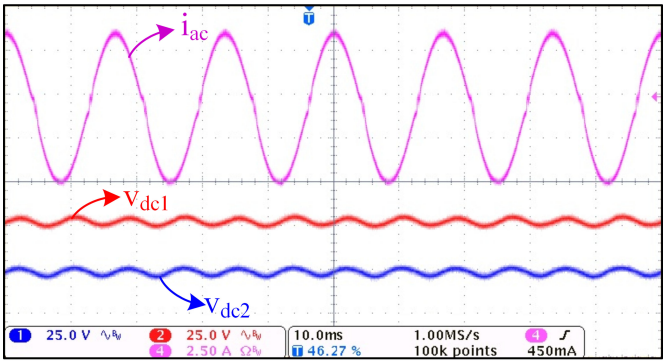


(b)

Fig. 12. Experimental results of the input current and dc bus voltages. (a) $P_o = 650\,\mathrm{W}$, [25 V/div], [5 A/div]. (b) $P_o = 325\,\mathrm{W}$, [25 V/div], [2.5 A/div].

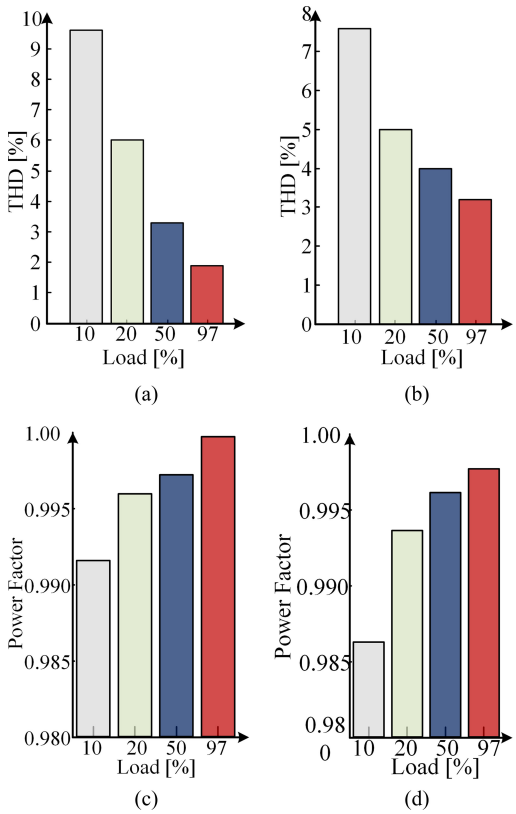
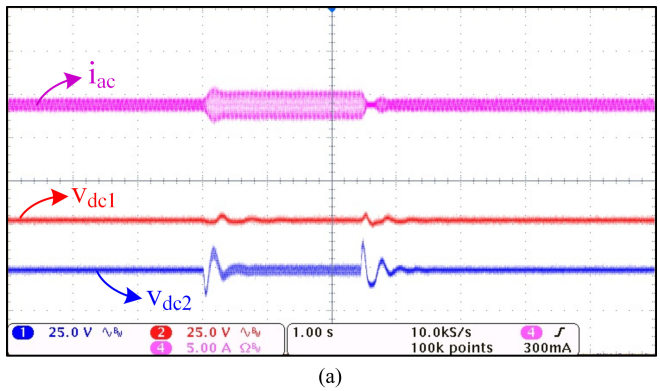


Fig. 13. Total harmonic distortion (THD) and power factor at various load power. (a) THD at 120 V. (b) THD at 220 V. (c) Power factor at 120 V. (d) Power factor at 220 V.

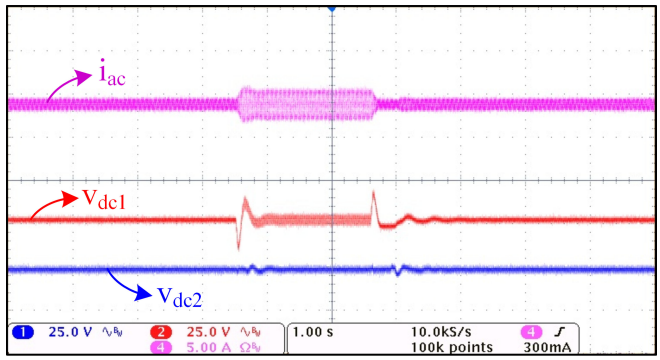
at 370 V. The high power factor can be seen from the overlap of the zero-crossings of current and voltage.

In Fig. 12, the input current and dc bus voltage ripples are given for two different output powers. The output voltage waveforms are shown in the ac mode. The input voltage is 120 V and output voltages are set to 370 V. Fig. 12(a) presents the waveforms when the output power is 650 W. In this case, the power factor is 0.999 and the peak-to-peak output voltage ripple is around 10 V. In Fig. 12(b), the output power is 365 W. For this case, the power factor is 0.996 and the peak-to-peak output voltage ripple is around 7.0 V. The recorded total harmonic distortion and power factor values corresponding to different loading conditions at high- and low-line voltages are provided in Fig. 13. The operation of the converter is in compliance with the EIC standards.

Fig. 14 shows the transient response of the system to step load variation. The loads connected to the first output $(R_L 1)$ and second output $(R_L 2)$ are varied with 160 W step as shown in Fig. 14(a) and (b), respectively. As seen from the figure, the transients on each output are handled successfully with minor disturbance on the other output. The mean values of the dc-link voltages are approximately 368 V at steady state, corresponding to a steady-state error of 0.5%. The experimental results demonstrate the effectiveness of the proposed control scheme. These waveforms also validate the proposed scaling scheme where the PWM duty ratio for each PFC stage is calculated from the combined PWM duty ratio (output of the single current controller)



(a)



(b)

Fig. 14. Transient response of the digital controller to step load variation. (a) $R_L 1$ is varied [25 V/div], [5 A/div]. (b) $R_L 2$ is varied [25 V/div], [5 A/div].

and the voltage controller outputs. The calculated PWM duty ratio is then applied to each PFC switch in order to steer an appropriate current through individual PFC inductors

$$U(k) = a_1 U(k-1) + a_2 U(k-2) + b_0 E(k) + b_1 E(k-1) + b_2 E(k-2). \quad (23)$$

IV. Conclusion

This letter proposes a digital control scheme for dual-output boost interleaved PFC converter with minimal computational burden, board size, cost, and hardware components. The presented dual-output architecture minimizes the transients seen at the first dc bus caused by the load variations on the second dc bus or vice versa. This feature is desirable in server applications where the load is sensitive to transients. In the proposed control scheme, the control electronics, the input voltage, and current sensing circuits are all shared between two interleaving power stages. This approach combines the advantages of dual-output PFC converters with reduced signal sensing, all implemented in a single digital controller. A 750-W universal input prototype has been designed to validate the effectiveness of the proposed architecture as well as the control technique based on single current sensing. The results exhibit high power factor, fast response, and minimized interference of dc-bus voltages during instantaneous load variations.

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