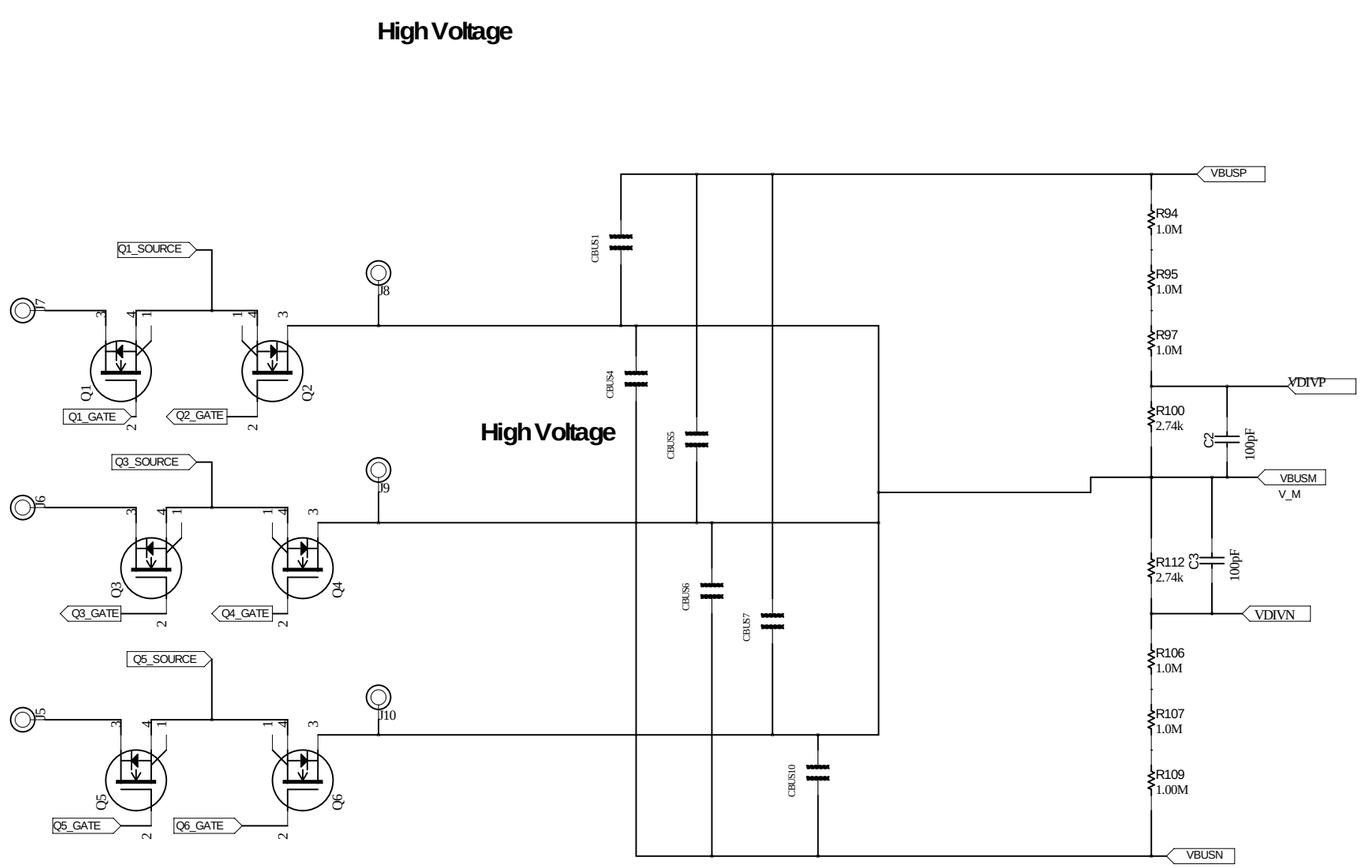
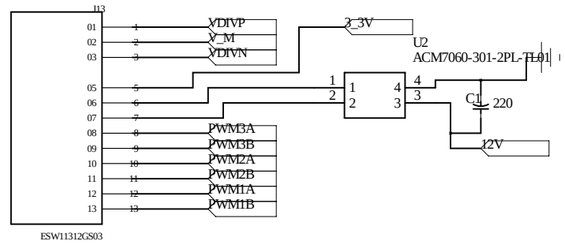
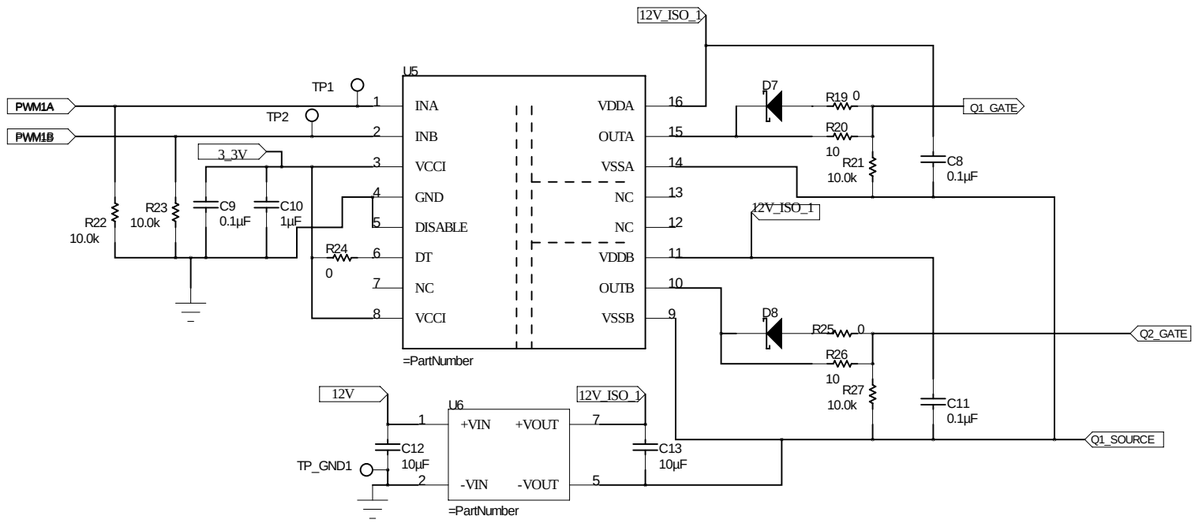
PCB Rule
All the nets higlighted are high current carrying and high voltage carrying, appropriate clearance and width is needed

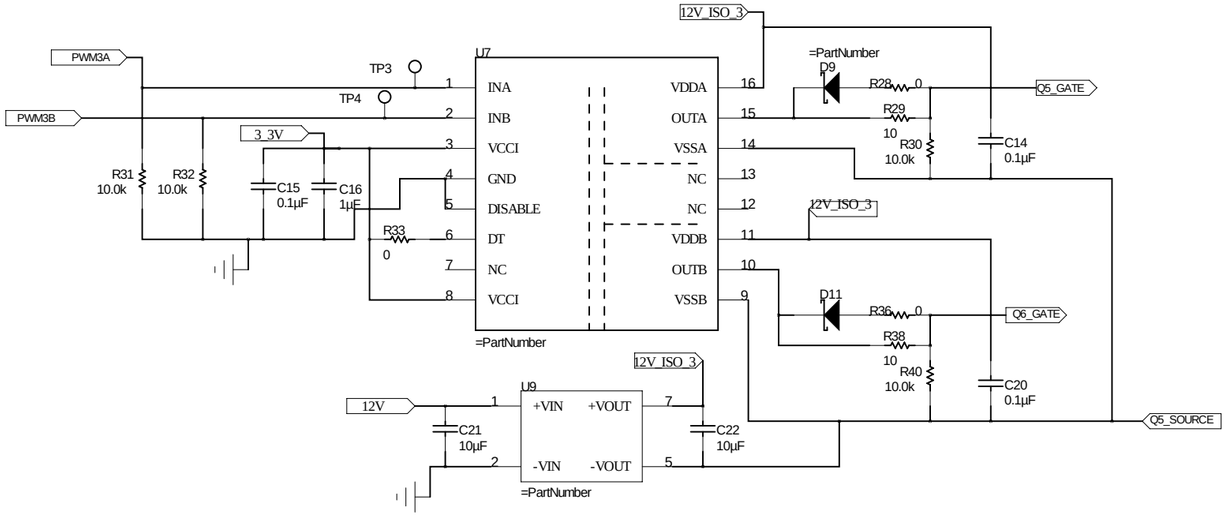


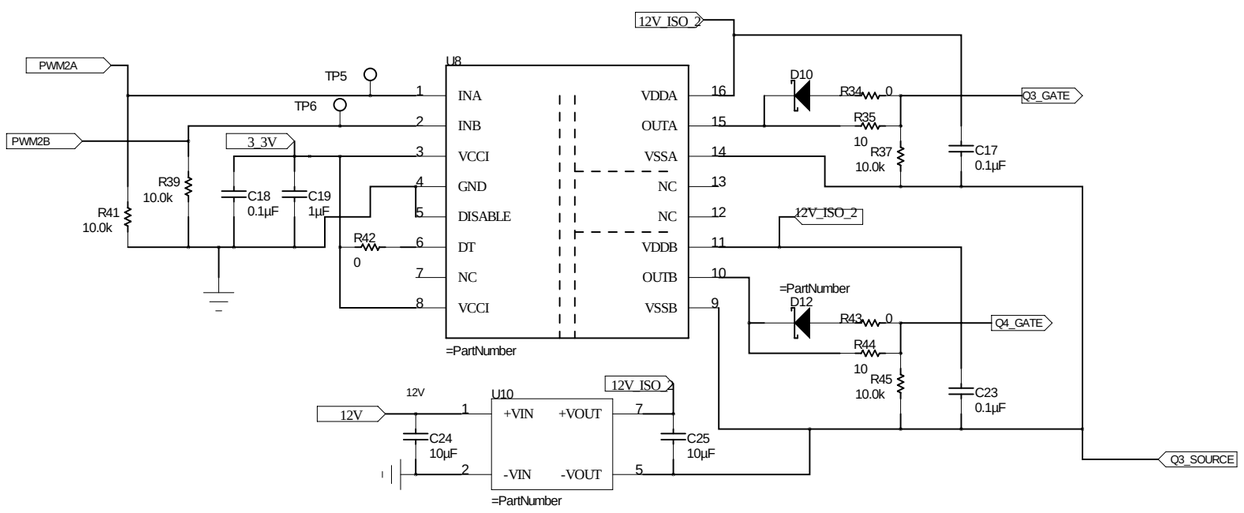


PCB Rule
Place U1 Close to Q1 and Q2, and minimize distance between Q1_Gate and U1-OUTA, Q2-Gate and U1-OUTB , VSS1 &VSS2 and Q1-Source



High Voltage





PCB Rule
Place U3 Close to Q5 and Q6, and minimize distance between Q5_Gate and U3-OUTA, Q6-Gate and U3-OUTB , VSS1 &VSS2 and Q5-Source

PCB Rule
Place U2 Close to Q3 and Q4, and minimize distance between Q3_Gate and U2-OUTA, Q4-Gate and U2-OUTB , VSS1 &VSS2 and Q3-Source

Orderable:		Designed for:	Mod. Date: Not shown in title block
TID #:		Project Title:	
Number:	Rev:	Sheet Title: PWM Gate Drivers	
SVN Rev:		Assembly Variant:	Sheet: 2 of 2
Drawn By: Manish Bhardwaj		File: Not shown in title block	Size: B
Engineer:		Contact:	http://www.ti.com