1

2 IC Package Mounting Considerations

2.1 Ball Grid Array (BGA) Packages

Several C2000 processors use variants of the 0.8-mm pitch Ball Grid Array (BGA) package. These include 289-pin Concerto PRP package and 337-pin Delfino ZWT package. In order to achieve good manufacturability results when soldering these packages to printed circuit boards it is critical to choose proper ball land and via dimensions, as well as correct opening dimensions for the solder mask and solder paste stencils. Solder mask is the typically green layer that protects most of the top and bottom surfaces of the board except where there are exposed lands (sometimes also called pads) to be soldered to board components. Solder paste stencils have openings through which solder paste is deposited on the exposed component lands (areas not covered by solder mask) prior to board assembly and soldering. The Figure 2-1 represents the 289-pin PRP package, but the same recommended dimensions apply to both the PRP and the ZWT packages. See SPRAA99B for additional information on PCB design considerations.

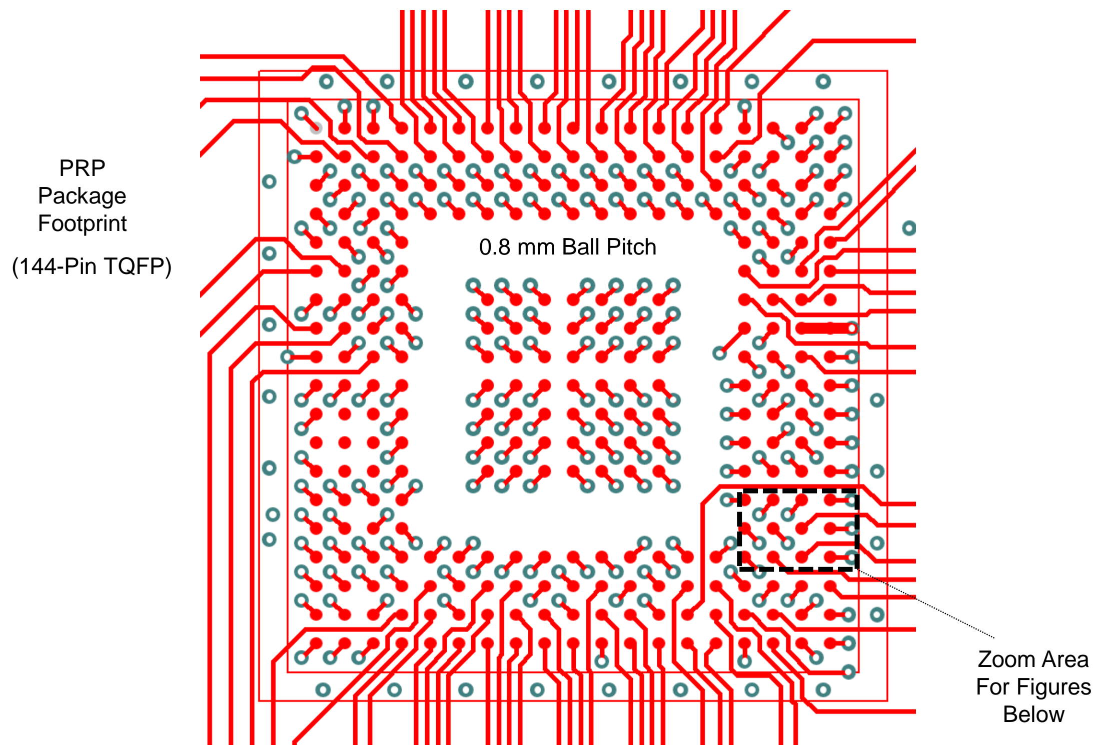

Figure 2-1 Example of PRP Package Footprint (289-Pin BGA with 0.8mm Pitch)

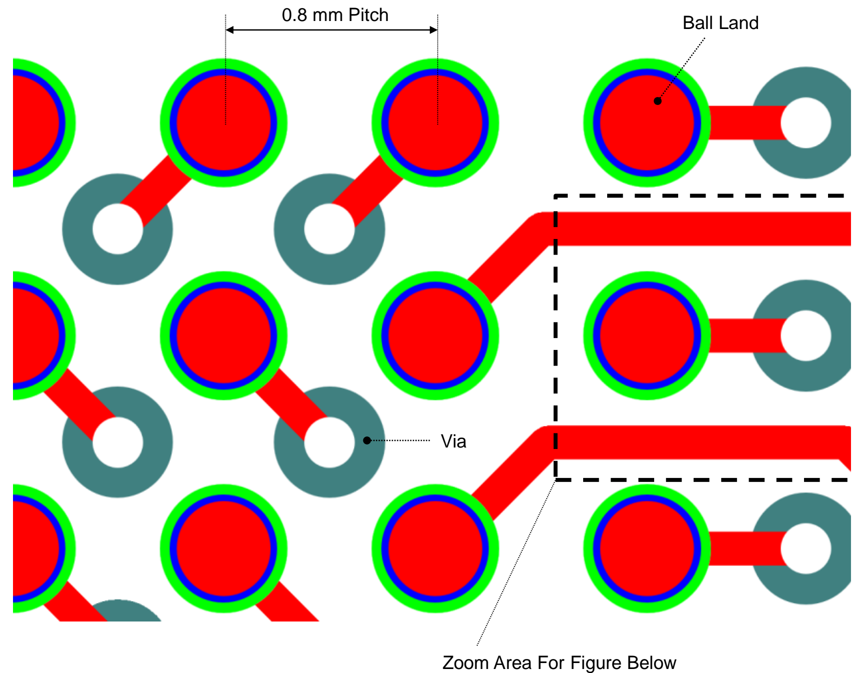

Figure 2-2 PRP Package Footprint Example – Medium Zoom

The PCB land size must be matched to the package via to which the ball is attached. This ensures that after reflow (soldering process) the resulting solder ball is as round as possible. This in turn reduces thermal and mechanical stresses and prevents premature cracks in the BGA package balls due to a difference in coefficient of thermal expansion between PCB substrate and BGA, or flexing and vibration. For 0.8-mm BGA packages the recommended PCB land diameter is between 0.40 mm and 0.50 mm (15.7 mils – 19.9 mils). Note that the land diameter is not the same as the ball diameter – it is smaller than the ball diameter. The sample design shown in Figure 2-4 and Figure 2-5 uses a 14 mil PCB land.

The solder mask covering the 0.8 mm BGA package footprint has a void around each ball land to permit its soldering to the package ball. This opening depends on the board manufacturer's process, but typically it extends about 1-2 mils beyond the edge of the land when the ball lands are Non Solder Mask Defined (NSMD). The sample design shown in Figure 2-4 and Figure 2-5 uses a 20 mil solder mask opening around the 16 mil diameter land. If the solder mask opening specified by board design is too small for a particular board manufacturing process, the manufacturer's software will automatically adjust the solder mask to give it proper clearances.

There are 2 types of BGA ball lands – Solder Mask Definded (SMD) and Non Solder Mask Defined (NSMD). Figure 2-3 shows the difference between the two.

SMD ball lands have the outside portion of the land covered by solder mask – thus the exposed ball land is defined by the opening in the solder mask. The SMD lands are typically used for BGAs with pitch smaller than 0.8 mm (such as 0.4-mm BGAs) as these lands have better resistance to lifting off the board (due to their larger size) when stressed by external impact events.

When using NSMD ball lands, the solder mask opening is larger than the ball land, thus the exposed ball land is not defined by the opening in the solder mask. NSMD lands are recommended for 0.8-mm pitch BGAs for the following reasons: they produce a better solder joint because of exposed side edges, their size and location registered by optical exposure is better controlled than the solder mask deposition method, and their smaller size leaves more room for signal routing in tight spaces under the BGA package.

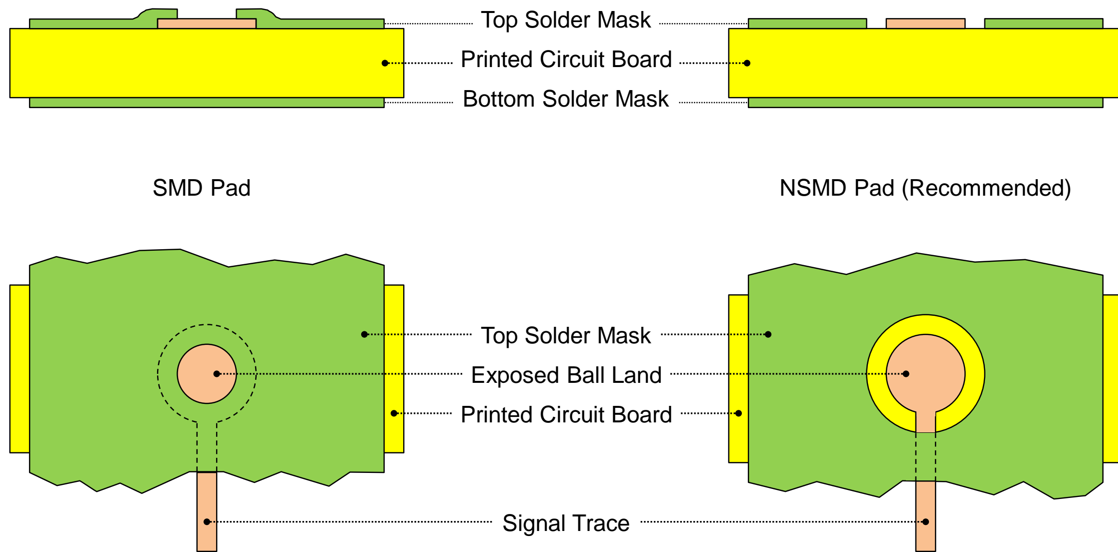

Figure 2-3 SMD and NSMD BGA Landing Pads

The solder paste stencil for a BGA package has an opening for each PCB land through which a proper amount of solder paste is dispensed just prior to board assembly and reflow. The amount of dispensed solder paste is proportional to the thickness of the stencil and the diameter of the stencil opening. Assuming the stencil thickness 5 mils the recommended stencil opening for each of BGA lands is 17 mils. The sample design shown in Figure 2-4 and Figure 2-5 uses the 17-mil stencil opening. Using a thicker 5.9 mil (0.15-mm) stencil requires a slightly smaller stencil opening of 15.7 mils (0.40 mm) to ensure that a proper volume of paste is dispensed on each ball land.

Vias connect PCB lands to the middle and opposite surface routing layers of the board. The proper pad diameter and drill size for vias underneath the BGA package typically reflect a compromise between the constraints of the board manufacturing process/cost and the signal routing needs in the area below the footprint of the BGA package. For example a very small via with a very small drill size will require a more costly manufacturing process, while vias that are too large may block some signals from being routed out from underneath the BGA. The sample design in Figure 2-4 uses vias with 16.5 mil pad diameter and 7.5 mil drill size. This geometry allows for one 5-mil signal trace to be routed between adjacent vias under a 0.8-mm pitch BGA package, while allowing for a reasonable mismatch between the drill location and via land placement at maximum drill tolerance offset. This means that due to an imperfect manufacturing process, the drill hole may not always be in the center of the via pad, but it should always be contained within the via pad area (and not be on the edge of the pad).

If the board manufacturing process can resolve 4-mil traces, the via land diameter can be increased to 19 mils and via drill diameter can be increased to 10 mils. The increased minimum via drill diameter will most likely decrease board manufacturing cost. The geometry shown in Figure 2-5 features 4-mil traces, 4.25 mil spaces, 19-mil via lands, and 10-mil via drill holes.

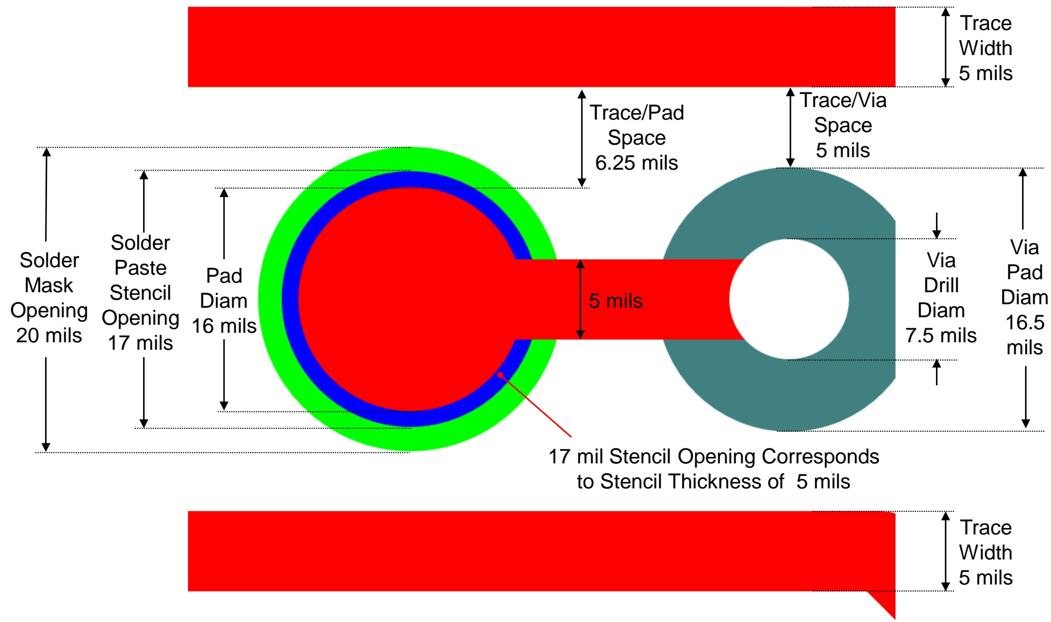

Figure 2-4 PRP Package Footprint Example 1 – 5-mil Trace and 7.5-mil Via Drill Hole

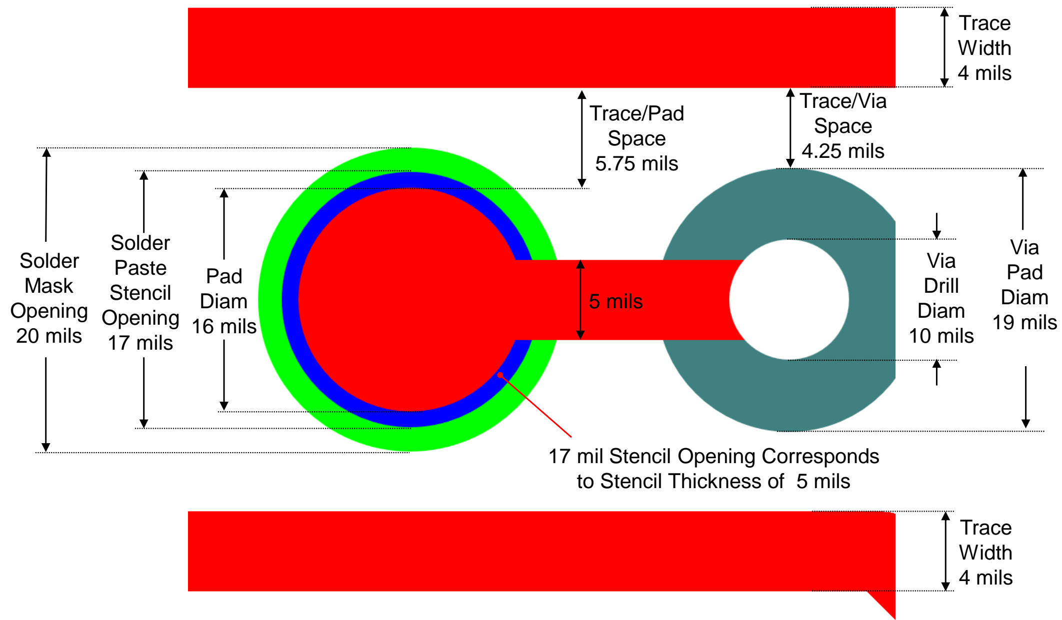

Figure 2-5 PRP Package Footprint Example 2 – 4-mil Trace and 10-mil Via Drill Hole

2.2 Escaping Signals Out From Under 0.8-mm BGA Packages

Many considerations are relevant when routing signals out from under 0.8-mm pitch BGAs. They include via sizes, trace witdth and number of board layers dedicated to routing signals.The signal escape strategies typically try to minimize the number of signal layers neccessery to break out from the BGA footprint, as the number of board layers is directly proportional to the cost of the board. The PRP and ZWT BGA packages used in Concerto and Delfilno device families map signals to BGA balls in such way as to use no more than 2 signal layers to escape from under the BGA footprint. This is accomplished by limiting the placement of signals to be routed within the first 4 outside rows of balls, and by placing power and ground balls toward the middle of the BGA.

Figure 2-6 shows an upper-left corner of a 0.8-mm pitch ball array footprint with 4 rows of signal ball lands forming the outer 4 rows and the power/ground ball lands contained towards the middle of the device. Some of the the 4 outer rows of balls may may be assigned to power or ground, but none of the rows beyond the first 4 rows are assigned to routable signals. Figure 2-6 also shows a channel devoid of balls intended for placement of decoupling capacitor on the back side of the board. Other channels between rows of balls are wide enough to route just a single 4-mil or 5-mil signal trace. This allows for the first two outer rows of signal balls to escape without vias on the top or bottom board layer where the BGA package is soldered, whichever may be the case.The next two rows (3 and 4) must escape using vias to a second signal layer – typically a top or bottom layer opposite to the layer on which the BGA package is mounted.

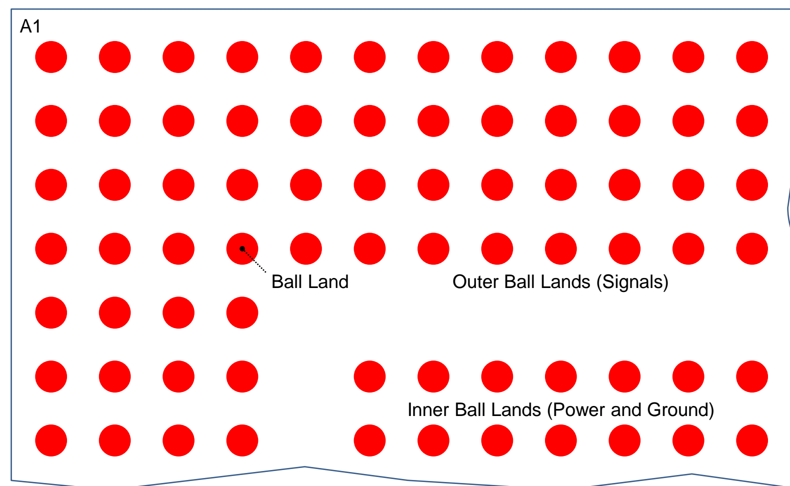

Figure 2-6 Upper-Left Corner of a 0.8-mm BGA Package Footprint

Figure 2-7 shows the signals of the first two rows of balls escaping the BGA footprint on the same top layer that the BGA is mounted on, thus no vias are neccessary. The signals of the first row are routed directly out and away from the BGA, while the second row signals are routed out between the ball lands of the first row of ball lands.

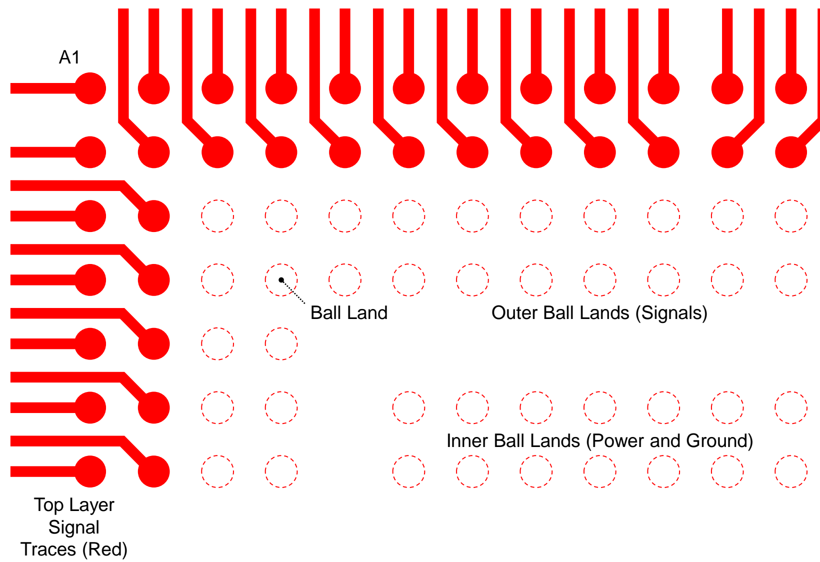

Figure 2-7 Breaking Out of BGA – First 2 Ball Rows Routed on Top Layer

The next two signal rows must use vias to another signal layer in order to escape the BGA footprint. Figure 2-8 shows signals from rows 3 and 4 routed from top to bottom layer through vias placed in the diagonal direction towards the nearest corner of the BGA package. This creates 2 additional channels devoid of vias under the package - one vertical and one horizontal crossing at the center of the BGA footprint.. These channels can be used for placement of additional decoupling capacitors on the bottom of the board.

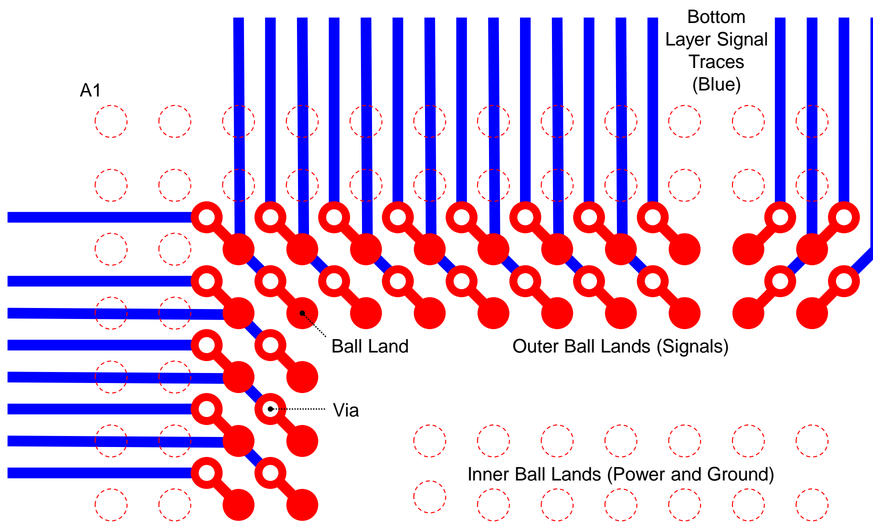

Figure 2-8 Breaking Out of BGA – Ball Rows 3 and 4 Routed on Bottom Layer

Figure 2-9 provides a combined view of all BGA signals emerging from the outside 4 rows of ball lands. The first two rows are routed on the top layer and the second two rows escape to the bottom layer through dedicated vias – one per signal. Vias are also used (not shown here) to connect the ground and power ball lands to corresponding ground and power planes.

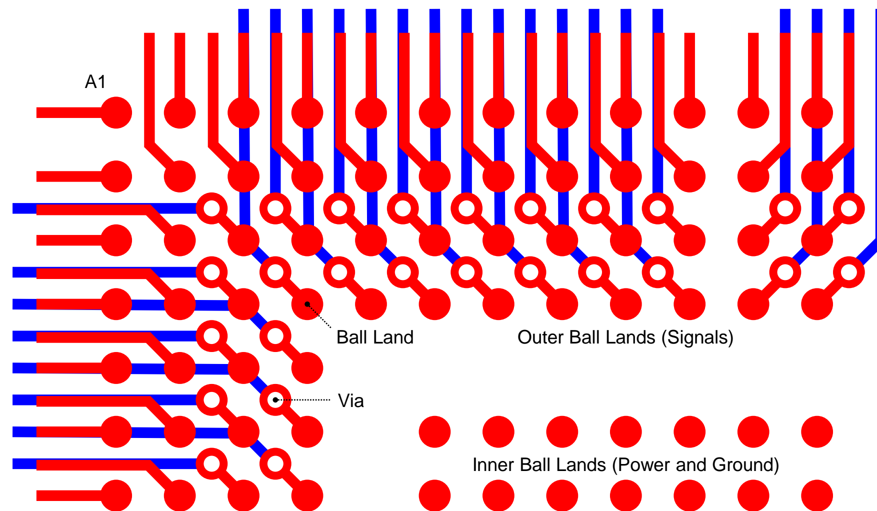

Figure 2-9 Breaking Out of BGA – Top and Bottom Layers Combined

2.3 PowerPAD Thermally Enhanced Packages

Several C2000 processors use PowerPAD thermally enhanced packages to improve thermal performance. PowerPAD packages permit higher clock speeds and more compact designs by efficiently removing heat away from the die. This improved thermal performance is achieved through low thermal resistance between the exposed leadframe pad that the processor die is mounted on, and the corresponding thermal land of the printed-circuit board (PCB). The thermal land has a pattern of thermal vias to channel heat into the ground plane where it is subsequently dissipated into the rest of the board and the surrounding air. PowerPAD packages can be mounted using standard PCB assembly techniques, but in order to leverage the full thermal performance benefits, the exposed leadframe pad must be soldered to a matching thermal pad on the PCB with an array of thermal vias to ground plane. No power plane other than ground should be used because C2000 processors also use exposed PowerPAD leadframe for connection to ground. This frees several pins, which would otherwise be ground pins, for use as digital or analog signals. See Figure 2-10 to visualize how a PowerPAD package is mounted on a PCB. See document SLMA002G for additional information on PowerPAD packages.

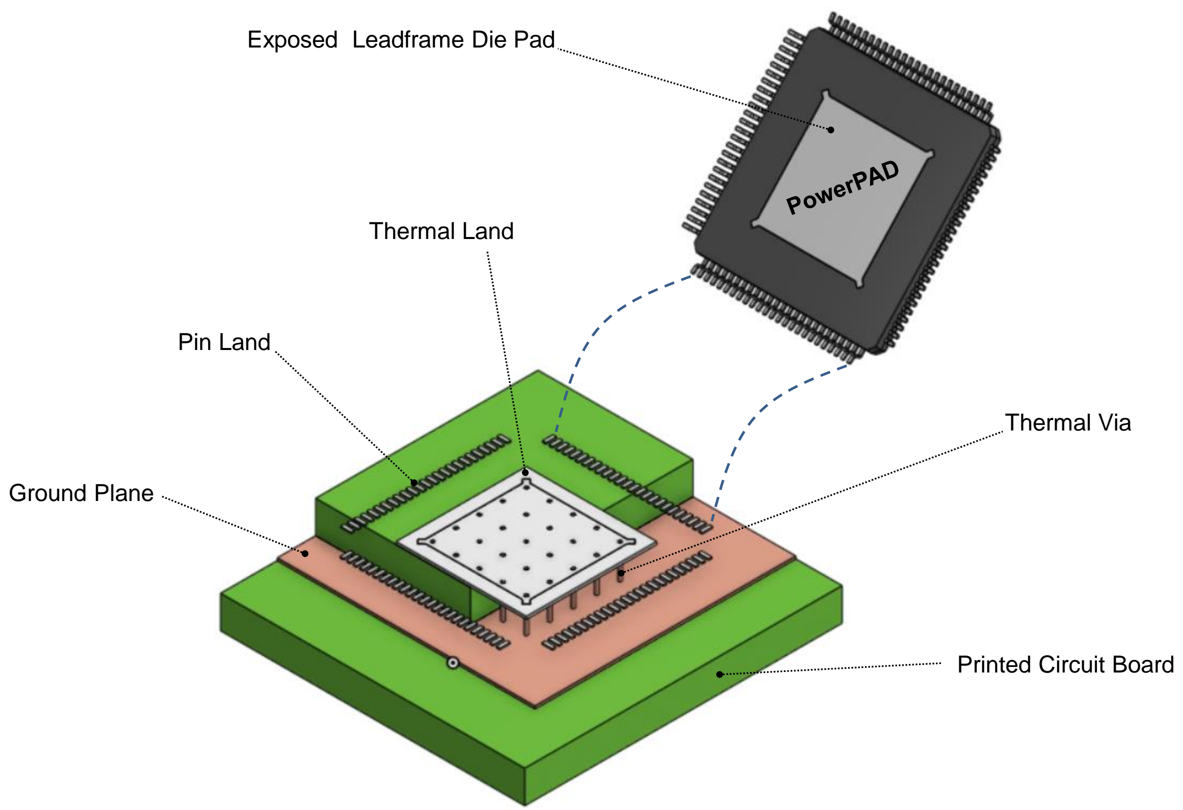

Figure 2-10 PowerPAD Thermally Enhanced Package Mounting

Figure 2-11 shows ideal thermal land sizes and associated thermal via patterns for 3 types of PowerPAD packages used by C2000 processors. The thermal pad in these examples is plated at the surface of the board with 1 oz copper. The 0.3 mm (12 mils) diameter thermal vias, spaced about 2 mm appart, have also been plated with 1 oz copper inside the barrel of each via. Using larger vias may wick too much solder from the themal pad. Using vias that are much smaller reduces the amount of heat that can be removed from the package. The thermal vias used in the thermal land should not use the "wagon wheel" pads with spokes that are typically used for common vias. The thermal vias should use continuous connection around the hole diameter (instead of spokes) to achieve maximum heat removal (see Figure 2-12). Smaller thermal land sizes and fewer vias may also be used and still attain a reasonable thermal transfer characteristics. The actual size of thermal lands and via patterns may be influenced by how much heat the processor is actually generating in a given application, and by how much room is needed to route signal traces underneath the footprint of the package.

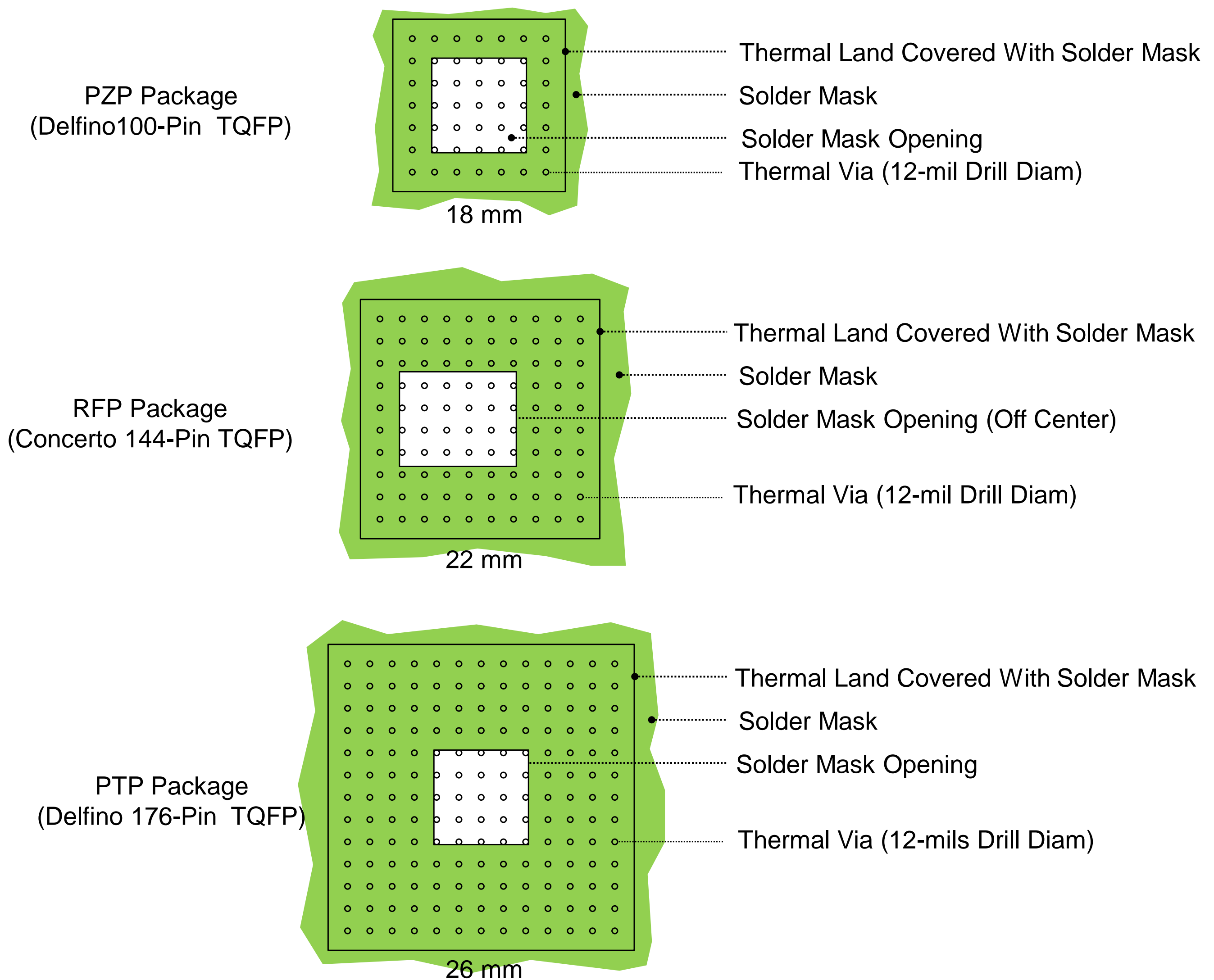

Figure 2-11 Exampes of Thermal Lands, Thermal Via Patterns, Solder Mask Openings

The thermal pad is typically larger than the exposed leadframe die pad to which it is soldered. A larger thermal pad with more thermal vias will dissipate more heat from the package. During assembly, solder paste is dispensed on the exposed portion of the thermal land and pin lands that attach pins of the package to the board. The areas of the board outside where these lands are soldered to the package are covered with green solder mask. Since the thermal pad is typically larger than the exposed leadframe die pad, the solder mask opening for the solder paste that connects the two will typically be smaller than the entire thermal land. This means that the portion of the thermal land not directly below the exposed leadframe die pad will be covered with the green solder mask. Refer to device datasheet for actual dimensions of the exposed leadframe die pad.

When using standard board assembly process some solder voids may occur between the thermal land and the exposed leadframe die pad due to solder wicking into the thermal vias and other causes. But even with these effects in play, a typical standard assembly process achieves greater than 80% solder joint area that is more than satisfactory to preserve low thermal resistance of the PowerPad packages. Therefore it is not necessary to optimize the standard assembly process for thermally enhanced packages such as PowerPad.

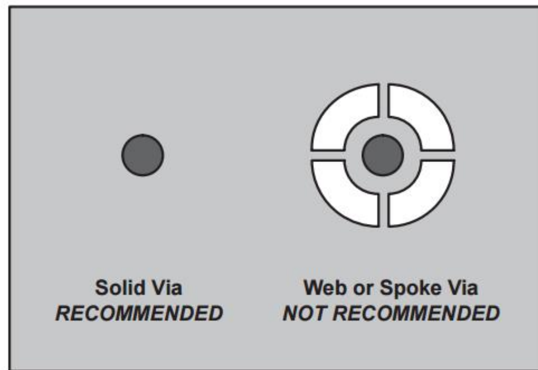

Figure 2-12 Solid vs. Spoked Via

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3 Power and Ground Distribution

3.1 Decoupling Capacitors

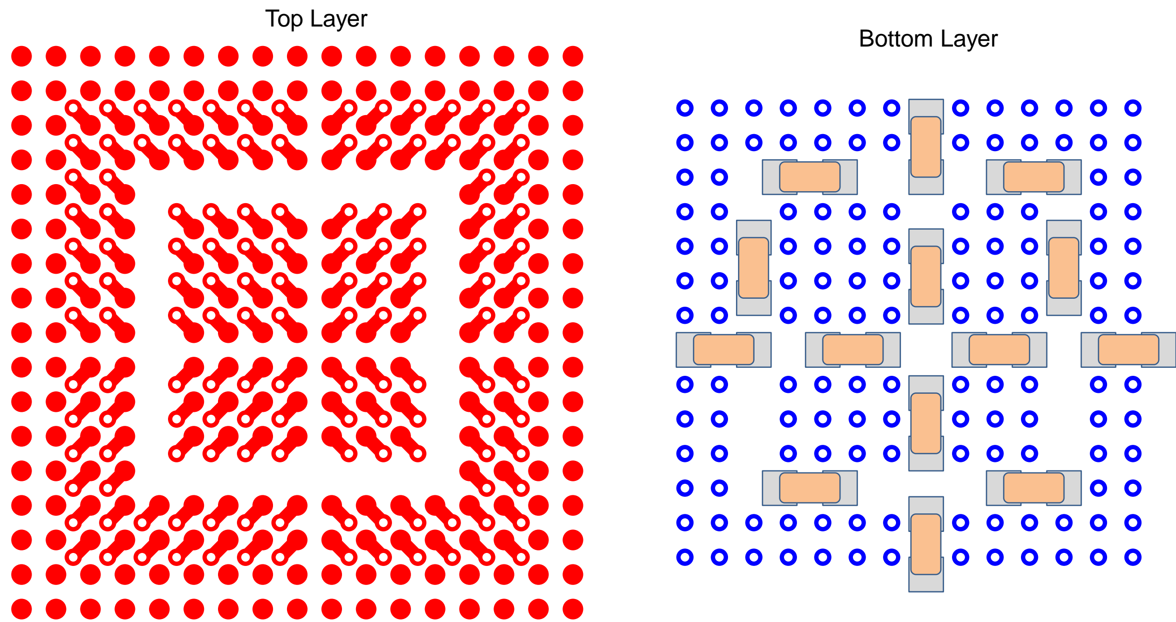

Figure 3-1 PRP Package Footprint Example – Placement of Decoupling Capacitors

Placement of de-coupling capacitors should be such that it minimizes the distance between capacitor components and corresponding power pins. Both the PRP and ZWT packages have “channels” devoid of balls that can be used to place decoupling capacitors closer to power pins. Figure 3-1 shows multiple decoupling capacitors placed under the package footprint on the bottom side of the board in the channels devoid of vias. The remaining capacitors can be placed as close to the package as possible outside of the package footprint.