ADC Timing – Simultaneous Sampling

Latch — 2 Clocks

Sample — 7 Clocks

Convert "A" Channel — 13 Clocks

Write — 2 Clocks

Convert "B" Channel — 6 Clocks — 7 Clocks

Write — 2 Clocks

Generate Early Interrupt "A" Channel

Generate Late Interrupt "A" Channel & Generate Early Interrupt "B" Channel

Start Sampling Next Channel

Generate Late Interrupt "B" Channel
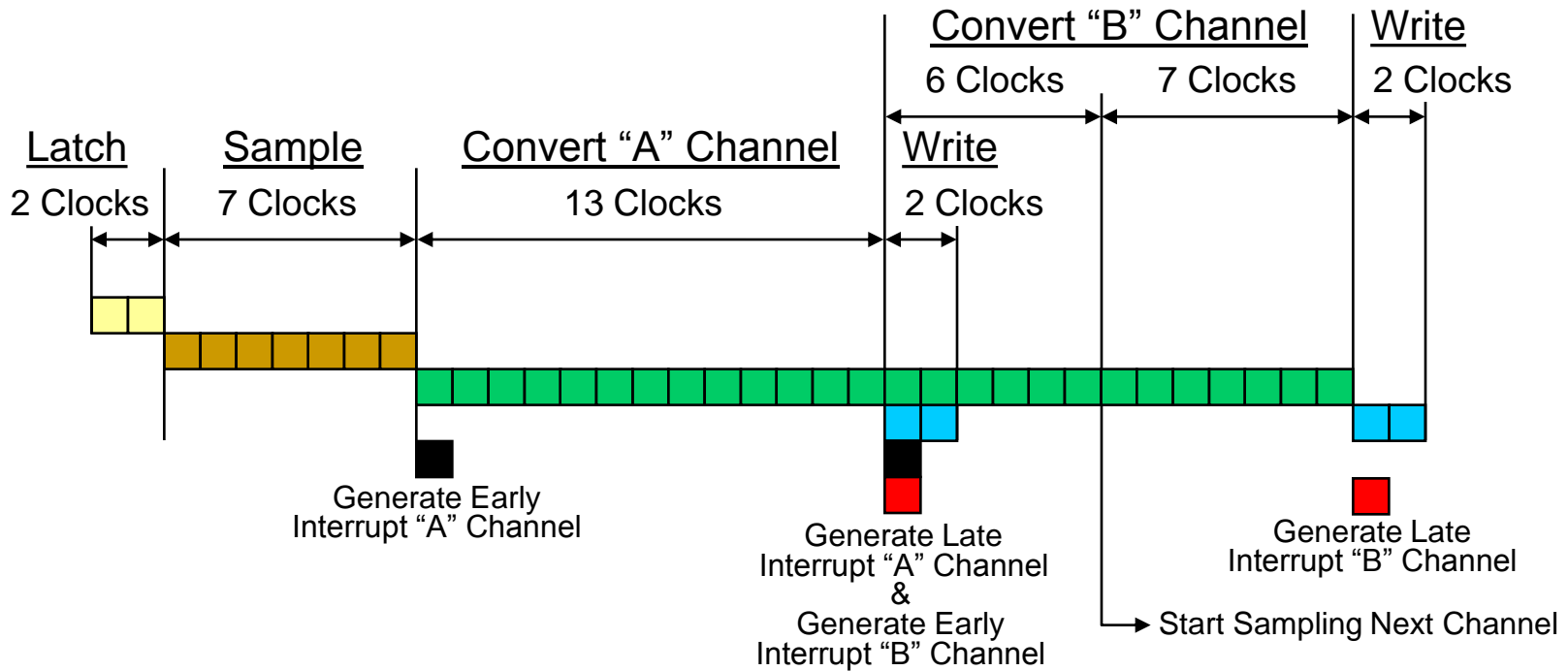
Max Continuous Sampling:

$$\frac{40\ \text{MHz}}{26\ \text{cycles} / 2\ \text{sample}} = 3.08\ \text{MSPS}$$

Note: Sampling window of 7 cycles is minimum and it can be larger