Piccolo F2806x ISO controlCARDs

Texas Instrument's **Piccolo F28069 ISO controlCARD** and **Piccolo F28069M ISO controlCARD** can be used as an evaluation tool and allows the user to experiment with the major control and connectivity features on the F2806x MCU.

The F28069 ISO and F28069M controlCARDs are identical except that the MCU is different between the two cards. The F28069 controlCARD is populated with the TMS320F28069U MCU whereas the F28069M controlCARD is populated with the TMS320F28069M MCU.

1. The controlCARD features: Rev0.4:

- Small size – 90mm x 25mm (3.5" x 1.2")
- DIMM100 compatible cards for C2000 system application boards
- Built in Isolated XDS100 V2 JTAG port for easy interface to Code composer 4.2.x
- Supports USB host/device
- All GPIO, ADC and other key signals routed to gold connector fingers
- Single 5V input supply to the controlCARD and external supply pin decoupling with L+C connected close to the device
- Clamping diode protection at ADC input pins
- Anti-aliasing filter (noise filter) at ADC input pins
- Ground plane
- Isolated RS-232 communication

Note:

1. **See cautionary notes /errata for rev 0.2 BOM and isolation care in section 2.**
2. **Download ControlSUITE from www.ti.com for latest update on software, documentation and examples**

2. Exceptions on Docking station/cCARD set up:

- This controlCARD is designed to be debugged via the on-card emulator. JTAG ports on the docking station or any other baseboard will not be able to connect to the MCU.

- CAUTION: J200 supports USB host/device connectivity. This USB port is not isolated USB port. Care should be taken while connecting external USB devices and this card is used in high power application boards. External USB isolation buffer will be required while debugging high power application boards/systems.

- **Apply caution while using this board in high voltage board testing. Use an external isolator if necessary.**

2.1 Errata/Caution

2.1.1 Rev0.3 & Rev0.4 ISO controlCARDs have an isolated JTAG stage. Earlier control cards had isolated JTAG capabilities but an improper capacitor was placed across the isolation (C276 - .10uf/ 10V).

If using a Rev0.2 or previous design, the existing caps are not recommended for good isolation. Please remove these caps while emulating in high voltage environment (>10V).

All control cards shipping from Nov'11 (R0.3) will have 450V isolation capability.

2.1.2 On the F28069 ISO controlCARD schematic, pin 59 of the F28069 MCU should connect to the net consisting of R3.1, X1.1, and C30.1. Pin 60 should attach to X1.3 and C31.1. This will allow pin 59 (X1) to be grounded via R3 if no external crystal is used.

Each controlCARD includes a "Hardware Developer's Package", a set of "soft collateral" files which makes deploying this technology very easy, these files include:

- Schematics
- Bill of materials (BOM)
- Gerber files

This Hardware Package can be found in C2000's controlSUITE software package:
http://www.ti.com/controlsuite

3. References

Isolated JTAG – ISO JTAG:

J1	USB_A connector is intended for XDS100V2 JTAG emulation and SCI communication through dedicated FTDI logic

Connectivity ports:

J200	USB micro AB connector supports USB 2.0 host/device

LEDs:

LD1	Turns on when controlCARD is powered on (Green)
LD2	Controlled by GPIO-31 (Red)
LD3	Controlled by GPIO-34 (Red)
LD4	Turns on when ISO JTAG logic is powered on (Green)
D2	Uart/SCI/ toggle indicator through Isolated buffer
D3	Uart/SCI/ toggle indicator through Isolated buffer

SW1: Controls the boot options of the F2806x device

Position 1 (GPIO-34)	Position 2 (TDO)	
0	0	Parallel I/O
0	1	Wait mode
1	0	SCI
1	1	(default) Get mode; the default get mode is boot from FLASH

SW2: ADC VREF control

By default, the ADC will convert from 0 to 3.3V. However, if the ADC in the ADC registers is configured to use external limits, the ADC will convert its full range of resolution from VREF-LO to VREF-HI.

Position1 - Controls VREF-HI, the value that the ratio-metric ADC will convert as the maximum 12-bit value, which is 0x0FFF. In the downward position, VREF-HI will be connected to 3.3V. In the upward position, VREF-HI will be connected to pin 66 of the DIMM100-socket. This would allow a connecting board to control the ADC VREF-HI value. This extends VREF-HI connections to both the ADCs on the F2806x device.

Position 2 - Controls VREF-LO, the value that the ratio-metric ADC will convert as the minimum 12-bit value, which is 0x0000. In the downward position, VREF-LO will be connected to 0V. In the upward position, VREF-LO will be connected to pin 16 of the DIMM100-socket. This would allow a connecting board to control the ADC-VREFLO value. This extends VREF-LO connections to both the ADCs on the F2806x device.

SW3: TRST/ ISO SCI communication signal enables

Position 1 -

ON - TRST signal from ISO JTAG circuit (USB connector J1) will be connected to F2806x. This configuration is necessary when using JTAG to debug the device and connect to Code Composer Studio.

OFF - TRST signal from ISO JTAG circuit will NOT be connected to F2806x. This configuration is necessary when the application is running from flash at power up without debug capability.

Position 2 -

ON - The default option. SW3 in the “ON” position enables a UART COM link between the MCU and USB connector J1. This is accomplished using the FT2232’s USB-to-Serial port bridge and GPIO28 of the F28069 MCU.

OFF - Disables the serial link between the MCU and USB connector J1. This allows GPIO28 to be used as desired by the baseboard that the controlCARD is plugged in to.