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TI Designs
DC Power-Line Communication Reference Design

TEXAS INSTRUMENTS

TI Designs

TI Designs are analog solutions created by TI's analog experts. Reference Designs offer the theory, part selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of useful circuits. Circuit modifications that help to meet alternate design goals are also discussed.

Design Resources

24VDCPLCEVM	Tool Folder Containing Design Files
AFE031	Product Folder
TMS320F28035	Product Folder
LM34910	Product Folder
TPS62170	Product Folder
TPD1E10B06	Product Folder
TMDXEVM3358	Tool Folder

Design Features

- Robust protection against power-up surges with two-stage AC-coupling design with TVS protection
- Power design implements low-pass filtering to filter PLC communication from switching regulator operation
- Hardware and software supports multiple nodes
- DC-input voltage 18-V to 35-V operation
- Long cable support, (40-m) cable passed with no bit errors even at the lowest Transmitter Power Level
- Configurable hardware that supports different PLC standards
- Complete PHY, MAC, and application layer

Featured Applications

- Industrial control
- Lighting applications
- Smoke and fire detection systems and many more building automation applications

TI E2E™ Community

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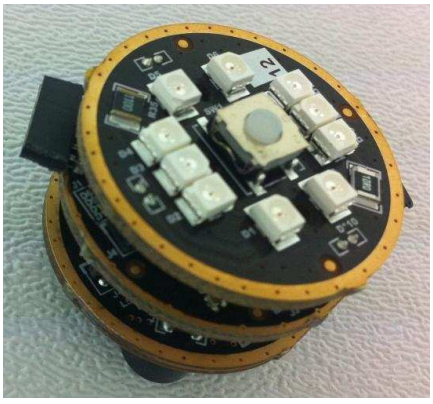

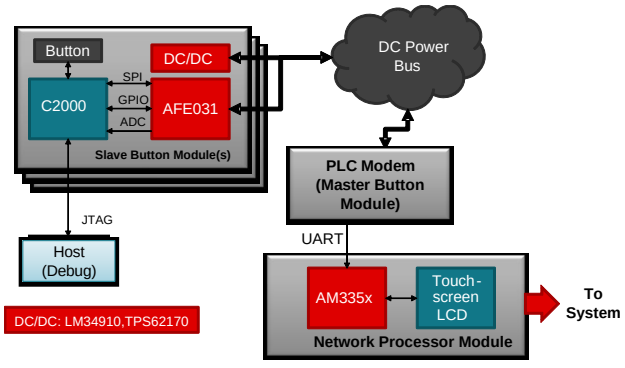

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1 System Description

The DC (24 V, nominal) Power-Line Communication (PLC) reference design is intended as an evaluation module for users to develop end-products for industrial applications leveraging the capability to deliver both power and communications over the same DC-power line. The reference design provides a complete design guide for the hardware and firmware design of a master (PLC) node, slave (PLC) node in an extremely small (approximately 1-inch diameter) industrial form factor. The design files include schematics, BOMs, layer plots, Altium files, Gerber Files, a complete software package with the application layer, and an easy-to-use Graphical User Interface (GUI).

The application layer handles the addressing of the slave (PLC) nodes as well as the communication from the host processor (PC or Sitara™ ARM® MPU from Texas Instruments, see Figure 1). The host processor communicates only to the master (PLC) node through a USB-UART interface. The master node then communicates to the slave nodes through PLC. The easy-to-use GUI (see Figure 7) is also included in the EVM that runs on the host processor and provides address management as well as slave-node status monitoring and control by the user.

The reference design has been optimized from each slave (PLC)-node source-impedance perspective such that multiple slaves can be connected to the master (see Section 9.1). Protection circuitry has also been added to the analog front-end (AFE) so that it can be reliably AC coupled to the 24-V line (see Section 9.4). Also note that this reference design layout has been optimized to meet the PLC-power requirements. See Section 13.1 for the AFE031 layout requirements for high-current traces.

At the heart of this reference design are the AFE from TI, AFE031 (see Figure 2), to interface with power lines and the TMS320F28035 Piccolo™ Microcontroller (see Figure 3) that runs the PLC-Lite protocol from TI (see Section 5).

1.1 AFE031

The AFE031 device is a low-cost, integrated, power-line communication (PLC) AFE device that is capable of capacitive-coupled or transformer-coupled connections to the power line while under the control of a DSP or microcontroller. The AFE031 device is also ideal for driving low-impedance lines that require up to 1.5 A into reactive loads. The integrated receiver is able to detect signals down to 20 µVRMS and is capable of a wide range of gain options to adapt to varying input signal conditions. This monolithic integrated circuit provides high reliability in demanding power-line communications applications. The AFE031 transmit power-amplifier operates from a single supply in the range of 7 V to 24 V. At a maximum output current, a wide output swing provides a 12-VPP (I_{OUT} = 1.5 A) capability with a nominal 15-V supply.

The analog and digital signal-processing circuitry operates from a single 3.3-V power supply. The AFE031 device is internally protected against overtemperature and short-circuit conditions. The AFE031 device also provides an adjustable current limit. An interrupt output is provided that indicates both current limit and thermal limit. There is also a shutdown pin that can be used to quickly put the device into its lowest power state. Through the four-wire serial-peripheral interface, or SPI™, each functional block can be enabled or disabled to optimize power dissipation. The AFE031 device is housed in a thermally-enhanced, surface-mount PowerPAD™ package (QFN-48). Operation is specified over the extended industrial junction temperature range of –40°C to +125°C.

1.2 C2000

The F2803x Piccolo family of microcontrollers (C2000™) provides the power of the C28x core and control-law accelerator (CLA) coupled with highly integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code, as well as providing a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed full scale range and supports ratiometric VREFHI and VREFLO references. The ADC interface has been optimized for low overhead and latency.

Based on TI's powerful C2000-microcontroller architecture and the AFE031 device, developers can select the correct blend of processing capacity and peripherals to either add power-line communication to an existing design or implement a complete application with PLC communications.

2 PLC-Over-DC Design Features

- DC-input voltage 18-V to 35-V operation
- Uses DC-power line and GND for both power and communication to multiple nodes
  - Eliminates need for additional serial-communication wiring
  - Significantly reduces copper-wire installation
- Complete PHY, MAC, and application layer handles node addressing and communications
  - Reduces design time and increases system-installation speed
- Configurable hardware supports different PLC standards
  - PLC-Lite, G3 and PRIME

3 Block Diagram

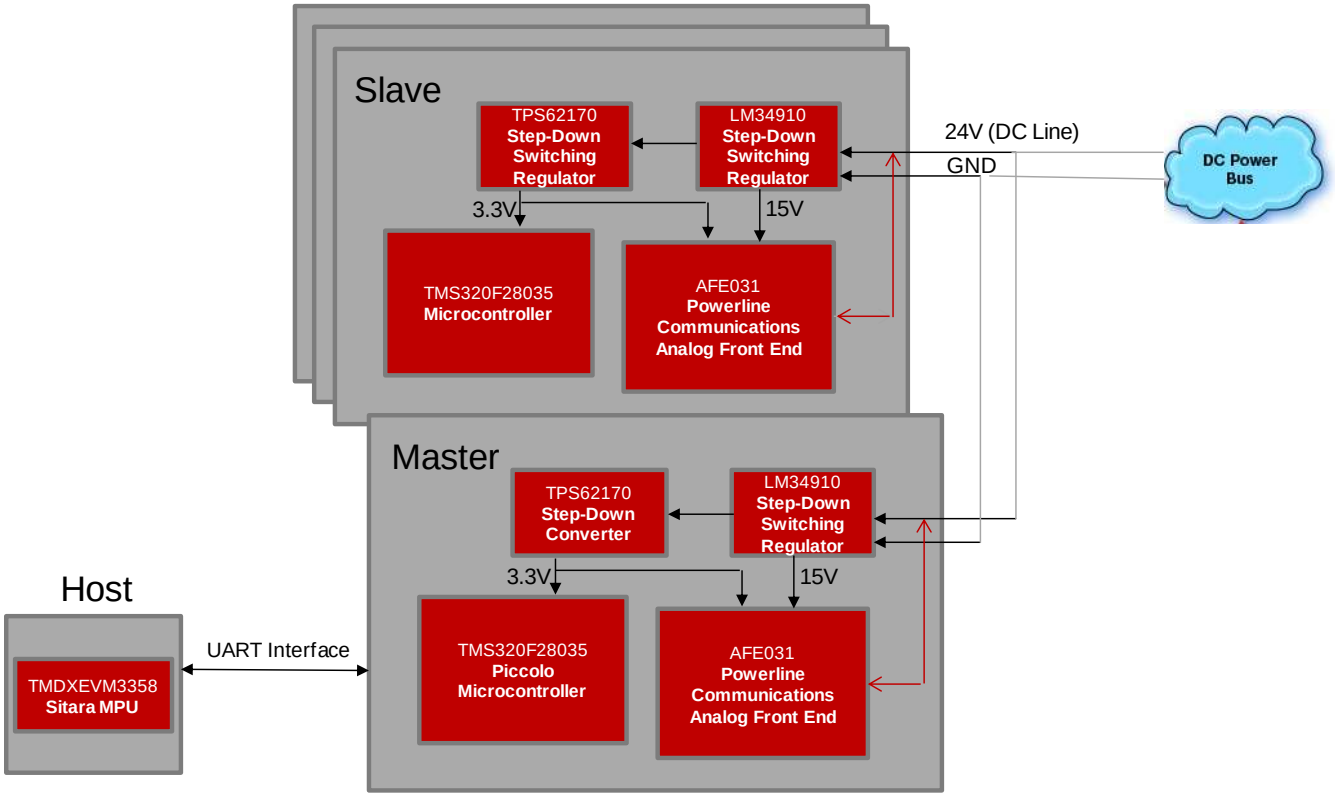


Figure 1. PLC Over DC Solution System Block Diagram

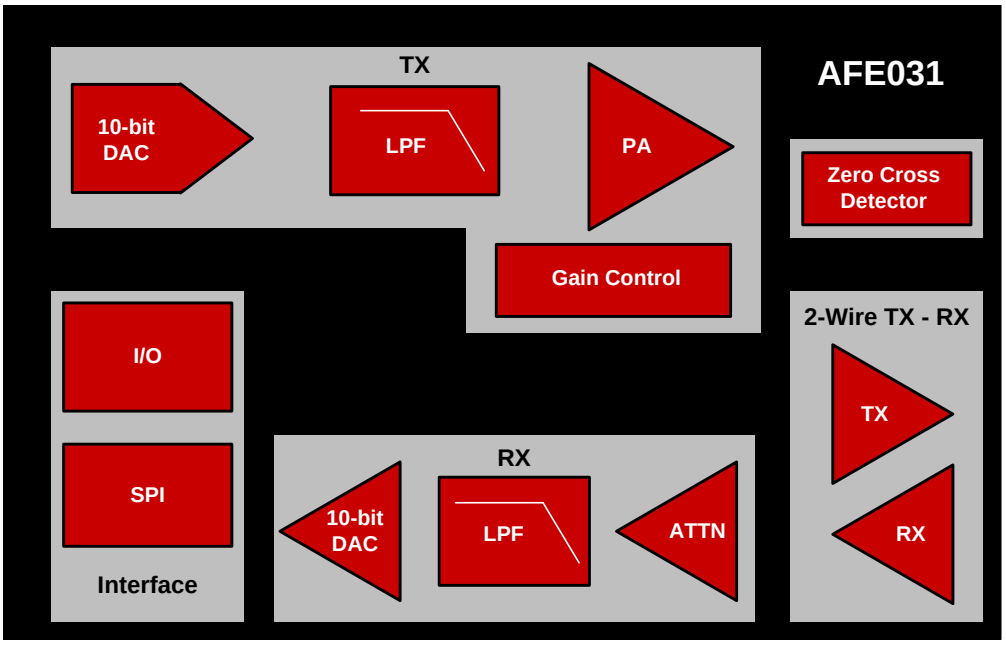


Figure 2. AFE031 Block Diagram

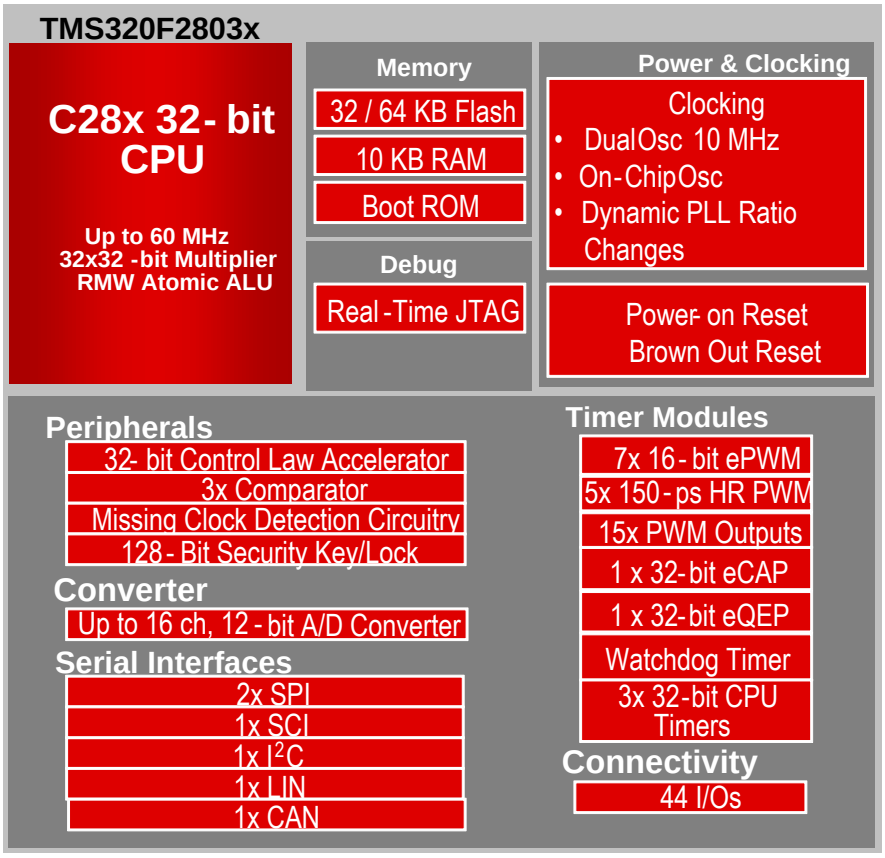


Figure 3. TMS320F2803x Block Diagram

4 Highlighted Products

The DC-PLC Reference Design features the following devices:

- AFE031
  - Power-line communications analog front-end (AFE)
- TMS320F2803x
  - Piccolo family of microcontrollers
- LM34910
  - High-voltage 40-V 1.25-A step-down switching regulator
- TPS62170
  - 3 to 17-V 0.5-A step-down converter with DCS-control in 2 × 2 QFN package

For more information on each of these devices, see the respective product folders at www.TI.com.

4.1 AFE031

- Integrated power-line driver with thermal and overcurrent protection
- Conforms to EN50065-1
- PRIME certified
- Large output swing: 12 Vpp to 1.5 A (15-V supply)
- Low Power Consumption: 15 mW (receive mode)
- Programmable TX and RX Filters
- Supports EN50065 CENELEC bands A, B, C, D
- Supports FSK, S-FSK, and OFDM
- Supports PRIME, G3, IEC 61334
- Receive sensitivity: 20 µVRMS, typical
- Programmable TX and RX gain control
- Four-wire serial peripheral interface
- Two integrated zero crossing detectors
- Two-wire transceiver buffer
- 48-pin QFN PowerPAD package
- Extended junction temperature range: –40°C to 125°C

4.2 TMS320F28035 (Piccolo Microcontroller)

- High-efficiency 32-Bit CPU (TMS320C28x™)
- 60-MHz device (16.67-ns cycle time)
- Single 3.3-V supply
- Integrated power-on and brown-out resets
- Two internal zero-pin oscillators
- Up to 45 multiplexed GPIO pins
- Three 32-bit CPU timers
- On-chip flash, SARAM, OTP memory; boot ROM available
- Code-security module
- Serial port peripherals input
  - One SCI (UART) module
  - Two SPI modules
  - One inter-integrated-circuit (I2C) bus
  - One local-interconnect-network (LIN) bus

  - One enhanced-controller area-network (eCAN) bus
- Enhanced control peripherals
  - Enhanced pulse width modulator (ePWM)
  - High-resolution PWM (HRPWM)
  - Enhanced capture (eCAP)
  - High-resolution input capture (HRCAP)
  - Enhanced quadrature encoder pulse (eQEP)
  - Analog-to-digital converter (ADC)
  - On-Chip temperature sensor
  - Comparator
- 16 × 16 and 32 x 32 MAC operations
- 16 × 16 dual MAC
- Harvard bus architecture
- Atomic operations
- Fast interrupt response and processing
- Unified memory programming model
- Code-efficient (in C/C++ and assembly)
- Programmable control-law accelerator (CLA)
  - 32-bit floating-point math accelerator
  - Executes code independently of the main CPU
- Endianness: Little Endian
- No power sequencing requirement
- Low power
- No analog support pins
- Low device and system cost
- Watchdog timer module
- Dynamic PLL-ratio changes supported
- On-chip crystal oscillator and external clock input
- Missing clock detection circuitry
- Up to 45 individually programmable multiplexed GPIO pins with input filtering
- Independent 16-bit timer in each ePWM module
- 128-bit security lock and key
  - Protects secure memory blocks
  - Prevents firmware reverse engineering
- Advanced emulation features
  - Analysis and breakpoint functions
  - Real-time debug through hardware
- 56-Pin, 64-Pin, and 80-Pin packages
- 2803x packages
  - 56-Pin RSH very-small quad flatpack (no lead) (VQFN)
  - 64-Pin PAG thin-quad flatpack (TQFP)
  - 80-Pin PN low-profile quad flatpack (LQFP)

4.3 LM34910

- Integrated 40-V N-channel buck switch
- Integrated start-up regulator
- Input voltage range: 8 V to 36 V
- No loop compensation required
- Ultra-fast transient response
- Operating frequency remains constant with load current and input voltage
- Maximum duty cycle limited during startup
- Adjustable output voltage
- Valley current limit at 1.25 A
- Precision internal reference
- Low bias current
- Highly efficient operation
- Thermal shutdown

4.4 TPS62170

- DCS-Control™ topology
- Input voltage range: 3 V to 17 V
- Up to 500 mA Output current
- Adjustable output voltage from 0.9 V to 6 V
- Fixed output voltage versions
- Seamless power-save mode transition
- Typically 17-µA quiescent current
- power good output
- 100% duty-cycle mode
- Short-circuit protection
- Overtemperature protection
- Available in a 2 × 2 mm, WSON-8 package

5 PLC-Lite™ Standard

The reference design firmware and software support the PLC-Lite standard by default. TI offers PLC-Lite, as a non-standard-based, low-cost, and very flexible approach to PLC. Because PLC-Lite is not a fixed standard, developers can exploit the flexibility of PLC-Lite to optimize an implementation to specific channel characteristics. This optimal implementation improves link robustness in environments where G3 and PRIME experience difficulty because of interference on the line which requires exceptional handling.

Standard	Technology	Band Occupied	Data Rate Range	Target TI Processor
G1	SFSK	60– 76 KHz	1.2– 2.4 kbps	F28027
PRIME	OFDM	42– 90 kHz	21– 128 kbps	F28069
ERDF G3	OFDM	35– 90 kHz	5.6– 45 kbps (6–72 kbps)*	F28069
P1901.2/ G3 FCC	OFDM	35–450 kHz	34– 234 Kbps (37–580 kbps)*	F28M35x
PLCLite (TI Proprietary)	OFDM	42– 90 kHz	2.4–21 kbps	F28035/ F28027

*Without overhead.

Figure 4. PLC-PHY Standards Compliance

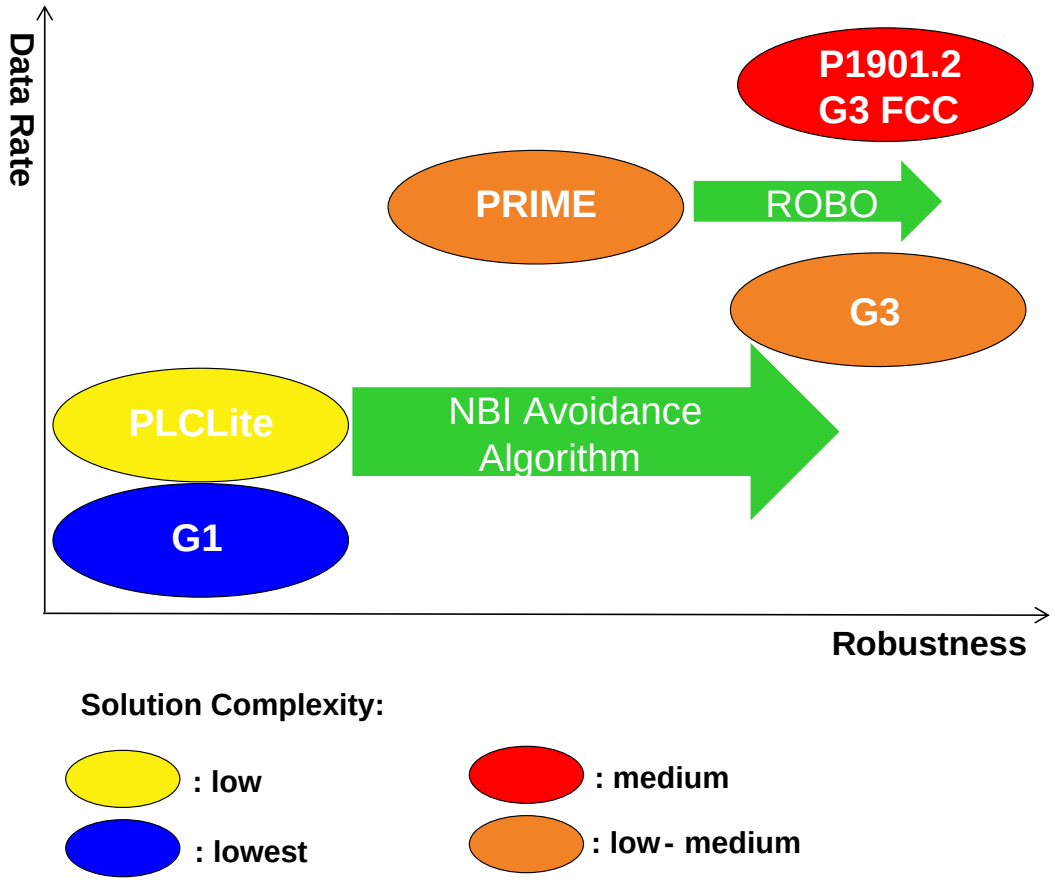


Figure 5. TI's PLC Solutions

PLC-Lite offers a maximum data rate of 21 Kbps and supports both full-band and half-band modes. PLC-Lite has been designed to provide added robustness to certain types of interference, including narrowband interference that can affect G3 links.

NOTE: PLC-Lite contains a simple Carrier Sense Multiple Access and Collision Avoidance (CSMA/CA) media access control (MAC) layer which can integrate with any application-specific stack.

Because of the simplicity and lower data rate of PLC-Lite, it can be implemented at a substantially lower cost per link. PLC-Lite also offers tremendous flexibility and allows developers to customize channel links outside the constraints of an industry standard.

Band	A/B/C/D half band, configurable at run-time CENELEC compliant	CENELEC A full band
Bandwidth	23 kHz	47 kHz
Sampling frequency	500 kHz	250 kHz
Data/Header symbol duration	2.24 ms	2.24 ms
Preamble duration (each)	2.048 ms	2.048 ms
PHY data rate	21 kbps (BPSK) 11 kbps (BPSK + FEC) 2.6 kbps (Robo-4) 1.3 kbps (Robo-8)	42 kbps (BPSK) 21 kbps (BPSK+FEC) 5.2 kbps (Robo-4) 2.6 kbps (Robo-8)
FFT size	1024	512
CP size	96	48
Number of subcarriers	49	97
MAC	CSMA/CA	CSMA/CA

Figure 6. TI's PLC-Lite Feature Parameters

PLC-Lite is appropriate for very cost-sensitive environments and applications where the complexities of G3 and PRIME are not required while still requiring a robust communications channel. In the same way that a television remote does not require the full capabilities of Wi-Fi® to change channels and adjust the volume, not every application needs the advanced functions and data rate of PRIME and G3. For example, PLC-Lite is the perfect solution for a simple light bulb or wall switch within a home network where only a few kilobits per second is sufficient.

6 PLC-Lite Based Application Layer Overview

6.1 Application Layer Built on PLC-Lite

The application layer in this reference design is based on existing PLC-Lite firmware from TI (see Figure 29).

- Uses standard C2000 and AFE031 support libraries
- Uses TI's PLC-Lite protocol for PLC communication
- PLC-Lite provides robust PHY and MAC layers for establishing communication
- Network discovery and addressing extensions examples developed for this reference design
- UART communication layer through the *master* button
- Simple protocol for re-transmitting PLC packets over UART

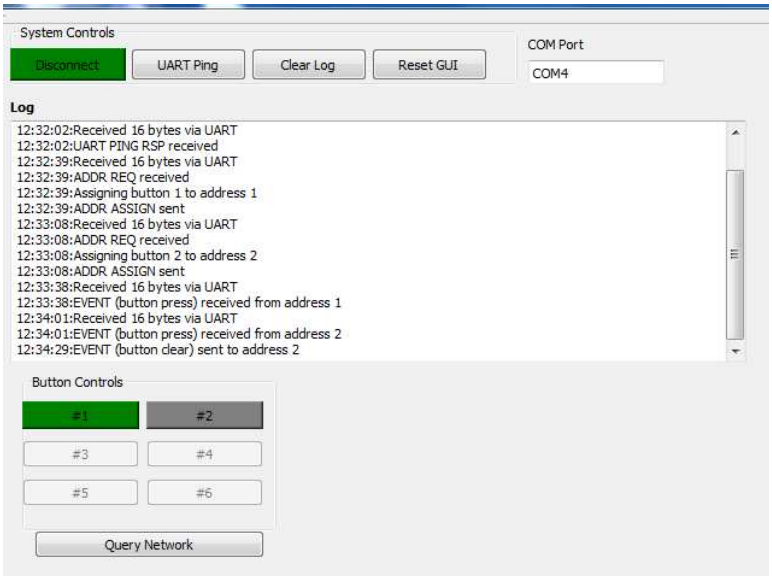


Figure 7. Graphical User Interface

- AM335x EVM-based GUI (using Qt Embedded) developed for a simple-button and LED-indicator control-panel application
- The GUI also works on Windows®-based host PCs with Qt SDK

6.1.1 Address Assignment Protocol

- Uses PLC-Lite MAC layer addressing filtering
- This reference-design software uses 16-bit addresses (see Figure 32)
- Unicast and broadcast messages only
  - Master can send either of those messages
  - Buttons can send only unicast messages to master.
- Master has a default address 0x0000
- Broadcast message use address 0xFFFF
- Unassigned buttons have an arbitrary starting address from remaining address space
  - Unassigned buttons ignore address assignment messages unless they have sent a previous request to avoid collisions during assignment

6.1.2 Message Types

Master-to-slave (see Figure 8 and Figure 9)

- Addressed
  - Address assign
  - Event (such as: clear a button)
  - Event response
- Boradcast
  - Query network
    - Receives the status of all buttons (PLC nodes) on the network

Slave-to-master (see Figure 8 and Figure 9)

- Address request
- Event (such as: press a button)
- Event response

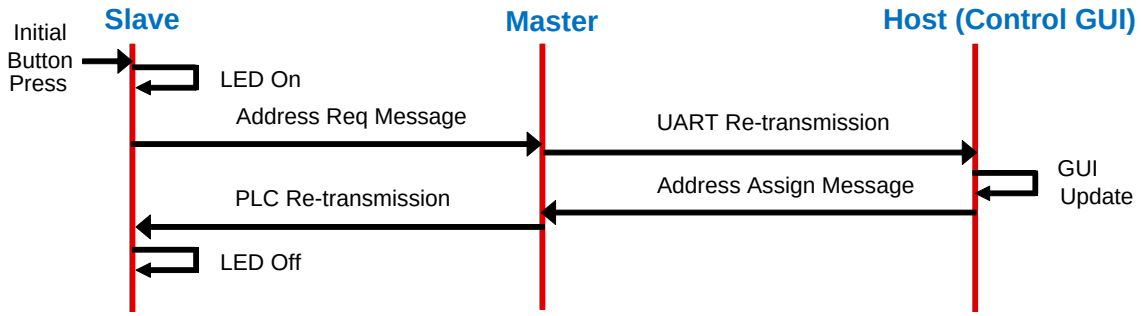


Figure 8. Message Flow Example: Address Assignment

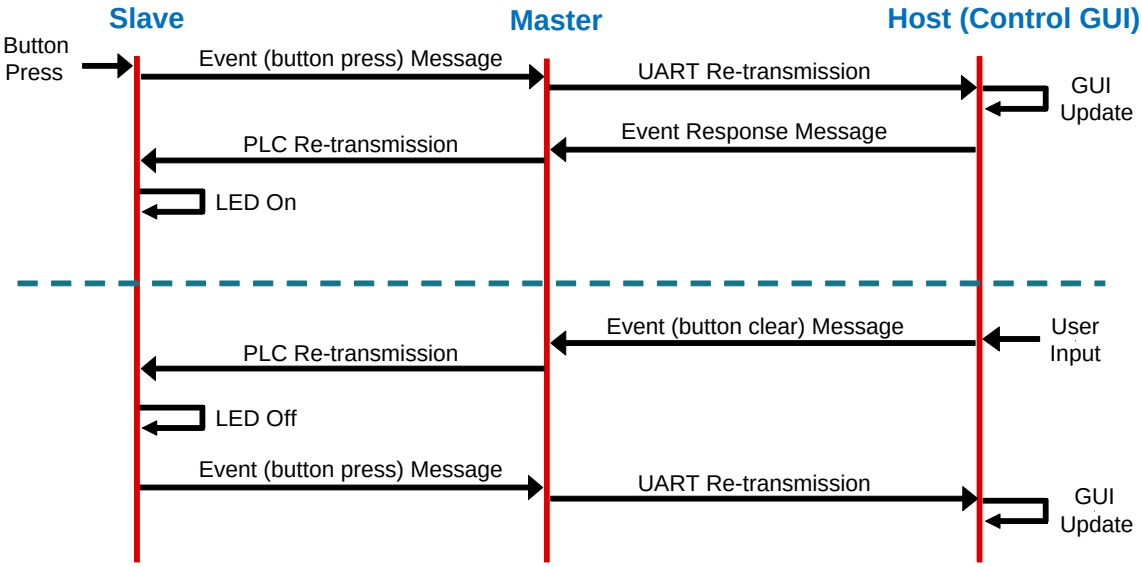


Figure 9. Message Flow Example: Button Press and Clear

7 PLC Node Identification

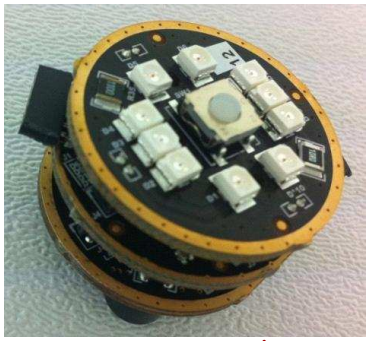
In this reference design software each PLC node is identified by three parameters:

1. Address
   - Assigned by the controller (or is arbitrary at power-up)
2. Token
   - Provided by the controller during address assignment
   - Used to identify a button function (for example: this is button number 4 in the GUI)
3. Current State
   - Determined by a combination of address state and button or LED state:
     - Unassigned Address
     - Waiting for Address
     - Inactive (address assigned with LED OFF)
     - Inactive and Waiting (button pressed, waiting for response from master)
     - Active (address assigned with LED ON)

All parameters are sent back to the master during a network query or a broadcast message.

8 Getting Started

8.1 Hardware



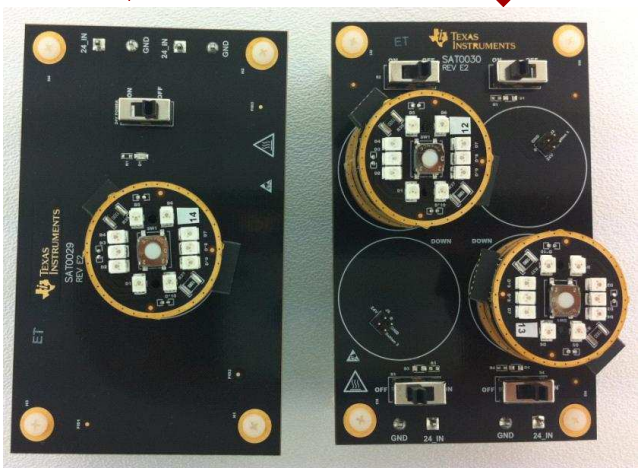
SAT21 (bottom)
- 24-V input
- Generate 15 V and 3.3 V

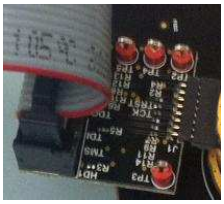
SAT22 (middle)
- PLC Modem – C2000 + AFE031

SAT23 (top)
- Application board – LEDS + switch

SAT29 – master board
- Mount one PLC node

SAT30 – slave board
- Mount 1-4 PLC nodes
- Possible to daisy-chain





Other PCBs

SAT24–JTAG (to C2000) interface board

SAT45–UART (to C2000) interface board

Figure 10. Hardware

The reference platform comprises of seven different pieces of hardware as listed:

1. SAT0021 — Power board for the PLC node. This board has the switching regulators that take in the DC voltage (18 V to 36 V) and covert the DC voltage to 15 V and 3.3 V.
2. SAT0022 — Processor and AFE board. This board contains the C2000 (TMS320F2803x) and the AFE031.
3. SAT0023 — Application board. This board contains the LEDs and a push button.

NOTE: A PLC node comprises of SAT0021, SAT0022, SAT0023 connected through board-to-board connectors.

4. SAT0029 — Base board. The master PLC-node can be mounted on this board
5. SAT0030 — Base board. The slave PLC-node can be mounted on this board
6. SAT0024 — Connectivity interface board. This board connects to the SAT0022 for JTAG programming of both master and slave PLC-nodes.
7. SAT0045 — Connectivity interface board USB–UART. This board connects to the SAT0022 (master node) and is used by the host processor to communicate to the master PLC-node.

NOTE: The maser and slave PLC-nodes are the same hardware. The nature of firmware that is loaded to the C2000 determines the different functionality of the nodes as either master or slave.

8.1.1 Hardware Setup

To set up the reference-design hardware, follow the steps listed in this section.

Step 1: Connect a Power Supply

A power supply that can source up to 25 V and approximately 2 A is required. The supply is set to 24 V as shown in Figure 11.

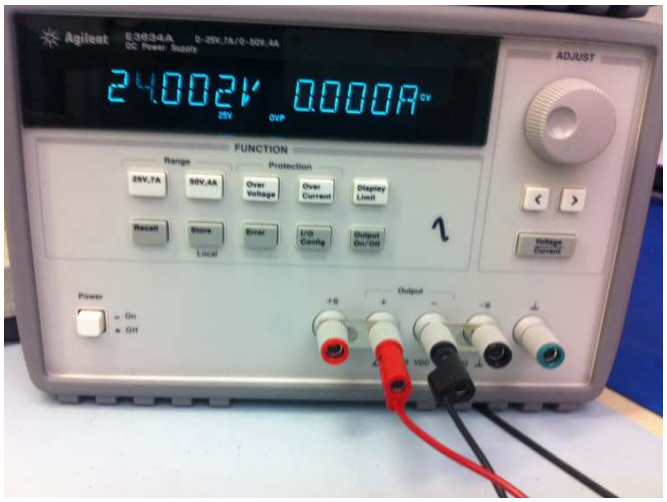


Figure 11. 24-V Power Supply

Step 2: Connect the Inductor

Connect an inductor in-series with the 24-V supply input. The inductor size must be large enough that the inductor provides enough impedance to the power-line-communication signal, such that the power supply, which can have a very low impedance, does not interfere with the PLC-signal modulation. For this design setup, the 5900-271-RC from Digi-Key is used which is a 270-µH inductor (for product detail see the Digi-Key website, http://www.digikey.com/product-detail/en/5900-271-RC/5900-271-RC-ND). This inductor provides approximately 75-Ω impedance to the PLC signal and therefore ensures that the power supply does not provide a low-impedance path for the usable PLC-modulation signal.

NOTE: Always ensure to use the inductor in-series (such as the 5900-271-RC) with the lab power supply to power this DC-PLC reference design as shown in Figure 12.

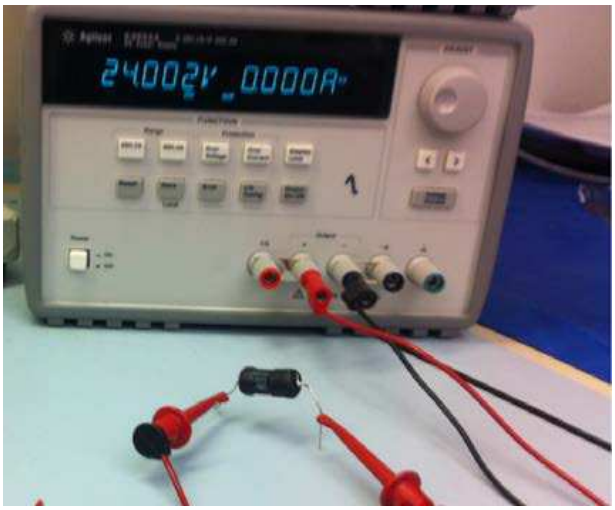


Figure 12. 5900-271-RC –270-µH inductor

Step 3: Install the PLC Node

Install the PLC node into the master and slave base boards. There is a 4-pin connectors on the PLC node (see Figure 13 and Figure 53 for the SAT0021 schematic) and a complimentary 4-pin male connector on the SAT0029 (master-node base board, see Figure 14) and SAT0030 (slave-node base board, see Figure 15).

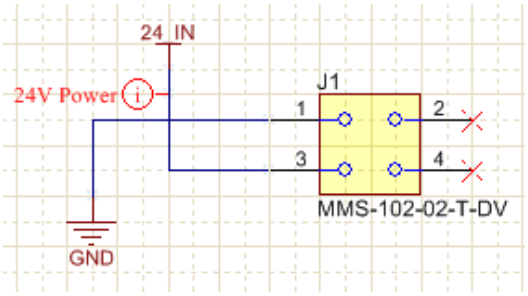


Figure 13. 4-Pin Connector on the SAT0021 That Feeds Power to the PLC Node

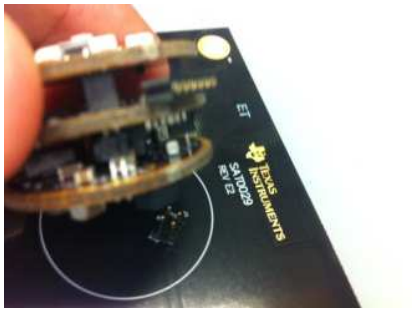


Figure 14. Master Panel

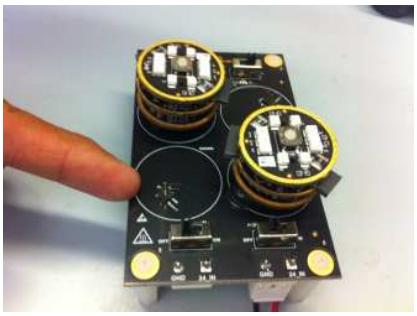


Figure 15. Slave Panel

Step 4: Connect Slaves and Master

Both of the base boards for mounting the master and slave nodes have an individual ON switch and OFF switch to individually control the power to a given node (see Figure 16 and Figure 17). Each board also has two power connectors so that multiple boards can be daisy-chained together allowing for additional slaves.

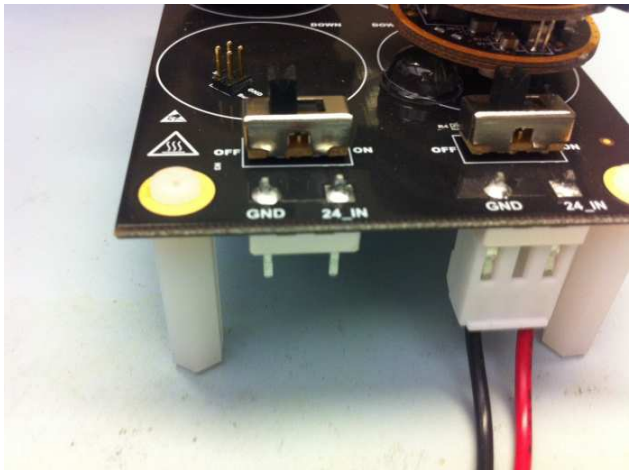


Figure 16.

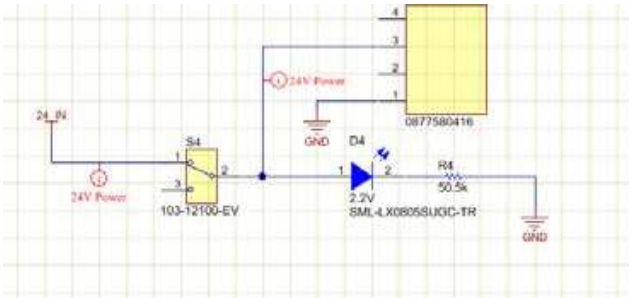


Figure 17.

Turn on the ON switch for the connected master and slaves. At this step in the setup the power consumed by two slaves and one master is approximately 75 mA from the 24-V supply.

NOTE: On power-up the LEDs on the slaves pulse, as the slaves do not have an assigned address.

Step 5: Connect USB-UART

As shown in Figure 18, connect the USB-UART (see Figure 60 for the SAT0045 schematic) to the 6-pin connector of the master node (see Figure 54 for the SAT0022 schematic). Note that the slaves are connected to the master only through a power line.

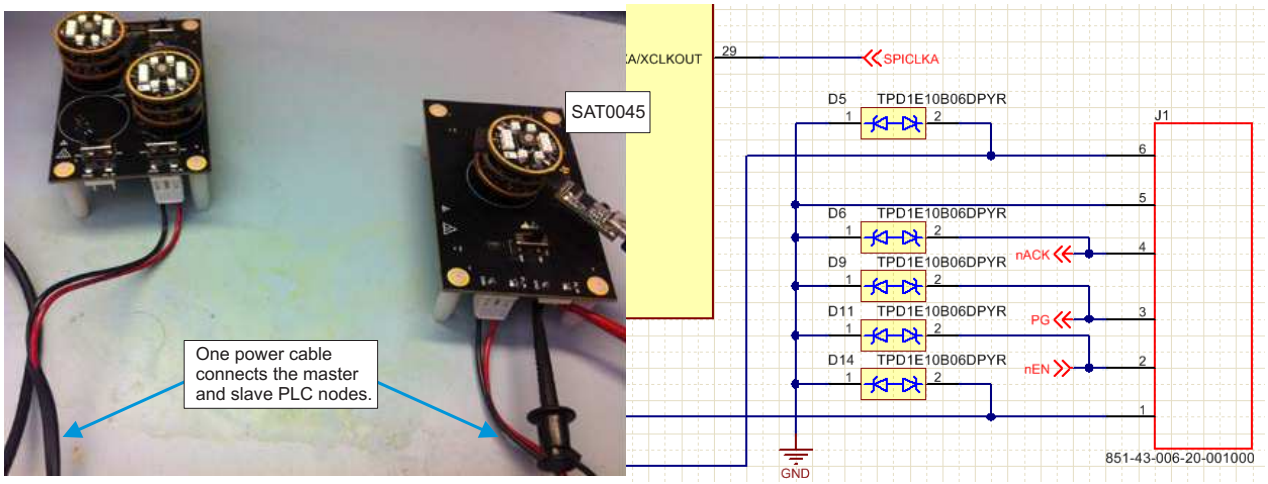


Figure 18. Single Power Supply

At this step in the setup, open the software GUI (see Section 8.3).

When the USB-UART board is connected to the host, the USB-UART board is identified as a COM Port in the GUI. Ensure that the correct COM-Port number appears in the *COM Port* field (see Figure 19).

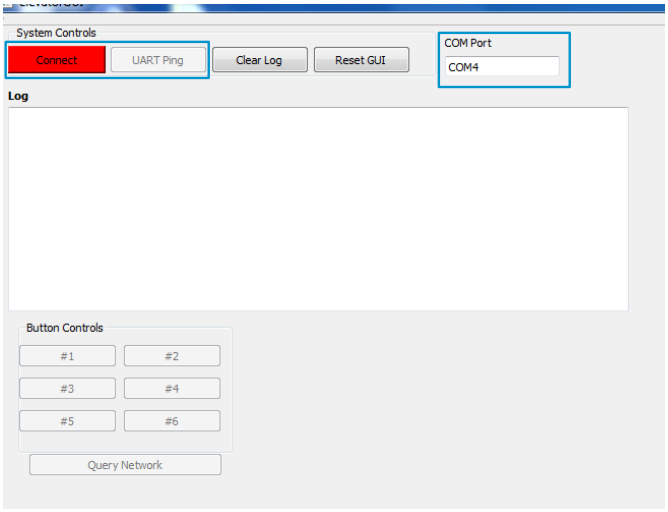


Figure 19.

Once the correct COM-Port number appears in the field, click *Connect* and then click *UART Ping* as shown in Figure 19.

If the master board is connected and the correct COM Port is selected in the GUI, a message is displayed which verifies successful communication to the master (see Figure 20). Also note that the buttons under *Button Controls* are grayed out as there are no slave nodes on the network during this step.

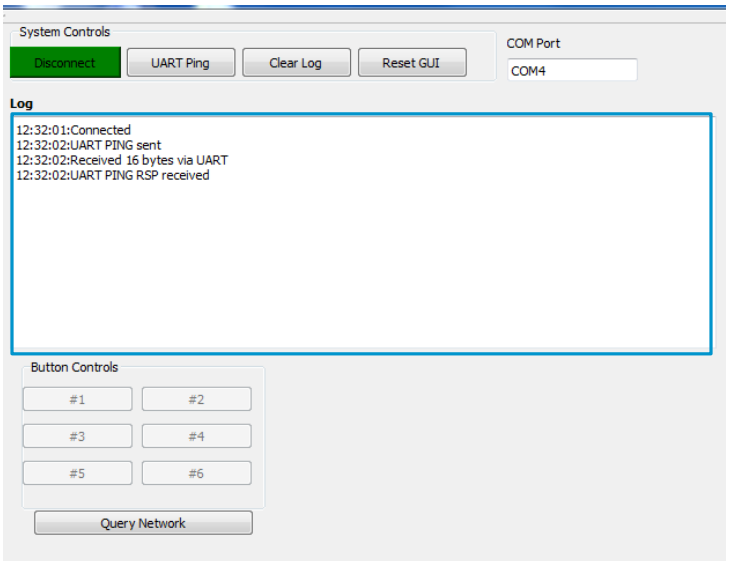
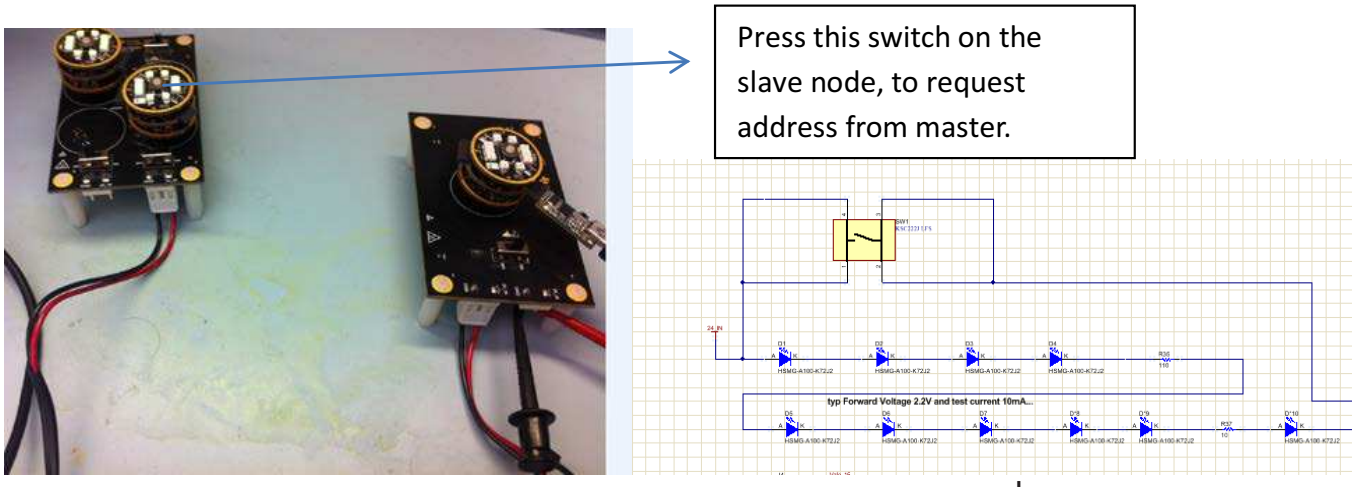


Figure 20.

Step 6: Address Assignment to Slave Node

As previously noted, the slave-node LEDs pulse after power-up because no address has been assigned to the slave nodes. If the switch on the slave node is pressed, the slave node communicates to the master node over the power line (see *a.* and *b.* in Figure 21). The master communicates to the host through the UART and the host assigns the network address to the slave.

NOTE: When the slave node is assigned the address, the slave-node LEDs stop pulsing.



a. b.

Figure 21.

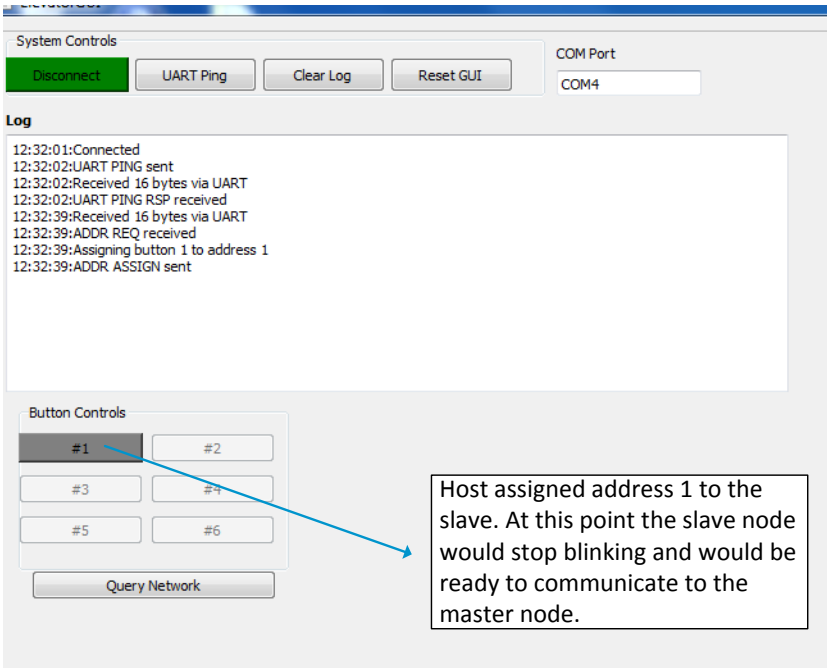


Figure 22.

Similarly, if the switch on another slave node is pressed, the same process repeats and the host assigns an address to the other slave PLC-node (see Figure 23).

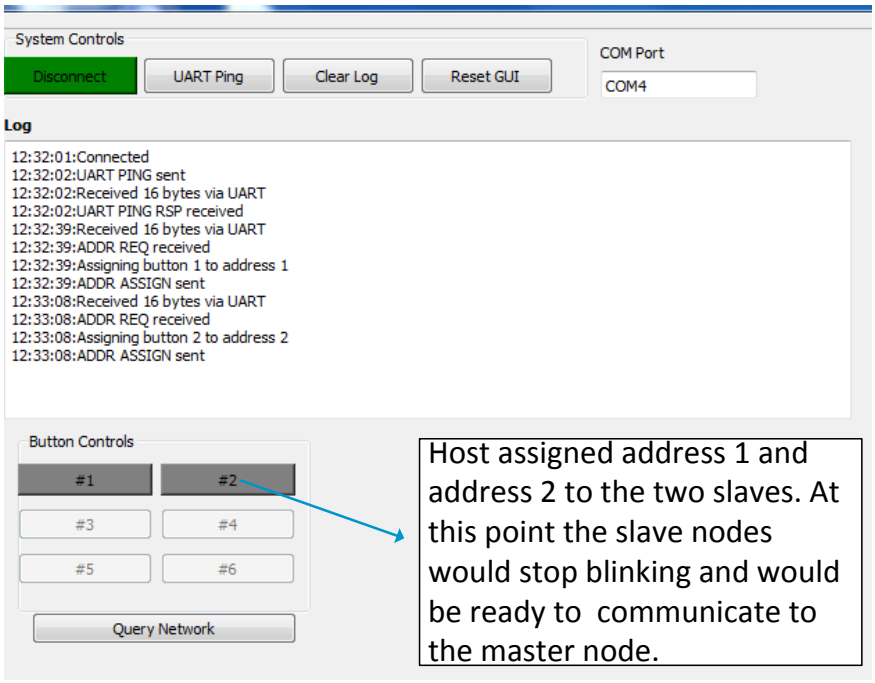


Figure 23.

Step 7: PLC Communication

If the switch on the slave node is pressed after the slave node has an assigned address, then the slave communicates through PLC to the master that the button has been pressed. The master then communicates this status to the host through UART that a *button-press* event on the slave with address 1 has occurred (see Section 7). This status is reflected in the GUI as shown in Figure 24. The host then sends the message to the master node through UART to light up the LED of the slave with address 1. The master communicates this message to the slave node through PLC.

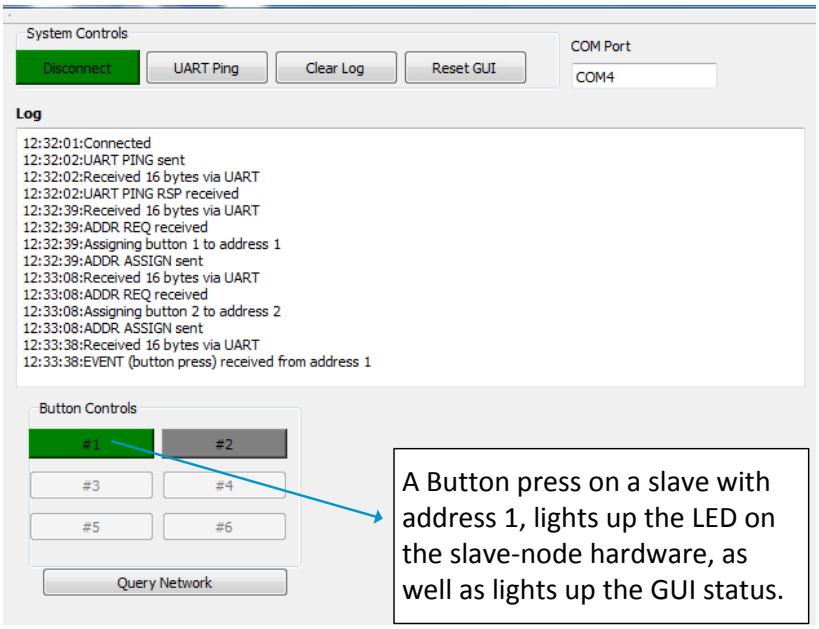


Figure 24.

Similarly, on button press of the slave node with address 2, the same process is repeated (see Figure 25).

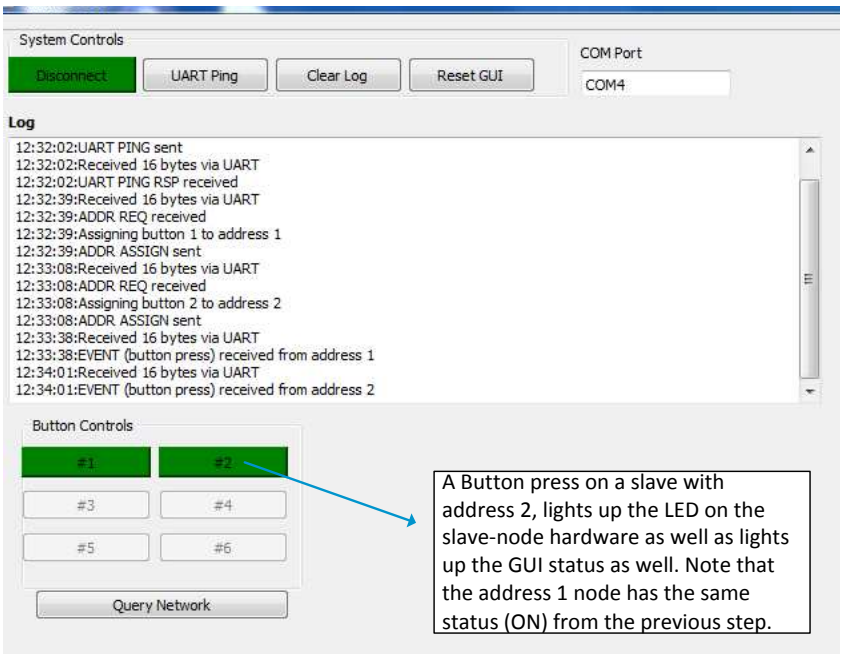


Figure 25.

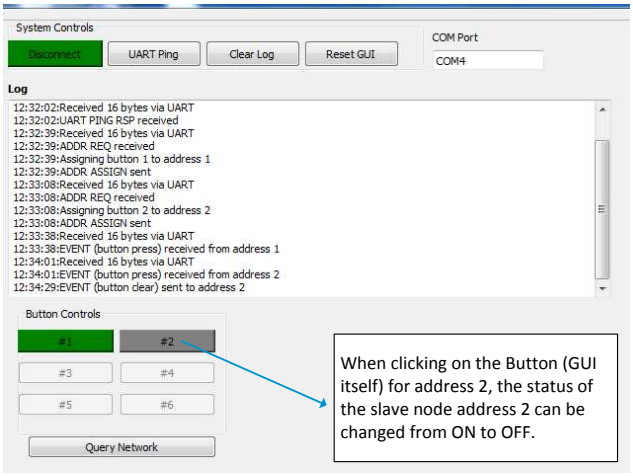


Figure 26.

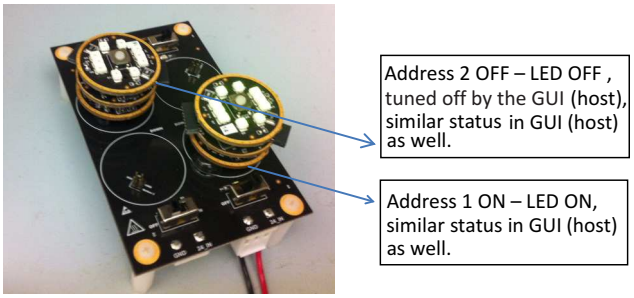


Figure 27.

Step 8: Activate the Broadcast Feature

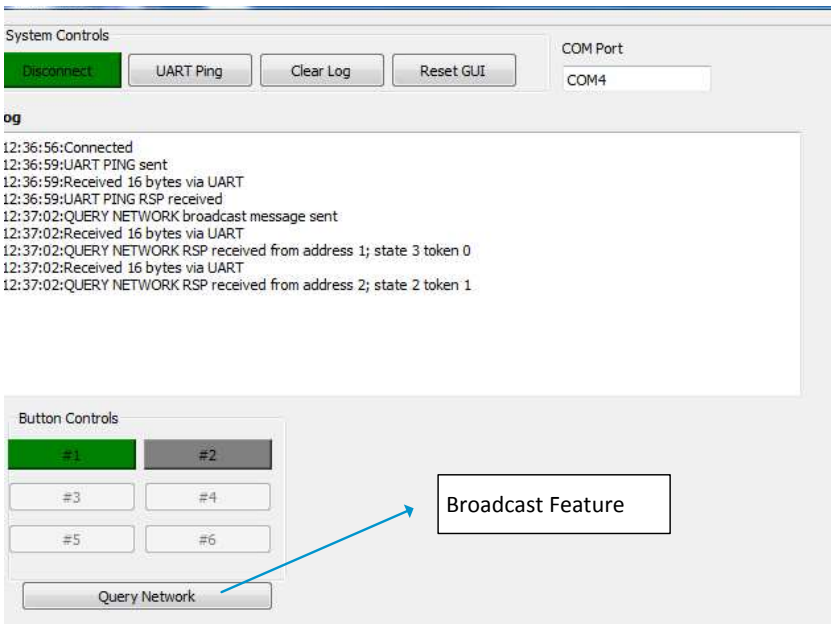


Figure 28.

Another feature implemented in this reference design, is the ability to query the network. As shown in Figure 28, by clicking on the *Query Network* button, the host receives the status of each slave. A message appears in the GUI listing each slave, the address, and status.

8.2 C2000 Firmware

This reference design and the accompanying software demonstrate an example application of this system as a button and LED-indicator control panel. The button and LED control panel is implemented by any number of button modules which communicate their status back to the network processor module. The network processor module displays the status in an example GUI.

The PLC-Lite components that are necessary for the demo are included in the demonstration software described in this section. However, for the complete PLC-Lite Software Development Kit (SDK) including detailed documentation, please download the PLC-Lite SDK from www.ti.com/plc.

8.2.1 Demonstration Software Archive

All firmware and software necessary to run the demonstration system is included a single-archive file, TIDC188.zip. The first step in exploring the demonstration software is to extract this archive to a directory on the user's computer. In the remainder of these instructions, the directory location of the extracted files is referred to as DEMO_DIR. The following sections list the detailed instructions for building and running both the C2000 firmware and GUI application. Table 1 lists the details of the key directories in the archive.

Table 1. Key Archive Directories

DIRECTORY	DESCRIPTION
`firmware/dsp_c28x`	Top-level directory for C2000 firmware
`firmware/dsp_c28x/lib`	Contains libraries and headers for general C2000 device support
`firmware/dsp_c28x/plc_lite`	Contains libraries, headers and application code for PLC-Lite demonstration
`firmware/dsp_c28x/plc_lite/inc` `firmware/dsp_c28x/plc_lite/lib`	Include files and object code libraries for PLC-Lite network stack
`firmware/dsp_c28x/plc_lite/src/common`	Common source files for both master and slave C2000 firmware
`firmware/dsp_c28x/plc_lite/src/master`	Source files for master node C2000 firmware. Also contains CCS project files for the dc_plc_master project
`firmware/dsp_c28x/plc_lite/src/slave`	Source files for slave node C2000 firmware. Also contains CCS project files for the dc_plc_slave project
`gui/dc_plc_gui`	Qt based GUI application code
`gui/qextserialport-1.2rc`	Qt serial port library code

The C2000 firmware for this demonstration system uses TI's PLC-Lite network stack which includes PHY and MAC layers (see SPRCAC9). There are two separate firmware binaries: one for the modem attached the network processor (denoted the master) and one for each button (denoted the slave firmware). Figure 29 shows the various components in the C2000 firmware. The following lists the component details.

- Existing C2000 firmware libraries:

  PHY— PLC-Lite PHY layer

  MAC— PLC-Lite MAC layer

  UART— UART driver

  CSL— C2000 chip-support library

  HAL— AFE031 hardware abstraction library
- Source code for the demonstration system:

  Source Code for Demonstration System—A simple protocol designed for addressing assignment and control of the individual buttons

  Host Communication— Library for host communication over UART

  Application— Other application-level logic (for example: button-state machine)

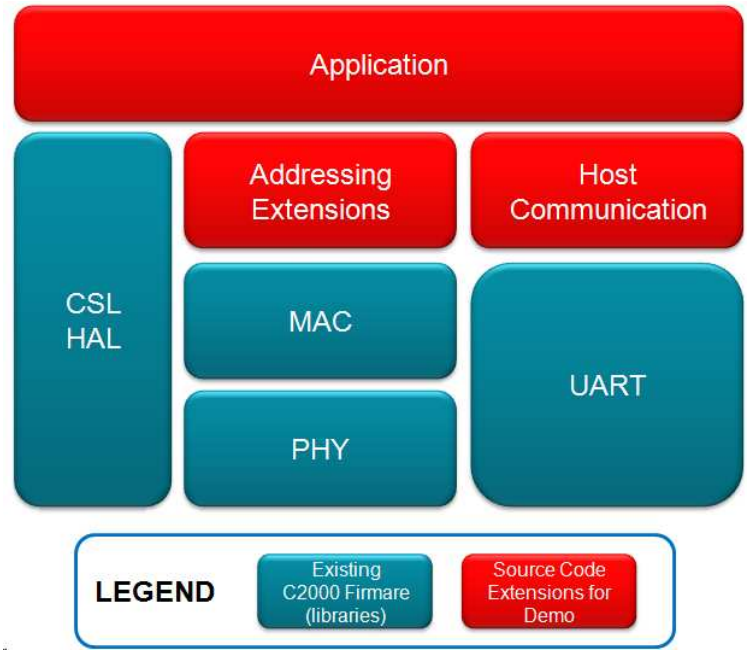


Figure 29. C2000 Firmware Layers

8.2.2 Installing and Building the C2000 Firmware

Installing and building the C2000 firmware requires Code Composer Studio™ 5.x with C2000 device support installed on the computer of the user. This guide assumes general familiarity of the user with Code Composer Studio (CCS) and with the tasks of building and running applications on C2000 devices.

When the demonstration software archive has already been extracted to the DEMO_DIR directory, use the following instructions to import, build, and run the firmware.

8.2.2.1 Importing the Firmware Projects

1. Open CCS and select *File → Import*.
2. select *Code Composer Studio → Existing CCS Eclipse Projects*, then click *Next*.
3. Select *Browse* and choose the demonstration archive directory, DEMO_DIR
4. Check the boxes for both the dc_plc_master and dc_plc_slave projects
5. Deselect the check box for *Copy Projects into Workspace*

NOTE: The projects depend on relative path variables for locating the library and included files therefore not copying these files onto your workspace directory is critical.

6. Click *Finish* when the dialog box is set as shown in Figure 30.

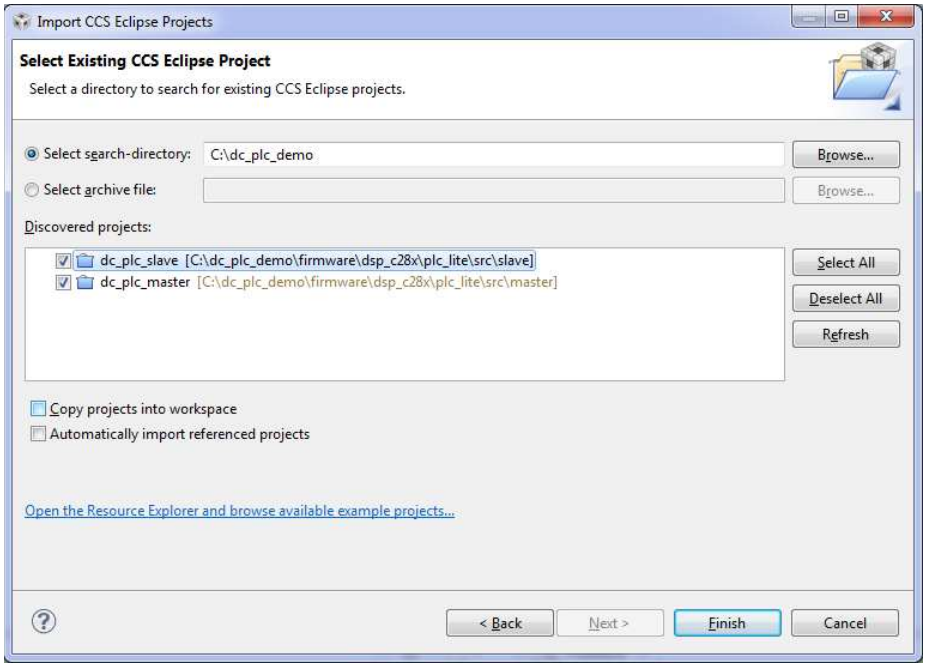


Figure 30. CCS Eclipse Project Import

8.2.3 Building the Firmware

To build either project (dc_plc_slave or DC_plc_master), right click on the project name and select *Build Project*. Alternatively, select the desired project and click on the build icon ( ) in the CCS toolbar .

The projects include both Debug and Release configurations, but for demonstration purposes only use the Debug configuration.

8.2.4 Running the Firmware

Programming and debugging the firmware requires the demonstration hardware and an XDS100 JTAG Emulator (see the tool folder for more information, http://www.ti.com/tool/xds100.

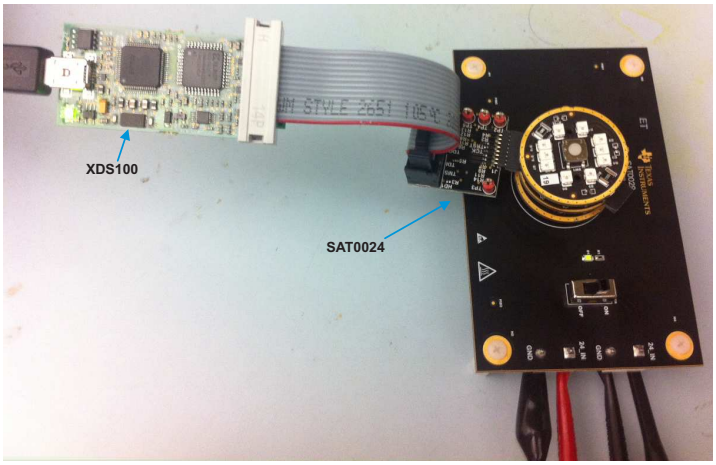


Figure 31. XDS100 Connected to SAT0024

With the XDS100 is connected to the target demonstration device (see Figure 31), select either project and click the debug icon ( ) in the CCS toolbar.

8.2.5 Common Firmware Details

The firmware projects collect common code into a number of files which are referenced by each individual project, but are stored in the single directory, firmware/dsp_c28x/plc_lite/src/common. Table 2 lists the source file details.

Table 2. Source-File Details

FILES	DESCRIPTION
F28035_init.c	Contains general F28035 initialization function.
dc_plc_common.h dc_plc_common.c	Header and source file for demonstration application code which is common to both master and slave devices. Includes global variables, interrupt service routines and common initialization function.
host_comm.h host_comm.c	Header and source file for host communication (UART) functions. Technically only used by master device firmware but included in common code for future extensions and re-use.
address_protocol.h firmware_protcol.c	Header and source file implementing the addressing and control event protocol used by the demonstration.

8.2.6 Master Firmware Details

The specific firmware for the master device is located in the firmware/dsp_c28x/plc_lite/src/master directory. This directory includes the CCS project files, compilation outputs, and the dc_plc_master.c source file which implements the main function of the master firmware and application-level code.

The master firmware is a very simple-state machine with a few background tasks. The main function executes a single loop which continually performs the following steps:

1. Execute host communication and PLC-Lite MAC-layer tasks
2. Check if a UART message was received, and, if so, forward this message to the PLC interface
3. Check if a PLC message was received, and, if so, forward this message to the UART interface

8.2.7 Slave Firmware Details

The specific firmware for the slave device is located in the firmware/dsp_c28x/plc_lite/src/slave directory. This directory includes the CCS project files, compilation outputs, and the dc_plc_slave.c source file which implements the main function of the slave firmware and application-level code.

The slave application code is a state machine driven by three possible events: a button press, receiving a PLC message, or transmitting a PLC message. Table 3 lists the states and state transitions. In the code, the slave-states are implemented with simple preprocessor definitions (#define) in the form DC_PLC_SLAVE_STATE_XXX where XXX is the state name as referenced in the table.

Table 3. State Transitions

CURRENT STATE	NEXT STATE	TRIGGERS	COMMENTS
INITIAL	WAIT	Button press	Default state after power-up. The slave has no assigned address and blinks the LEDs periodically to alert the user. A button press causes it to send an address request to the master.
WAIT	INACTIVE	RX message	Default state after power-up. The slave has no assigned address and blinks the LEDs periodically to alert the user. A button press causes it to send an address request to the master.
INACTIVE	INACTIVE_WAIT	Button press	In this state, the LEDs are off (for example: inactive). A button press will trigger an event message to the master and the slave will then wait for a response indicating it should turn on its LEDs
INACTIVE_WAIT	ACTIVE	RX message	In this state the slave is waiting for a response from the master after sending an event. Upon receiving an appropriate response it will turn on the LEDs and enter the active state
ACTIVE	INACTIVE	RX message	In this state the LEDs are on (for example: active). An appropriate event message from the master will tell the slave to turn off the LEDs and re-enter the inactive state.

8.3 GUI Software

The GUI included with the demonstration system is a Qt-based application which can run on a variety of platforms. This section describes the GUI software including necessary steps for building the application.

The Qt based GUI has been built and tested in both a Windows PC and AM335x EVM (TMDXEVM3358) environment. For PC , Qt SDK 4.8.4 with Qt Creator 2.7.0 were used. For AM335x, the Qt SDK included with TI's LINUXEZSDK 5.xx or higher can be used with Qt Creator 2.7.0

8.3.1 Building the Application

The following SDKs and software are required to build the GUI application:

- Qt SDK
- Qt Creator

The remainder of these instructions assume that the previous software is installed as well as some general familiarity of the user with Qt-application development.

To build the GUI code, open the project file gui/dc_plc_gui/dc_plc_gui.pro in the Qt Creator. This project references the qtextserialport project directly and opening the project separately is not necessary.

Once the project is opened, the code can be built by selecting *Build → Build All* from the Qt Creator menu.

8.3.2 Application Source Files

Table 4 lists the details of the source files included in the GUI application.

Table 4. GUI Source Files

FILE	DESCRIPTION
`dc_plc_gui.h` `dc_plc_gui.cpp`	Main GUI includes file and source file. Implements application code for button responses and other actions. Selected pre-processor definitions in the include file must match those of the C2000 firmware for correct operation.
`comm.h` `comm.cpp`	Include and source file for communication APIs. Provides simple wrappers for constructing messages to be sent over UART to the PLC network.

8.3.3 Addressing and Control Protocol

This section provides further details on the addressing and control protocol built on top of the PLC-Lite MAC and PHY layers.

The key features of the addressing protocol are:

1. Dynamic address request and assignment between slaves and masters
2. Broadcast query of all slave node states in the network
3. Send and receive control events between the slave and master

The addressing protocol uses the PLC-Lite MAC-address filtering to implement unique node address as well as broadcast addresses.

Each node is given a 16-bit address. Addresses 0x0000 and 0xFFFF are reserved for the master node and broadcast respectively. Slave nodes can have an arbitrary starting address until an address is assigned by the master. Slave nodes begin in an *unassigned* state to avoid collisions of address assignment because of arbitrary starting addresses. In the unassigned state, slaves do not respond to address assignment messages unless a previous address request was sent.

Figure 32 shows the overall structure of the packets in the addressing protocol. The packet comprises of 96-bits which then become the Physical Packet Data Unit (PPDU) in the PLC-Lite PHY layer. The packet is organized around 16-bit units of data to simplify packet management. However, the protocol can be easily modified to optimize for smaller data fields if desired. The components of the packet are as follows:

- **UART** (see Figure 32)

Type — message type designator

Tag — optional message tag (not used)

Payload length — length of payload to follow in bytes

Padding — optional padding (not used)

- **PLC-Lite PHY (Physical-Packet Data Unit, PPDU)** (see Figure 32)

Src Addr— 16-bit source node address

Dest Addr— 16-bit destination node address

Type — 16-bit message-type designator

Data — 2 x 16-bit data field that is application-specific and message-specific

CRC — 16-bit CRC of packet contents (**not used**, but can be implemented)

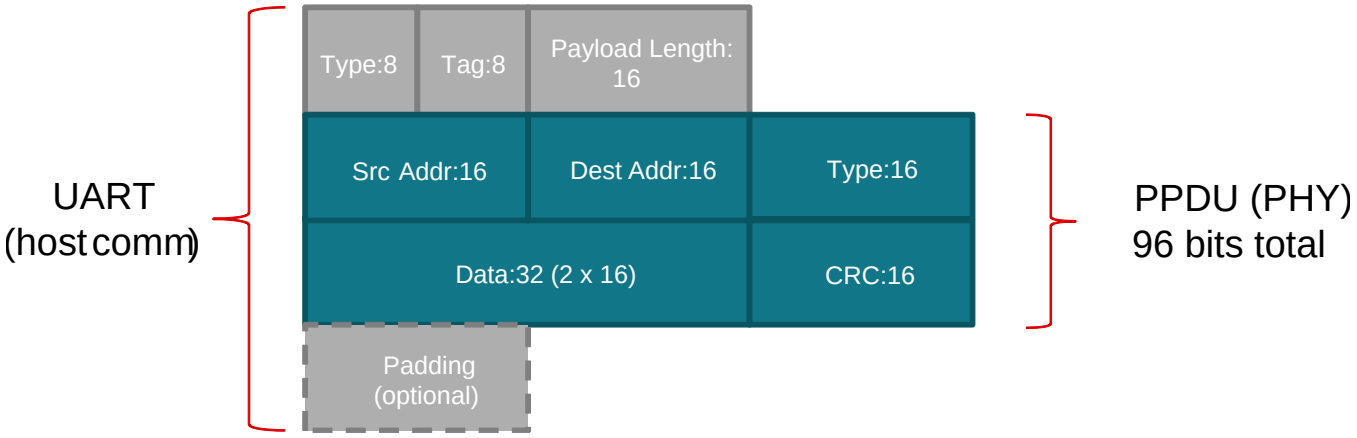


Figure 32. Packet Structure

8.3.3.1 Adjusting PLC-Lite Parameters

The PLC-Lite stack parameters used by the addressing protocol are fixed at compile-time but can be easily modified by the developer if needed. The parameters are modified by changing the appropriate pre-processor definitions in the address_protocol.h header file. Table 5 lists key parameters for tuning. For more details on the parameters as they relate to the PLC-Lite stack, please see the PLC-Lite User's Guide which is part of the software package (SPRCAC9).

Table 5. Tuning Parameters

PRE-PROCESSOR DEFINITION	PARAMETER	DETAILED DESCRIPTION
PHY_TX_DEFAULT_LEVEL	PLC-Lite PHY transmission level; from 0 to 7 with 0 as the highest power.	Sets the output power of the AFE031 used by the PHY software. Maximum output level is approximately 13 Vpp. Typically settings of 5 or 6 for this parameter are sufficient for the demonstration but can depend on power supply and cabling used.
PHY_TX_DEFAULT_MOD	PLC-Lite data-payload modulation-coding scheme. See PLC-Lite documentation (SPRCAC9) for details on available modulation schemes.	Can be used to select more robust modulation coding schemes if needed, generally at the expense of datarate and, therefore, system latency. The default setting of 4 (DBPSK + FEC) has been thoroughly tested.
PHY_DEFAULT_ROBO_HEADER	PLC Lite ROBO setting for PHY layer header	Enables and disables ROBO mode for the PHY header — disabling reduces overhead for each transmission and is recommended for this application.

9 Test Data

9.1 Multiple Slave Nodes Support

The reference design is optimized from an impedance perspective to support multiple slave nodes. Refer to the SAT0021 schematic (see Figure 53), as more and more nodes are added, the C11 capacitor is added in parallel and therefore the total capacitance as seen by a slave node increases. To support multiple slave nodes, the source impedance must be very small as compared to the load impedance (see Figure 33).

C11 (100 pF) creates a low-pass filter and, as multiple nodes are added, the effective capacitance increases. Note that a PLC network is a star topology where each node drives the effective combination load of every other node. Thus C11 is chosen to be 100 pF such that even when up to 10 nodes are added the effective capacitance would be 100 pF x× 10 = 1nF. Therefore the impedance at the PLC-modulation band (see Figure 4) is calculated with Equation 1

$$\text{Impedance} = \frac{1}{2\pi f C} = \text{approximately } 1.8\,\text{k}\Omega$$

where

- f = 90 kHz
- C = 1 nF = 100 pF × 10 (1)

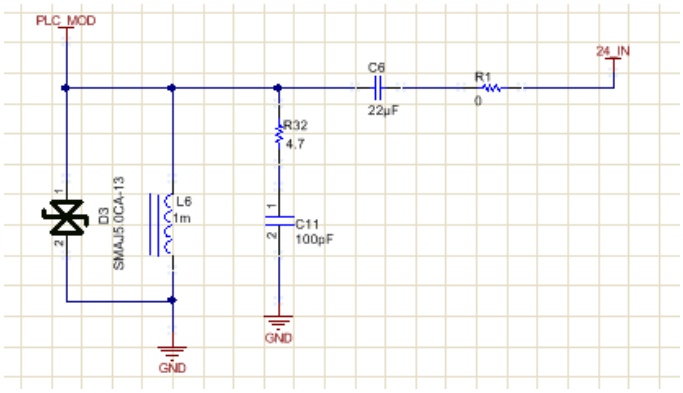


Figure 33. Power-Line Communication AC-Coupling Protection Circuitry

NOTE: Equation 2 is a key requirement to drive multiple slave nodes.

Source Impedance << Load Impedance (2)

For the following calculation assume that the PLC-Lite modulation frequency is approximately 40 KHz. The source impedance of a PLC node is then calculated as shown in Equation 3.

$$\text{Source Impedance} = \frac{1}{2\pi f c} = \frac{1}{2\pi(40000)(0.000022)} = 0.18\ \Omega$$

where

- c = C6 = 22 µF (see Figure 33) (3)

Assume that the load impedance of a given slave node as seen by the driver PLC-node is approximately 30 Ω. As multiple slaves are added, this load impedance is reduced as the loads are seen as a parallel combination of load impedances. For example, if there are nine slaves on the system, then the total load impedance as seen by one driver PLC-node is calculated as shown in Equation 4.

9 (slaves) + 1 (Master) = 10 PLC nodes, Load Impedance = 30/10 = 3 Ω (4)

4 (slaves) + 1 (Master) = 5 PLC nodes, Load Impedance = 30/5 = 6 Ω (5)

Based on the system requirements, optimizing the capacitance C6, 22 µF, and C11, 100 pF, is important in order to meet the requirement of Equation 2.

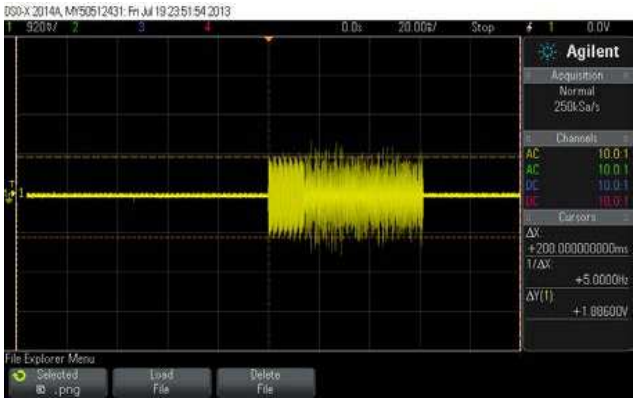


Figure 34. Test Results: One Master and Four Slaves

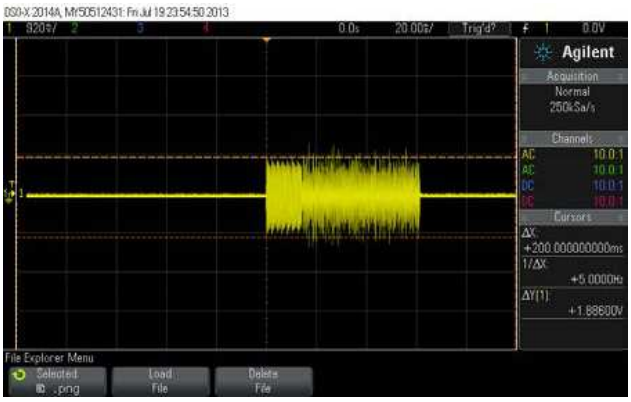


Figure 35. Test Results: One Master and No Slaves

As seen in Figure 34 and Figure 35, there is an insignificant change in amplitude of the modulation signal as more slaves are added. In the previous setup, the 24-V DC line is probed (AC coupled) to the oscilloscope. The oscilloscope is triggered when the button on the PLC node is pressed as it generates a PLC communication packet.

9.2 Multiple Slave transmissions and System Latency

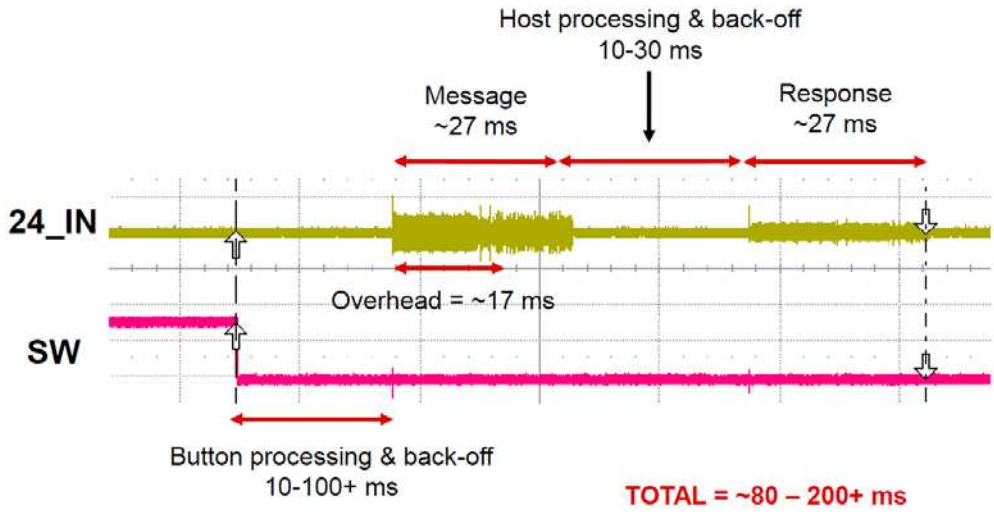


Figure 36. System Latency

PLC-Lite contains a simple CSMA/CA, MAC which means that if multiple slaves try to access the 24-V DC line, the MC layer in PLC-Lite senses that the line is busy and backs off for a random duration. The total latency for a typical transaction is thus a function of this random back-off for both the initial message and response, as well as the fixed time required to transmit the messages on the line. As shown in Figure 36, the system-level latency with one button press event was captured at approximately 80 to 200 ms. This measurement is typical for the default MAC and PHY layer settings used by the demonstration firmware. Modifying MAC or PHY layer parameters can change the system latency.

9.3 15-V Power-Supply Performance for AFE Power Amplifier

For this reference design, note that the 24-V DC supply generates a 15-V and 3.3-V supply as well as it is modulated by the AFE031 for PLC communication. The key point to note is that the switching-regulator operation that generates the 15 V and 3.3 V can interfere with PLC modulation if proper power supply filtering is not included in the design.

To ensure the above requirement, refer to the schematic as shown in Figure 37: the first circuit seen by the 24-V DC line is a low-pass filter (see Section 9.3.1) which is a very important element of the design. Without this low-pass filter circuit, PLC communication will not work.

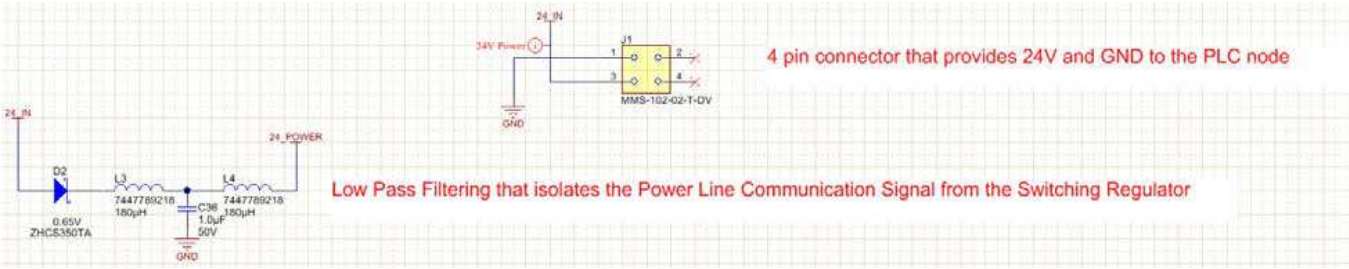


Figure 37. Power Section of the Schematic Showing the Low-Pass Filter

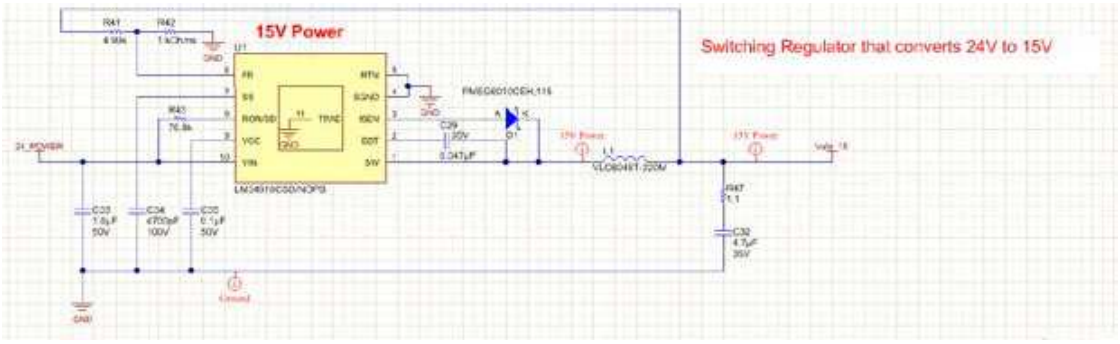


Figure 38. 15-V Section of the Power Schematic

In the DC-PLC reference design, another key requirements is to ensure that in an application when a PLC node transmits or receives data, the power amplifier for the AFE031 device is provided with the necessary power (500-mA power budget for the maximum TX swing, see Section 8.3.3.1) to drive the line and to drive the line with a fast response time. The LM34910 step-down switching regulator is used in this reference design (see Figure 38) to generate the 15 V for the power amplifier of the AFE031 device. The LM34910 device features all of the functions required to implement a low-cost efficient buck-bias regulator capable of supplying up to 1.25 A to the load. This buck regulator contains a 40-V N-Channel buck switch, and is available in the thermally enhanced WSON-10 package.

NOTE: The LM34910 device features a hysteretic-regulation scheme that requires no loop compensation, results in fast load-transient response, and simplifies circuit implementation.

The operating frequency remains constant with line and load variations because of the inverse relationship between the input voltage and the on-time.

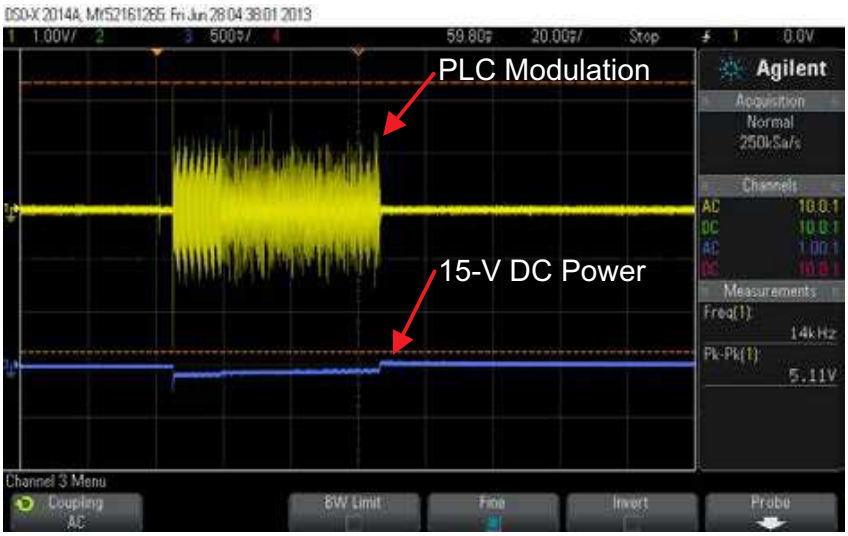


Figure 39. LM34910 With a 22-µH Inductor (TX Level 2 Vpp)

As shown in Figure 39, the LM34910 device as implemented in this reference design, provides the necessary power for the AFE031 to meet the PLC functionality.

NOTE: As seen in Section 9.5, the TX level of 2 Vpp is enough to drive up to a 40-m (length) cable without any BER.

9.3.1 T-Type Low-Pass Filter Design

As shown in Figure 37 and Figure 38, a low-pass filter separates the PLC modulation signal from the switching regulator. The Fc of the low-pass filter is calculated based on the band occupied by the PLC modulation. As shown in Figure 4, the PLC Lite occupies 42 to 90 kHz. Therefore, the Fc as per the low pass filter in Figure 37 comprises of L = 360 µH (180 µH + 180 µH) and C of 1 µF.

$$Fc = \frac{1}{\pi \times \sqrt{LC}} = \text{approximately } 17 \text{ kHz} \quad (6)$$

NOTE: Because of the space constraint on this reference design, the previous values of LC were selected. However in applications where board space is available, a lower cutoff Fc (lower than 10 KHz) is desirable.

9.4 PLC-Coupling Circuit Protection

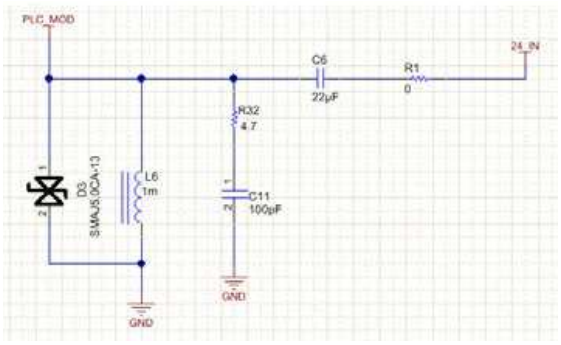


Figure 40. First-Stage AC Coupling

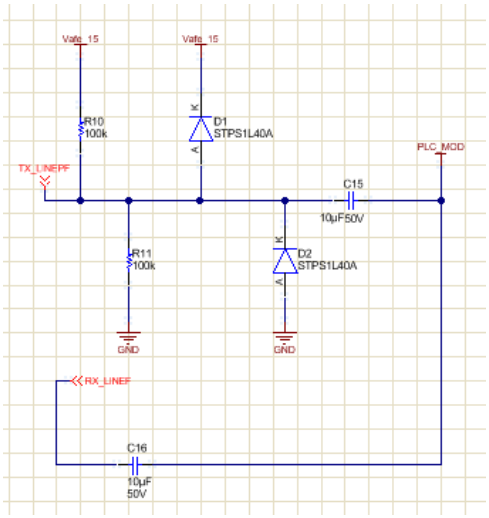


Figure 41. Second-Stage AC Coupling

To ensure the reliability of the overall system, the 24-V line is not directly AC coupled to the AFE031 device. The line goes through a two-step AC coupling (see Figure 40 and Figure 41). In the first stage, the 24-V line is AC coupled to an intermediary stage that has a TVS protection and therefore arrests voltage surges to 9.2 V for a peak surge current of 43.5 A. In this stage the common mode is biased to the GND. In the second-stage AC coupling, the data is AC coupled to the AFE031 device with a DC bias of 7.5 V. To ensure reliability, a simple test of powering off the node completely and then powering up the node was performed on five nodes approximately 250 times. This stress tests ensures that the surges on the power supply can be applied to the node under test.

Table 6. Reliability Data

PLC NODE	COMPLETE POWER-ON AND POWER-OFF SEQUENCE	STATUS
1	250 times	Pass, no reliability failure, no change in current drawn observed pre-stress and post-stress
2	250 times	
3	250 times	
4	250 times	
5	250 times	

9.4.1 PLC TX and RX Impedance-Path Testing

The impedance path of the TX and RX is optimized to avoid any signal losses to the PLC-modulation signal.

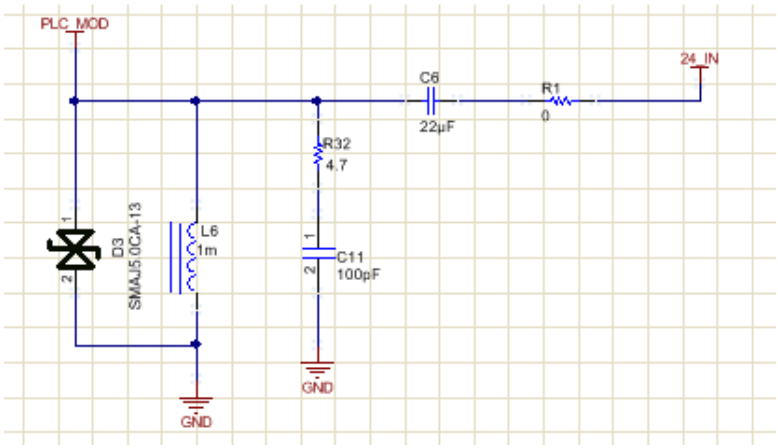


Figure 42. Power-Line Communication AC-Coupling Protection Circuitry

Figure 42 shows that R1 at 0 Ω provides optimized load impedance to the modulation signal. If R1 in Figure 42 is even changed to 15 µH (for example), the modulation signal is severely impeded as shown in Figure 43 and Figure 44.

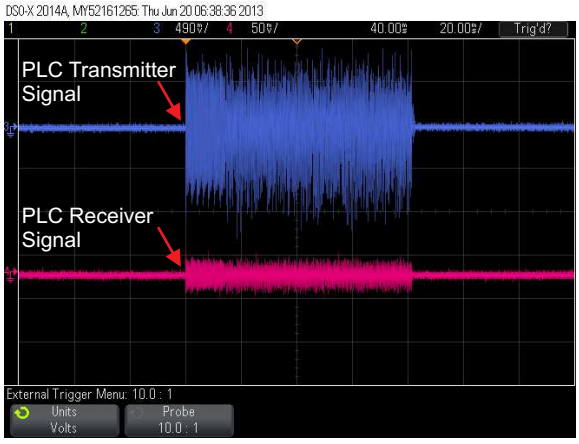


Figure 43. RX Signal Impeded With 15-µH Inductance

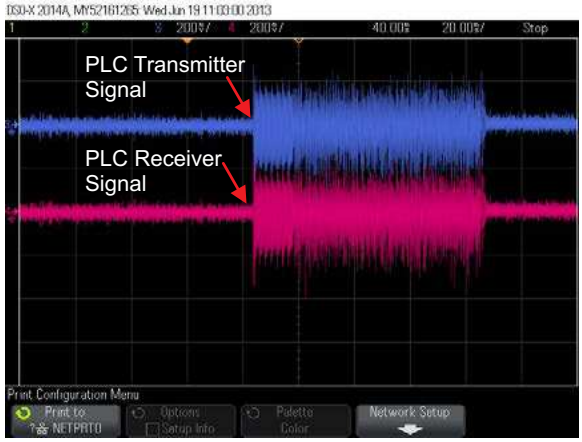


Figure 44. RX Signal Optimized With 0-Ω Resistor (R1)

9.5 PLC-Cable Performance Data

For performance characterization, a 40-m cable was used. To characterize the cable, use the following steps:

1. Generate a chirp signal.
2. Capture the response of the chirp after the cable as shown in Figure 45.
3. Post-process (correlation) the signal using Matlab® to generate the impulse response.
4. Leverage the impulse response of the given 40-m cable to generate approximately 320-m cable impulse response.

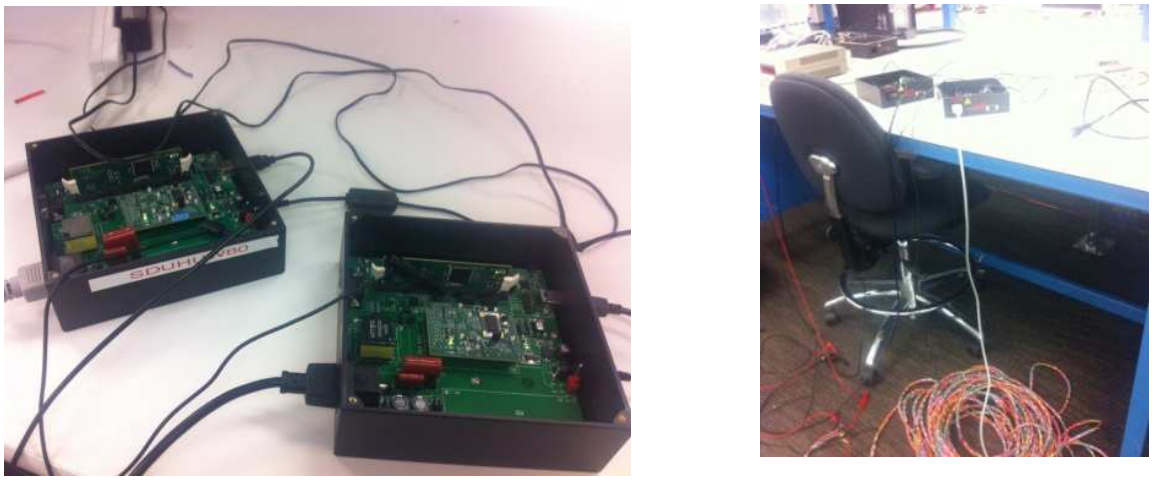


Figure 45. Cable Modeling Approach

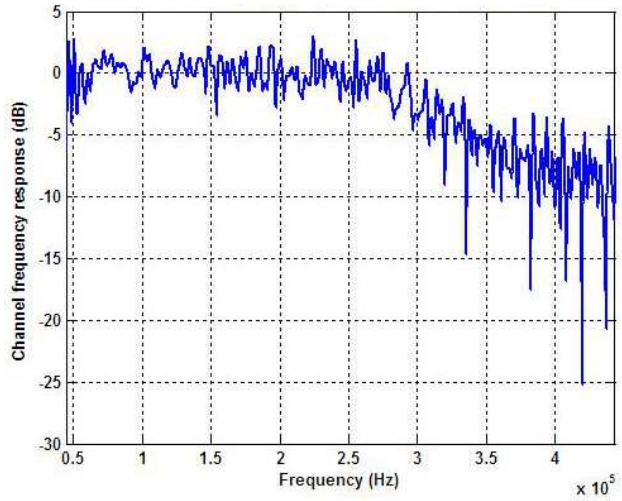


Figure 46. Channel-Frequency Response of 40-m Cable (Using Actual Cable)

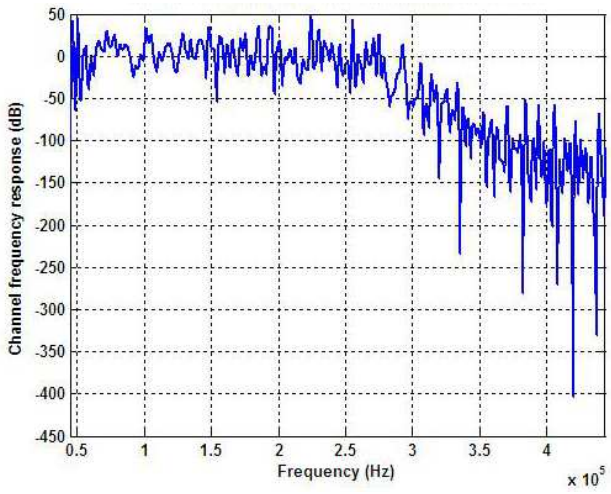


Figure 47. Channel-Frequency Response of 320-m Cable (Extrapolated)

The channel loss of the 320-m cable is not significantly more than the 40-m cable even up to 100 KHz as shown in Figure 46 and Figure 47.

The 40-m cable was then used with the DC-PLC hardware to collect the BER measurements across different AFE031 TX-amplitudes as shown in Figure 48. The software and firmware used to conduct BER testing is part of the PLC-Lite SDK and are not included in the demonstration software provided with this design.

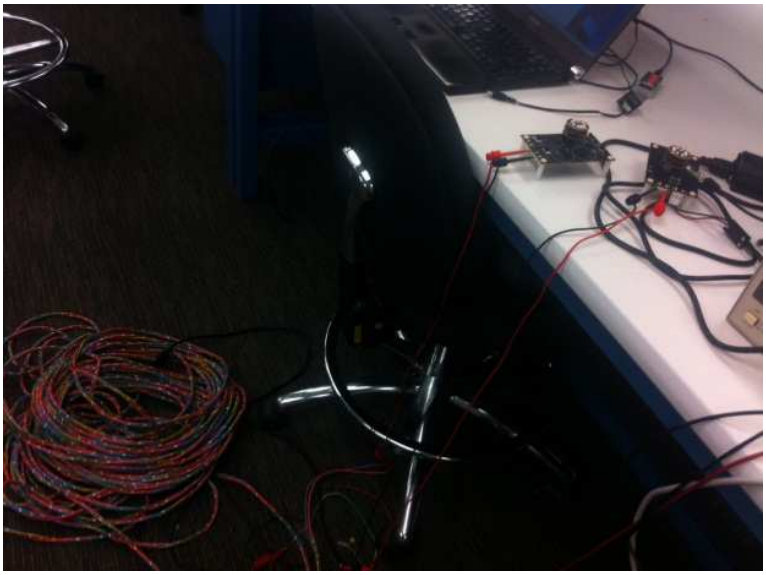


Figure 48. BER Measurement Using the 24-V DC PLC Hardware and the 40-m Cable

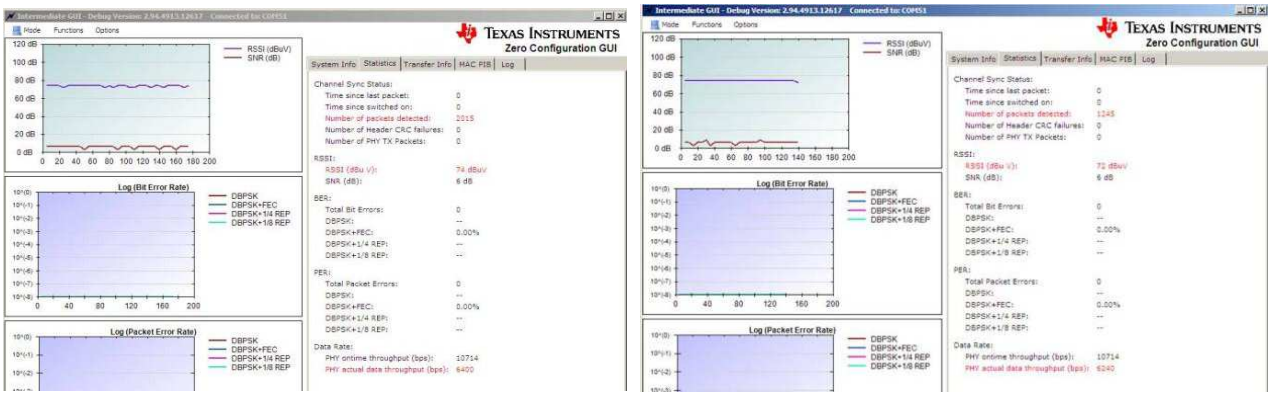


Figure 49. BER Data: No Packet Errors With Levels 5 and 6 (15 dB and 18 dB Below 15-V pp)

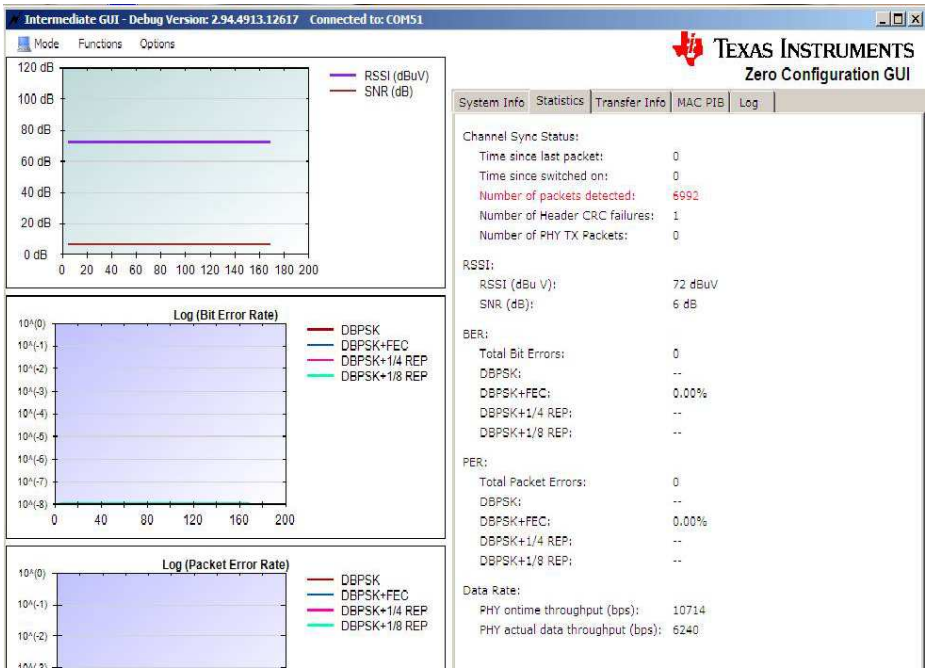


Figure 50. BER Data: No Packet Errors, Level 7 (21 dB Below 15-V pp)

Table 7. BER Measurement Results

TX AFE031 LEVEL	DECIBELS BELOW MAXIMUM AMPLITUDE	BER DATA
5	15 dB	0 packet error out of 10000 packets transmitted
6	18 dB	
7	21 dB	

The data listed in Table 7 confirms that the TI PLC-Lite solution with an OFDM solution can support cable length up to 320 m with a very-low TX amplitude of the AFE031 (see Section 8.3.3.1) resulting in a large margin to support even longer cables.

9.5.1 Thermal Performance of the Design

To confirm the thermal performance of the design a simple test was performed. To perform the test, the power amplifier was programmed to send a PLC-modulation signal every 1 second. Thermal-imaging camera hot spots were analyzed at time (t0) and then 30 minutes after launching the application (t1). The purpose of this test is to confirm that the design can effectively dissipate heat without localized heating.

As shown in Figure 51 and Figure 52, there is no localized heating observed in the system after time, t1, compared to t0. For layout guidelines of the AFE031 device and high-current trace routing, see Section 13.1.

NOTE: For the thermal-performance application testing, the TX setting for the AFE031 device was set to Level 3 (see Section 8.3.3.1).

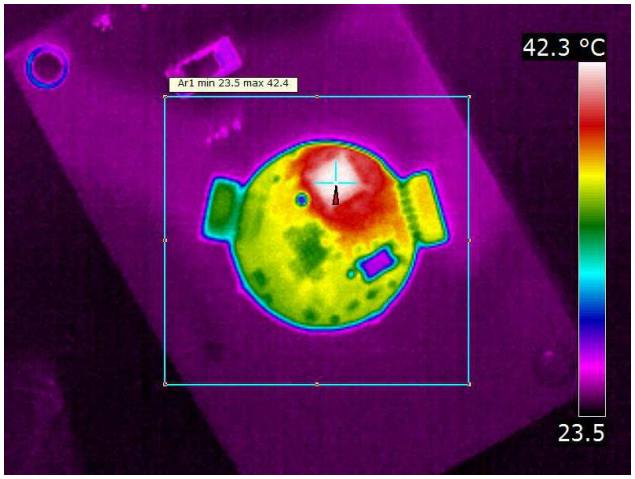


Figure 51. t0

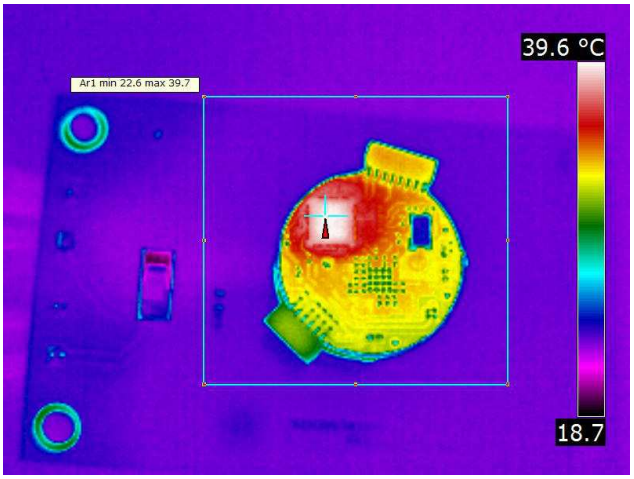


Figure 52. t1

9.6 IEC Electrostatic-Discharge Testing

The UART and JTAG interface pins on the SAT0022 processor section have IEC ESD-protection up to ±30-kV air, as well as ±30-kV contact which is provided by the TPD1E10B06 device from TI (see the product folder for more information, http://www.ti.com/product/tpd1e10b06). Table 8 lists the device level-IEC ESD testing data.

Table 8. Device-Level IEC ESD Testing

LEVEL	IEC-CONTACT SPEC = ± 30 kV			IEC-AIR SPEC = ± 30 kV		
	UNIT1	UNIT2	UNIT3	UNIT1	UNIT2	UNIT3
±2 kV	PASS	PASS	PASS	PASS	PASS	PASS
±4 kV	PASS	PASS	PASS	PASS	PASS	PASS
±6 kV	PASS	PASS	PASS	PASS	PASS	PASS
±8 kV	PASS	PASS	PASS	PASS	PASS	PASS
±15 kV	PASS	PASS	PASS	PASS	PASS	PASS
±20 kV	PASS	PASS	PASS	PASS	PASS	PASS
±25 kV	PASS	PASS	PASS	PASS	PASS	PASS
±30 kV	PASS	PASS	PASS	PASS	PASS	PASS

10 Schematics

The schematics are presented in the following order:

1. PLC Node
   - Power Section — SAT0021 (see Figure 53)
   - C2000 and AFE031 — SAT0022 (see Figure 54, and Figure 55)
   - Application Board — SAT0023 (see Figure 56)
2. Master Base Board — SAT0029 (see Figure 57)
3. Slave Base Board — SAT0030 (see Figure 58)
4. JTAG Programming Board — SAT0024 (see Figure 59)
5. USB to UART Board — SAT0045 (see Figure 60)

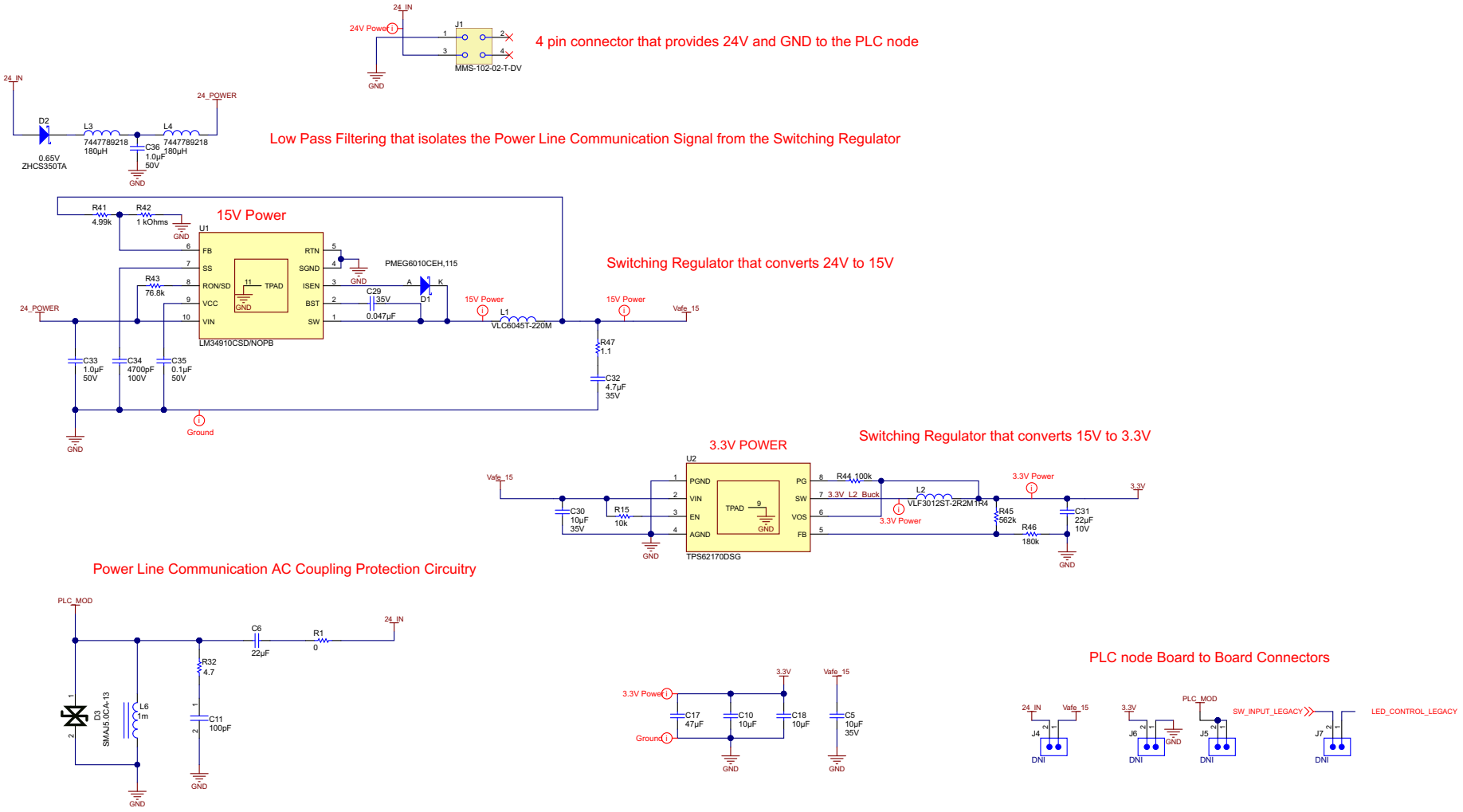


Figure 53. SAT0021 — Power Section of the PLC Node

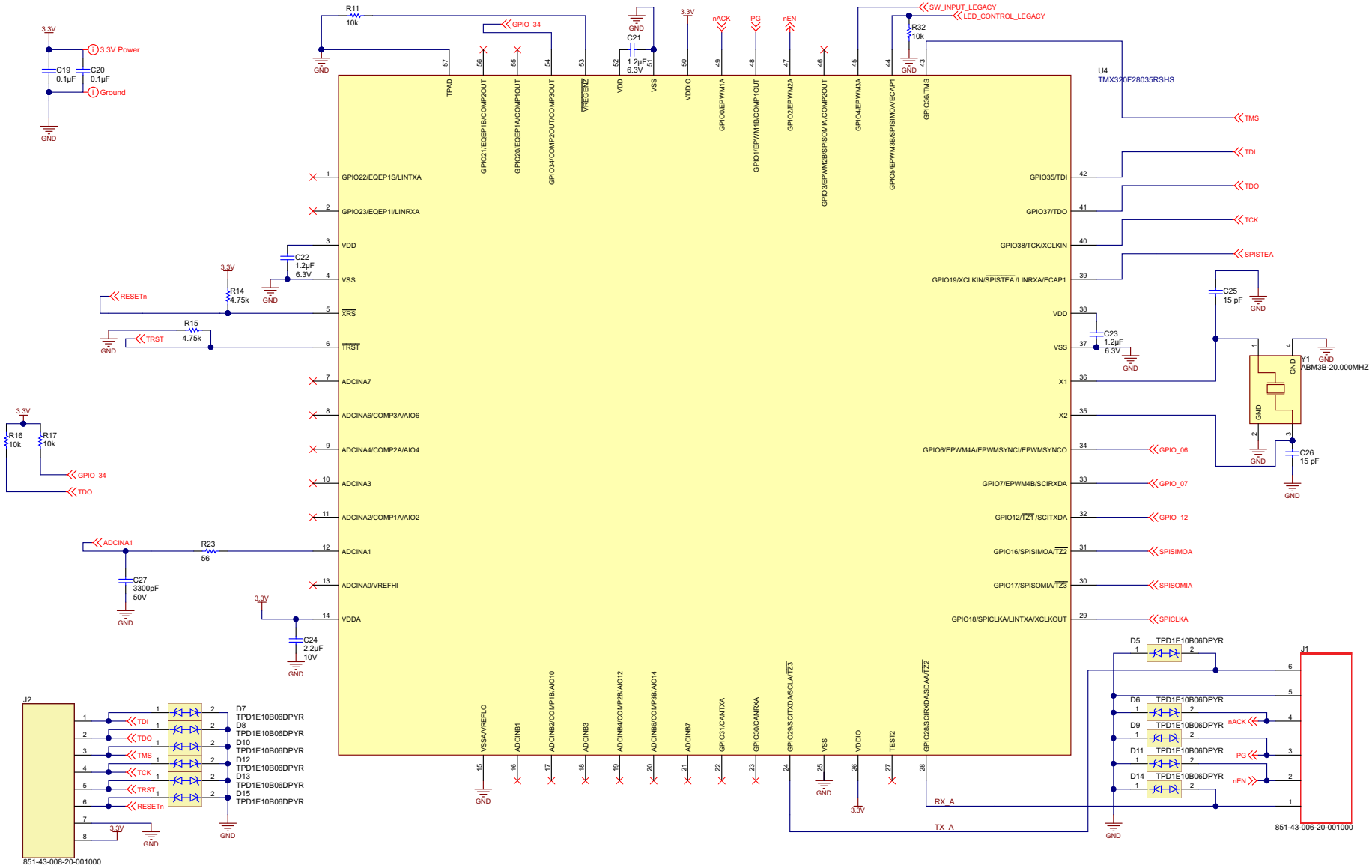


Figure 54. SAT0022 — Processor Section of the PLC Node

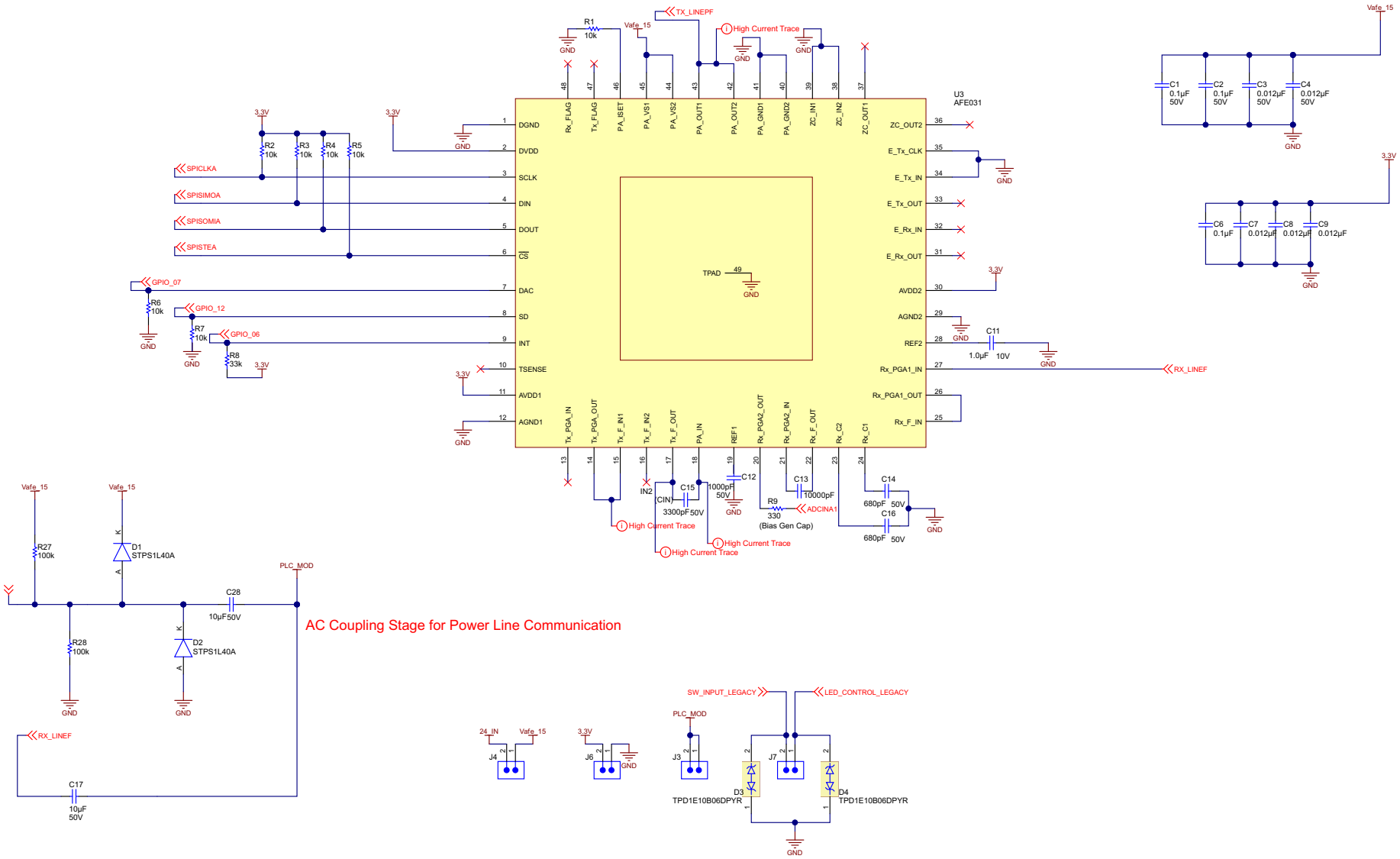


Figure 55. SAT0022 — AFE Section of the PLC Node

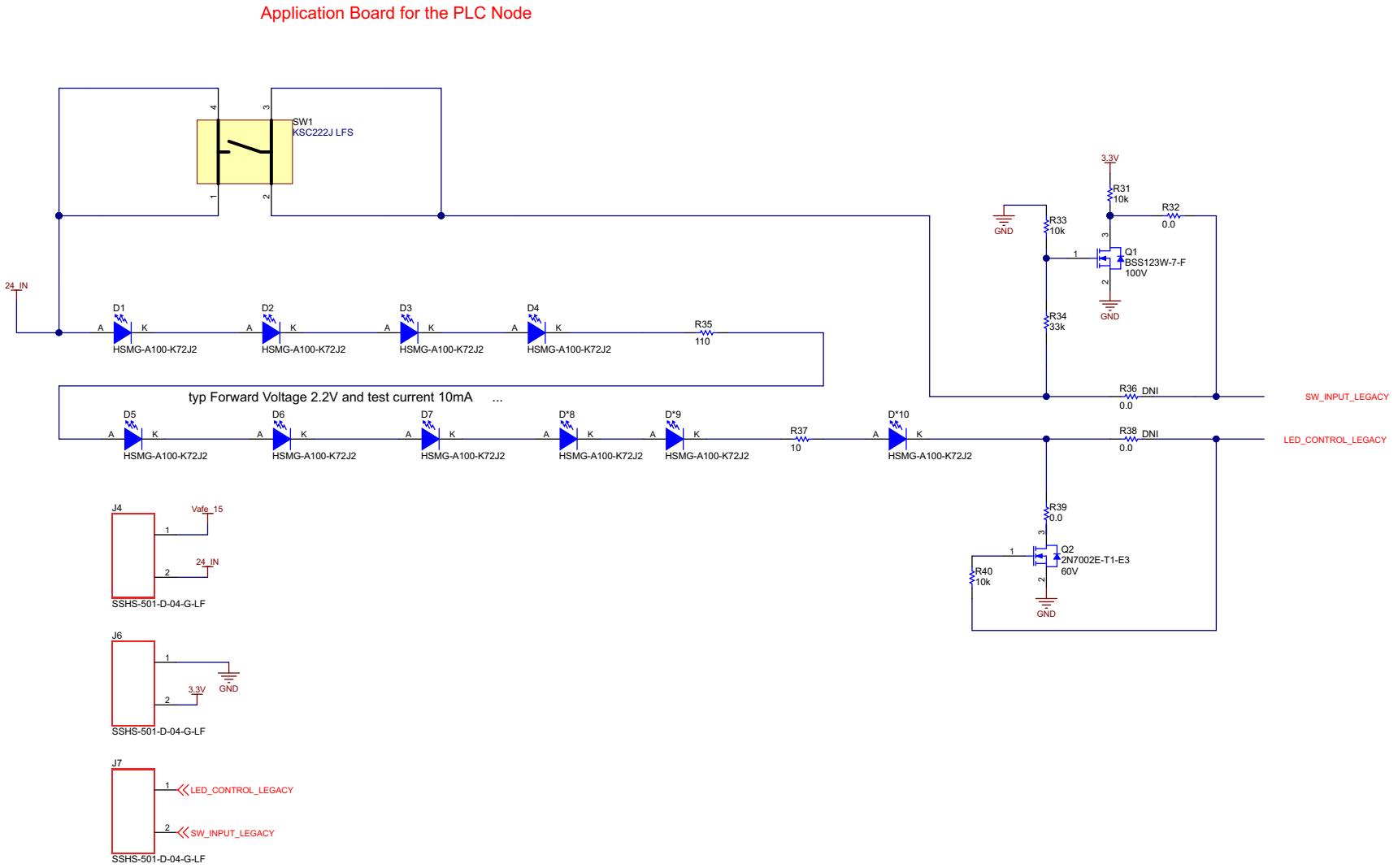
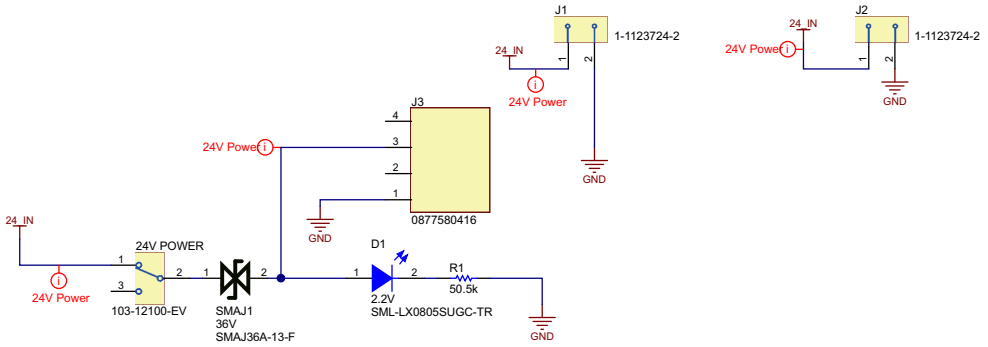
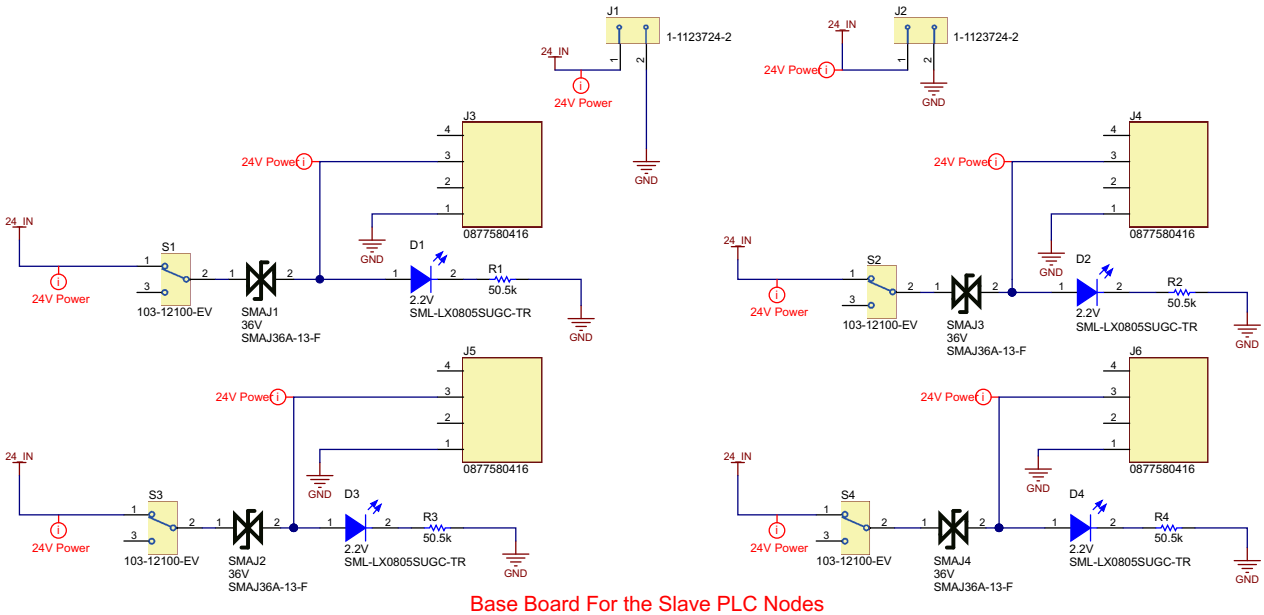


Figure 56. SAT0023 — Application Section of the PLC Node



Base Board For the Master PLC Node

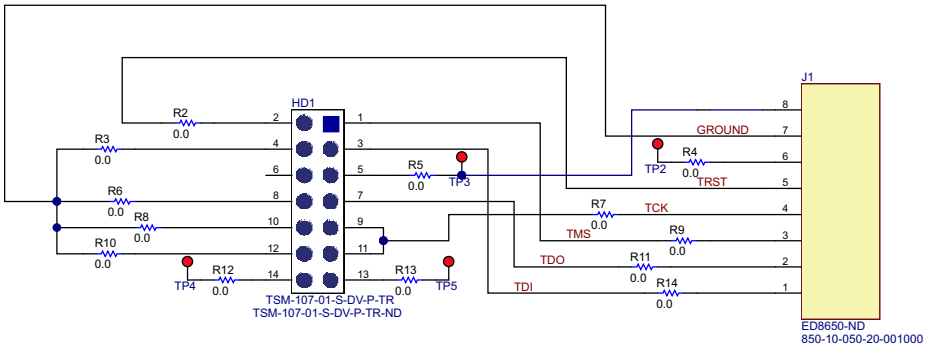
Figure 57. SAT0029 — Base Board to Mount the Master PLC



Base Board For the Slave PLC Nodes

Figure 58. SAT0030 — Base Board to Mount the Slave PLC Nodes

Interface Board that connects to the 8 pin connector (C2000 - processor) for JTAG programming



This board connects to the 8-pin connector (C200 processor) for JTAG.

Figure 59. SAT0024 — JTAG Interface Board for Programming C2000

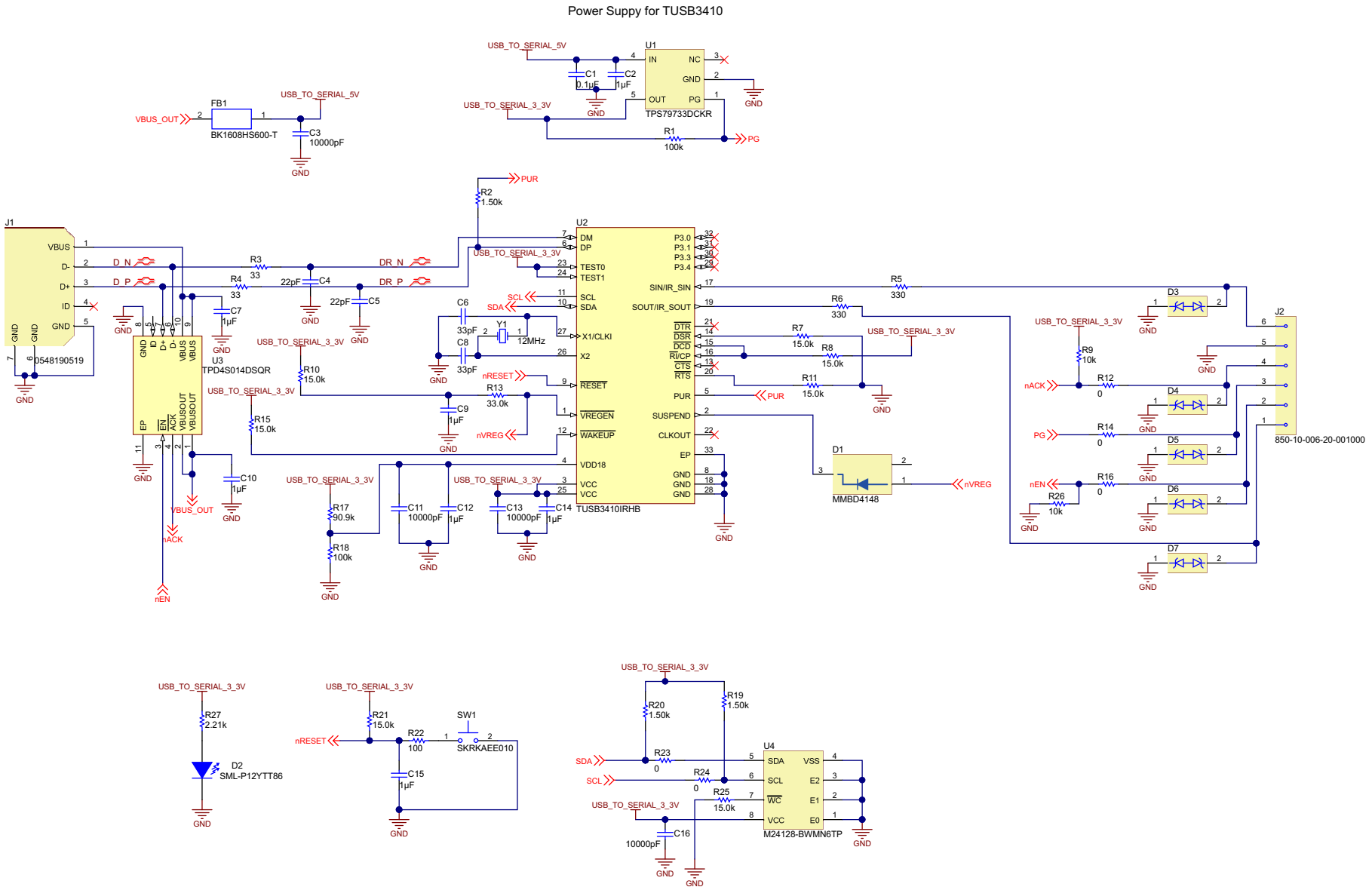


Figure 60. SAT0045 — USB to UART Interface Board for Host-to-Master PLC-Node Communication

11 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure 61 shows the BOM for the SAT0022.

LINE NO	KS PART NUMBER	CUSTOMER PART NUMBER	QTY	VALUE	DESIGNATORS	PKG/ CASE	T.COEFF/ PWR	TOL	VOLT RATED	DESCRIPTION	DISTRIBUTOR	DIST P/N	MANUFACTURER	MNFR. PART #	LOT NO
1	27513	B 14	2	0.012µF	C3, C4	0402	X7R	10	50V	Capacitors	Digi-Key	399-9949-1-ND	Murata	GRM155R71H123KA12D	K10000048010
2	27513	B 14	3	0.012µF	C7, C8, C9	0402	X7R	10	50V	Capacitors	Digi-Key	399-9949-1-ND	Murata	GRM155R71H123KA12D	K10000048010
3	22444	B 7	4	0.1µF	C1, C2, C19, C20	0402	X7R	10	50V	Capacitors	Digi-Key	445-5932-2-ND	Tdk Corporation	C1005X7R1H104K	K10000028604
4	12420	B 9	1	0.1µF	C6	0402	X7R	10	16V	Capacitors	Digi-Key	445-4952-2-ND	Tdk Corporation	C1005X7R1C104K	K10000049921
5	27514	B 14	1	1.0µF	C11	0402	X7S	10	10V	Capacitors	Digi-Key	445-9116-1-ND	Tdk Corporation	C1005X7S1A105K050BC	K10000048128
6	11116	B 1	1	10000pF	C13	0402	X7R	10	50V	Capacitors	Digi-Key	490-4516-2-ND	Murata Electronics North Am	GRM155R71H103KA88D	K10000049918
7	11296	B 1	1	1000pF	C12	0402	X7R	10	50V	Capacitors	Digi-Key	445-1256-2-ND	Tdk Corporation	C1005X7R1H102K	K10000032586
8	11229	B 1	2	15pF	C25, C26	0402	C0G	5	50V	Capacitors	Venkel	C0402COG500-150JNE	Venkel	C0402COG500-150JNE	OB6223AYV
9	11637	B 2	2	3300pF	C15, C27	0402	X7R	10	50V	Capacitors	Digi-Key	311-1034-2-ND	Venkel	C0402X7R500-332KNE	K10000034924
10	13093	B 3	2	680pF	C14, C16	0402	C0G	5	50V	Capacitors	Digi-Key	490-3240-2-ND	Murata	GRM1555C1H681JA01D	K10000011519
11	12509	C 4	1	2.2µF	C24	0603	X7R	10	10V	Capacitors	Digi-Key	445-5958-2-ND	Murata Electronics North Am	GRM188R71A225KE15D	K10000049081
12	27515	C 17	3	1.2µF	C21, C22, C23	0805	X7R	10	6.3V	Capacitors	Digi-Key	399-4929-1-ND	Kemet	C0805C125K9RACTU	K10000045794
13	24690	E 4	2	10µF	C17, C28	1206	X5R	10	50V	Capacitors	Digi-Key	445-5998-2-ND	Tdk Corporation	C3216X5R1H106K	K10000044076
14	27535	U 179	1	TMX320F28035RSHS	U4	56-VFQFN				Integrated Circuits	Mouser	595-TMS320F28035RSHT	Texas Instruments	TMX320F28035RSHS	K10000049505
15	14220	M 14	11	10.0K	R1, R2, R3, R4, R5, R6, R7, R11, R16, R17, R32	0402	1/10W	1		Resistors	Digi-Key	P10.0KLTR-ND	Yageo America	ERJ-2RKF1002	K10000048777
16	11016	M 1	2	100K	R27, R28	0402	1/16W	1		Resistors	Digi-Key	311-100KLRTR-ND	Yageo America	RC0402FR-07100KL	K10000045631
17	11322	M 4	1	33.2K	R8	0402	1/16W	1	50V	Resistors	Digi-Key	P33.2KLTR-ND	Panasonic - Ecg	ERJ-2RKF3322X	510283380
18	21035	M 24	1	330	R9	0402	±100ppm/°C	1	1/10W	Resistors	Digi-Key	P330LTR-ND	Panasonic - Ecg	ERJ-2RKF3300X	K10000049592
19	28777		2	4.75K	R14, R15	0402	1/16W	0.1		Resistors			Panasonic - Ecg	ERA-2AEB4751X	
20	13137	M 11	1	56.2	R23	0402	1/16W	1	75V	Resistors	Digi-Key	P56.2LTR-ND	Panasonic - Ecg	ERJ-2RKF56R2X	7121255502
21	24301	X 8	13	TPD1E10B06DPY	D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15	0402			6.0V	Circuit Protection	Texas Instruments	TPD1E10B06DPYR	Texas Instruments	TPD1E10B06DPY	K10000042224
22	27533	AE 41	2	STPS1L40A	D1, D2	DO-214AC, SMA	1A		40V	Discrete Semiconductor Products	Digi-Key	497-3753-1-ND	Stmicroelectronics	STPS1L40A	K10000048127
23	27534	U 175	1	AFE031AIRGZT	U3	48-VQFN				Integrated Circuits	Texas Instruments	AFE031AIRGZT	Texas Instruments	AFE031AIRGZT	K10000045657
24	27536	W 13	1	20.0000MHz	Y1	4-SMD 5mm x 3.2mm	-20°C ~ 70°C	20	18pF	Crystals	Digi-Key	535-9125-1-ND	Abracon Corporation	ABM3B-20.000MHZ-B2-T	K10000049524
25	20983-6	AM 78/LB 12	1	1 X 6 R/A	J1	0.05"				Connectors	Digi-Key	851-43-010-20-001000	Mill-Max	851-43-010-20-001000	K10000044132
26	20983-8	AM 78/LB 12	1	1 X 8 R/A	J2	0.05"				Connectors	Digi-Key	851-43-010-20-001000	Mill-Max	851-43-010-20-001000	K10000044132
27	26194	AM 88	4	FW-50-01-L-D	J3, J4, J6, J7	0.05"				Connectors	Samtec	FW-50-01-L-D-300-280	Samtec	FW-50-01-L-D-300-280	K10000041242

Figure 61. SAT0022 — BOM

12 Layer Plots

To download the layer plots for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure 63, Figure 63, and Figure 64 show the layer plots for the SAT0021, SAT0022, and SAT0023 respectively.

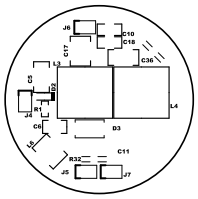


Figure 62. SAT0021 — Layer Plot

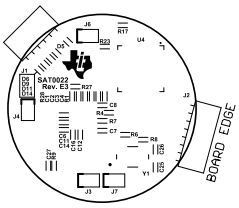


Figure 63. SAT0022 — Layer Plot

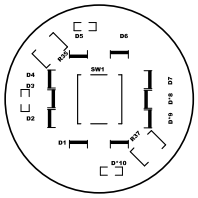


Figure 64. SAT0023 — Layer Plot

13 Altium Project

To download the Altium project files for each board, see the design files at www.ti.com/tool/24VDCPLCEVM. Figure 65, Figure 66, and Figure 67 show the layout for the SAT0021, SAT0022, and SAT0023 respectively.

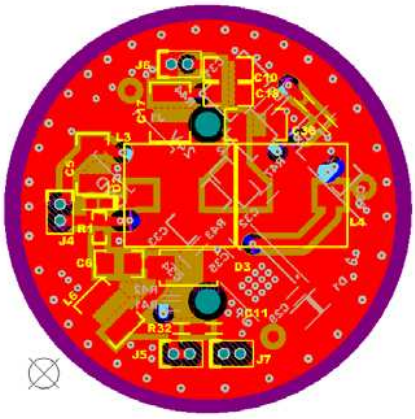


Figure 65. SAT0021 — Layout

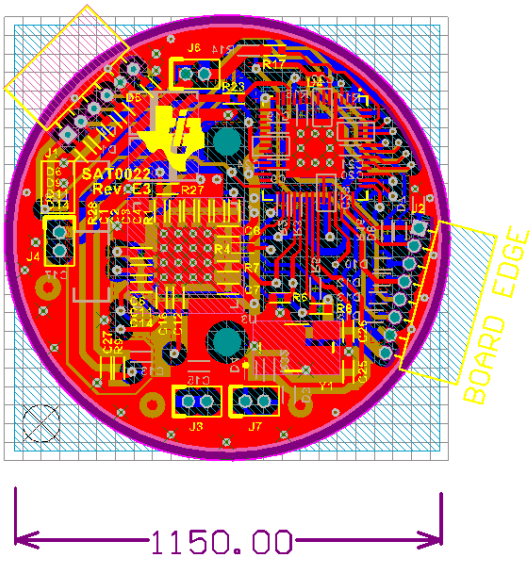


Figure 66. SAT0022 — Layout

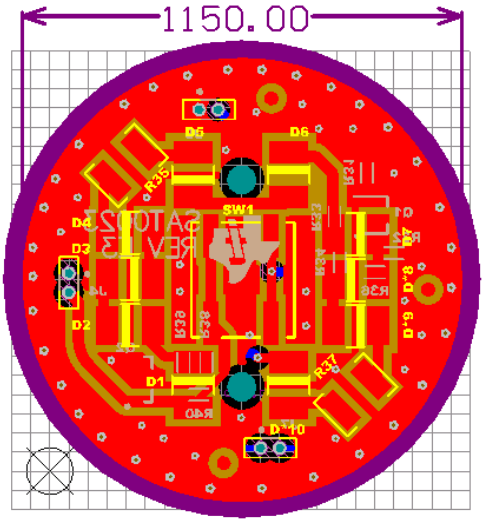


Figure 67. SAT0023 — Layout

13.1 AFE031 High-Current Trace Layout

In a typical power-line communications application, the AFE031 device dissipates 2 W of power when transmitting into the low impedance of the AC line. This amount of power dissipation can increase the junction temperature. An increase in junction temperature can lead to a thermal overload that results in signal transmission interruptions if the proper thermal design of the PCB has not been performed. Proper management of heat flow from the AFE031 device as well as good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend device operating life.

For a layout example of high-current traces see Figure 68. To achieve lower thermal resistance, 2-oz copper was used in the design as shown in Figure 69.

NOTE: The AFE031 device has a power amplifier (see Figure 2) that requires high-current trace layout.

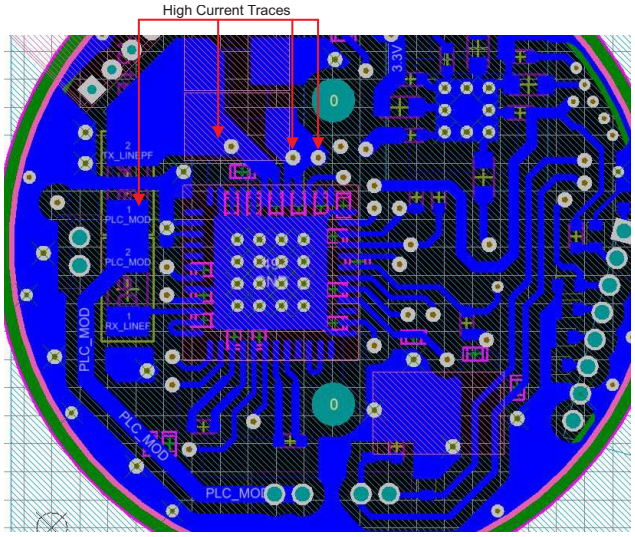


Figure 68. High-Current Traces

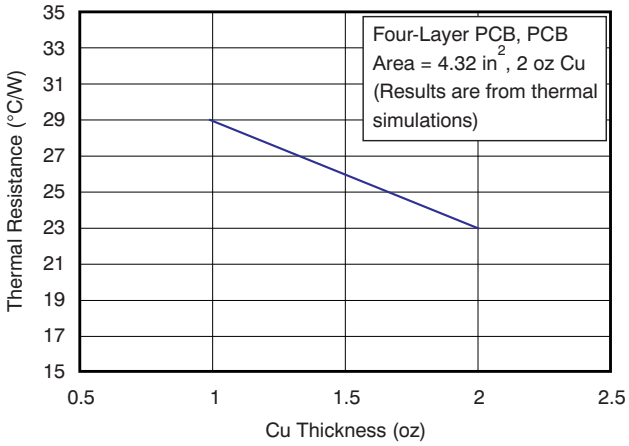


Figure 69. AFE031 — Thermal Resistance as a Function of Copper Thickness

See Section 9.5.1 for thermal performance data of the design when the application software is running.

14 Gerber Files

To download the Gerber files for each board, see the design files at www.ti.com/tool/24VDCPLCEVM

15 Software Files

To download the software files for the reference design, see the design files at www.ti.com/tool/24VDCPLCEVM

16 About the Author

AJINDER PAL SINGH is a Systems Architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Ajinder brings to this role his extensive experience in high-speed digital, low-noise analog and RF system-level design expertise. Ajinder earned his Master of Science in Electrical Engineering (MSEE) from Texas Tech University in Lubbock, TX. Ajinder is a member of the Institute of Electrical and Electronics Engineers (IEEE).

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