F280041 ADC Interrupt Overflow Issue Summary

Background and Issue Description:

- Basic configuration：
  a. ADCA SOC1 will sample the current and EOC1 will trigger ADCAINT1 for control loop calculation, where SOC1 receives CPUTimer0 as trigger source at frequency 80kHz@12.5us;
  b. The system only enables 1 interrupt i.e. ADCAINT1, so no other interrupts or nesting interrupts in the system, also global interrupt enable is operated only in the system initialization stage prior to the for(;;); loop and there're no further codes to disable or enable it anymore afterwards;
  c. In normal operation, ADCAINT1 ISR execution time is within the sample period, i.e. 12.5us, so we can say the ISR utilization ratio is less than 100% (typically most customers will control it within the range of 60~70% and VMAX is also aware of this);
  d. There's an exception that when a mode switch of their OBC and DCDC occurs, they need to turn off the CPUTimer0 and disable EPWM timer and outputs, and then re-configure the EPWM for new power stage control to re-start in that ADCAINT1 ISR, which will dramatically add execution time to about 3x sample period (or ISR utilization ratio is 300%), i.e. 37.5us;
- Issue was found in condition d) listed above that ADCAINT1 ISR will overflow and not be serviced any more, which means the power stage lost control.

Issue Analysis and Test:

- In condition d), if the execution time is not 3x sample period (or any integral multiple of sample period including 1x) where a new ADCAINT1 to be generated, e.g. 1.8x or 2.5x corresponding to 180% or 250% ISR utilization ratio, it can be serviced again although it's overflow (when 1x or 100% ISR utilization ratio it's not overflow);
- Adding codes (NOP instructions) in the ADCAINT1 ISR to simply increase execution time to 1x, 2x or 3x sample period (ISR utilization ratio corresponding to 100%, 200% or 300%) but removing the mode switch codes can easily re-produce the issue, which means it has nothing to do with the power stage but only relates to the timing;
- By checking other SOCs in ADCA and ADCB/C which accept identical CPUTimer0 trigger source, it's found CPUTimer0 is counting and triggering normally, ADC module is sampling and converting normally, which means issue is occurred in the interrupt pulse generation or PIE process;
- When checking flags set, it's almost exactly identical to the post "TMS320F28027: IFR Interrupt flag stop to be set" below except for PIEIFR register. With only ADCAINT1 interrupt configured:
  - ADCINTFLG = 0x0001;
  - ADCINTOVF = 0x0001;
  - PIEIER1 = 0x0001;
  - PIEIFR1 = 0x0000;
  - IER.bit.INT1 = 1;
  - IFR.bit.INT1 = 0;

  http://e2e.ti.com/support/microcontrollers/c2000/f/171/p/651013/2391803
  http://e2e.ti.com/support/microcontrollers/c2000/f/171/t/418757

Recommendation and Solutions:

- Control ISR execution time within the sample period, or the ISR utilization ratio to be less than 100%, especially within the range of 60~70% like most customers do. In customer system, that is to move the mode switch codes out of ADCAINT1 ISR to for(;;) loop;
- Follow the suggestions list in below post to ensure next new interrupt pulse can be generated and sent to PIE properly: http://e2e.ti.com/support/microcontrollers/c2000/f/171/p/651013/2391803:
  - Clear ADCINTOVF flag by setting ADCINTOVFCLR register in the ADCAINT1 ISR if it's set;
  - Configure ADCINT to run in continuous mode in initialization stage so that interrupts continue to trigger even if they are not serviced in time;

Questions and Support Needs:

- Recommendation and solutions listed above were accepted by customer and verified to work well in their system, while we still need your help to address below 2 questions;

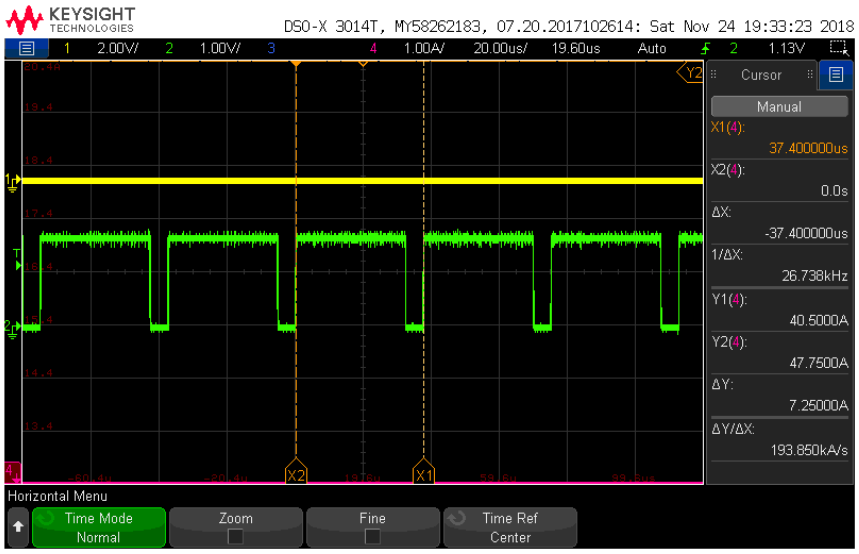
- Q1: What happens when the execution time is integral multiple of sample period (where a new ADCAINT1 to be generated) to cause a new and all following ADCAINT1s to be not serviced? Customer follows exactly what are required to do when exiting the ADCAINT1 like below but only adds a GPIO set when entering the ISR (DEBUG_LED_ON) and a GPIO clear when exiting the ISR (DEBUG_LED_OFF) to check if it's serviced or not and how long the execution time is.

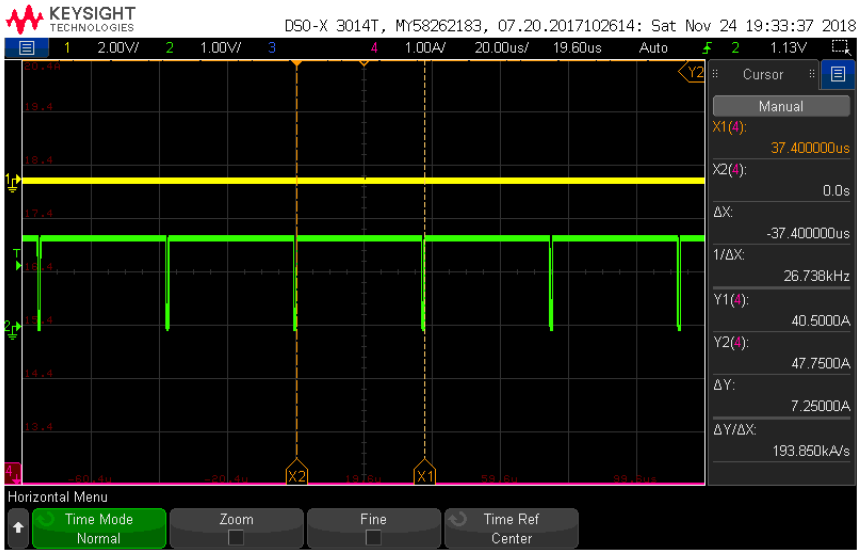
```
01102: #pragma CODE_SECTION(adcA1ISR, ".TI.ramfunc");
01103: __interrupt void adcA1ISR(void)
01104: {
01105:     static UINT16 ts_u16SampRecCnt = 0;
01106:     DEBUG_LED_ON;
01107:
01108:     App_IsrTaskAdCal();
01109:     App_IsrPowerDirCheck();
```

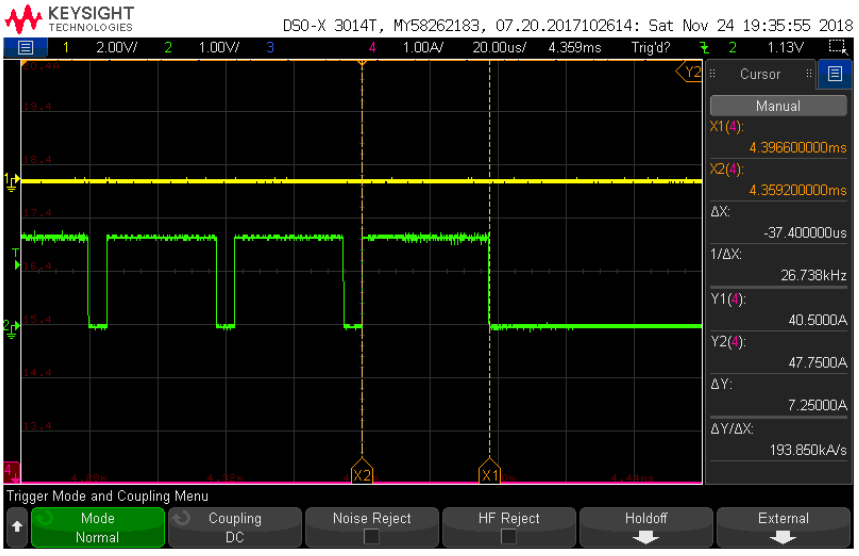
```
01167:     //
01168:     // Clear the interrupt flag and issue ACK
01169:     //
01170:     AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1;
01171:     PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
01172:     DEBUG_LED_OFF;
01173: } ? end adcA1ISR ?
01174:
```

- Q2: When the execution time is not integral multiple of sample period, e.g. 2.5x corresponding to 250% ISR utilization ratio, the ADCAINT1 can be serviced again although it's overflow (when 1x or 100% ISR utilization ratio it's not overflow) without clearing ADCINTOVF flag and enabling ADCINT to run in continuous mode, but it's not serviced right after the old ADCAINT1 exited, instead at the timing where is integral multiple of sample period (see captured waveforms below), why?

  Note:
  - Green (CH2) is GPIO controlled in ADCAINT1 ISR (high when entering and low when exiting);
  - Waveform #1 indicates execution time is >2x sample period and overflow occurs, while new ADCAINT1 can be serviced after old ISR exits, but is fixed to start running at the timing where is 3x sample period;
  - Waveform #2 indicates execution time is close to 3x sample period and overflow occurs, while new ADCAINT1 can be serviced after old ISR exits, but is fixed to start running at the timing where is 3x sample period;
  - Waveform #3 indicates execution time equals to 3x sample period and overflow occurs, while new ADCAINT1 and all following ADCAINT1s can't be serviced anymore;


KEYSIGHT TECHNOLOGIES
DSO-X 3014T, MY58262183, 07.20.2017102614: Sat Nov 24 19:33:23 2018
1 2.00V/ 2 1.00V/ 3 4 1.00A/ 20.00us/ 19.60us Auto 2 1.13V
Cursor
Manual
X1(4):
37.400000us
X2(4):
0.0s
ΔX:
-37.400000us
1/ΔX:
26.738kHz
Y1(4):
40.5000A
Y2(4):
47.7500A
ΔY:
7.25000A
ΔY/ΔX:
193.850kA/s
Horizontal Menu
Time Mode Normal
Zoom
Fine
Time Ref Center


KEYSIGHT TECHNOLOGIES
DSO-X 3014T, MY58262183, 07.20.2017102614: Sat Nov 24 19:33:37 2018
1 2.00V/ 2 1.00V/ 3 4 1.00A/ 20.00us/ 19.60us Auto 2 1.13V
Cursor
Manual
X1(4):
37.400000us
X2(4):
0.0s
ΔX:
-37.400000us
1/ΔX:
26.738kHz
Y1(4):
40.5000A
Y2(4):
47.7500A
ΔY:
7.25000A
ΔY/ΔX:
193.850kA/s
Horizontal Menu
Time Mode Normal
Zoom
Fine
Time Ref Center


KEYSIGHT TECHNOLOGIES
DSO-X 3014T, MY58262183, 07.20.2017102614: Sat Nov 24 19:35:55 2018
1 2.00V/ 2 1.00V/ 3 4 1.00A/ 20.00us/ 4.359ms Trig'd? 2 1.13V
Cursor
Manual
X1(4):
4.396600000ms
X2(4):
4.359200000ms
ΔX:
-37.400000us
1/ΔX:
26.738kHz
Y1(4):
40.5000A
Y2(4):
47.7500A
ΔY:
7.25000A
ΔY/ΔX:
193.850kA/s
Trigger Mode and Coupling Menu
Mode Normal
Coupling DC
Noise Reject
HF Reject
Holdoff
External