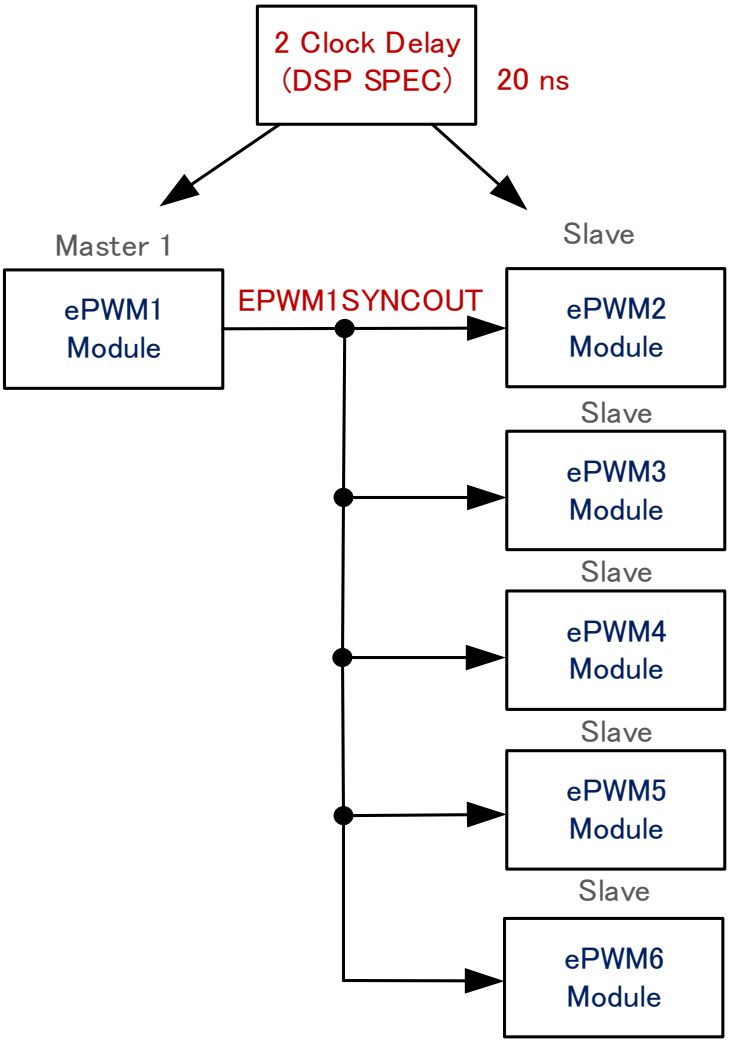
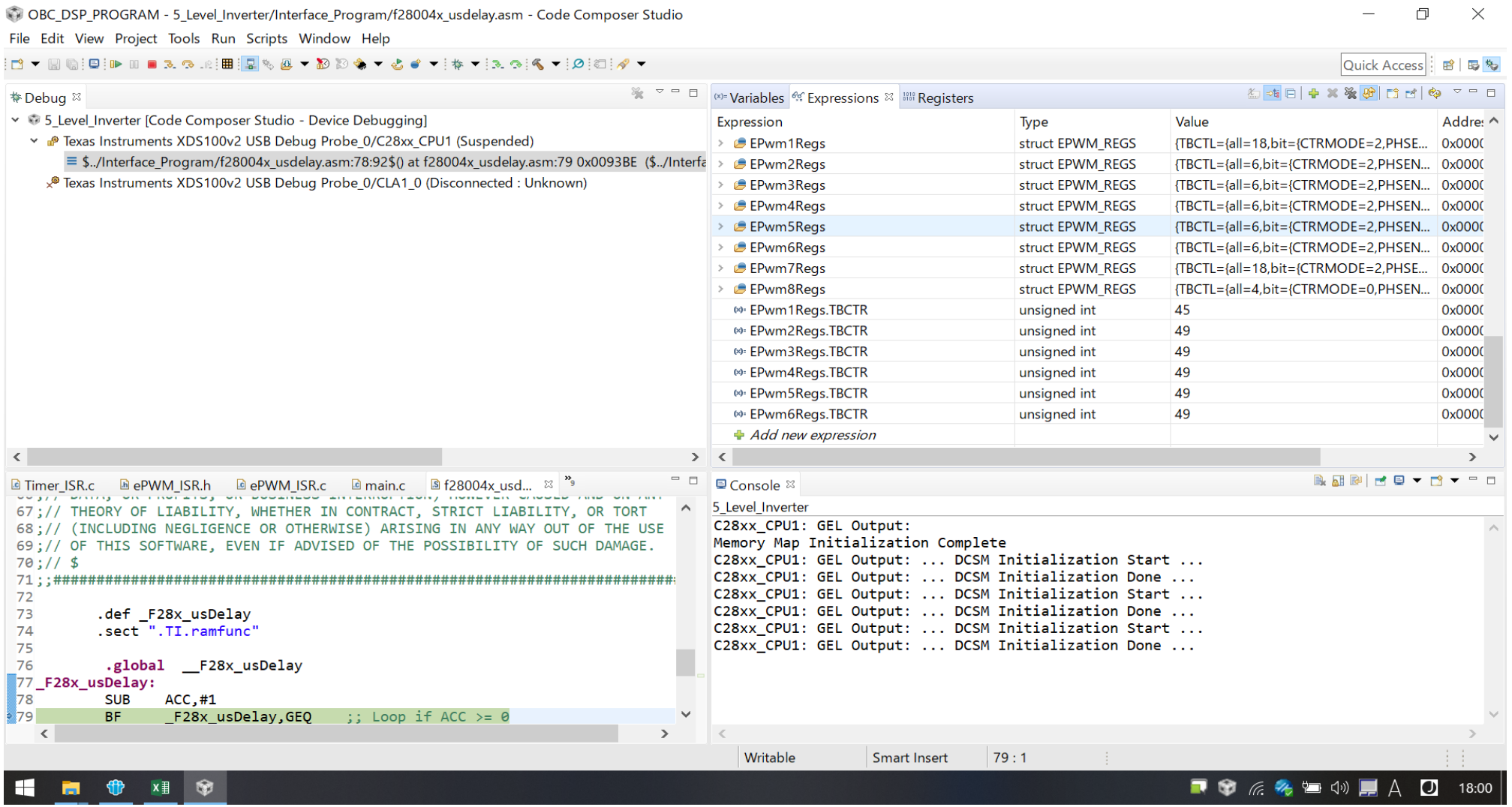

2 Clock Delay
(DSP SPEC)
20 ns
Master 1
ePWM1
Module
EPWM1SYNCOUT
Slave
ePWM2
Module
Slave
ePWM3
Module
Slave
ePWM4
Module
Slave
ePWM5
Module
Slave
ePWM6
Module

```
TMS320F280049_CLK_FREQUENCY = 100000000;
Fpwm = 100000;

EALLOW;
SyncSocRegs.SYNCSELECT.bit.SYNCOUT = 0;      // 0 -> EPWM1SYNCOUT selected
SyncSocRegs.SYNCSELECT.bit.EPWM1SYNCIN = 0;   // 0 -> EPWM1SYNCOUT selected
SyncSocRegs.SYNCSELECT.bit.EPWM4SYNCIN = 0;   // 0 -> EPWM1SYNCOUT selected
EDIS;

// EPWM1 Module Master Setup

EPwm1Regs.TBPRD = 0.5 * TMS320F280049_CLK_FREQUENCY / Fpwm;
EPwm1Regs.TBCTR = 0x0000;
EPwm1Regs.TBPHS.bit.TBPHS = 0;
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;
EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm1Regs.AQCTLB.bit.PRD = AQ_SET;
EPwm1Regs.AQCTLB.bit.CBD = AQ_CLEAR;
EPwm1Regs.DBCTL.bit.OUT_MODE = 0;
EPwm1Regs.DBCTL.bit.POLSEL = 0;
EPwm1Regs.DBCTL.bit.IN_MODE = 0;
EPwm1Regs.DBCTL.bit.SHDWDBFEDMODE = 1;
EPwm1Regs.DBCTL.bit.SHDWDBREDMODE = 1;
EPwm1Regs.DBCTL.bit.DEDB_MODE = 0;
EPwm1Regs.DBCTL.bit.HALFCYCLE = 0;
EPwm1Regs.DBCTL.bit.OUTSWAP = 0;
```

```
// EPWM2 Module Slave Setup

EPwm2Regs.TBPRD = 0.5 * TMS320F280049_CLK_FREQUENCY / Fpwm;
EPwm2Regs.TBCTR = 0x0000;
EPwm2Regs.TBPHS.bit.TBPHS = 2;
EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;
EPwm2Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;
EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;
EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
EPwm2Regs.AQCTLA.bit.ZRO = AQ_SET;
EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;
EPwm2Regs.AQCTLB.bit.PRD = AQ_SET;
EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;
EPwm2Regs.DBCTL.bit.OUT_MODE = 0;
EPwm2Regs.DBCTL.bit.POLSEL = 0;
EPwm2Regs.DBCTL.bit.IN_MODE = 0;
EPwm2Regs.DBCTL.bit.SHDWDBFEDMODE = 1;
EPwm2Regs.DBCTL.bit.SHDWDBREDMODE = 1;
EPwm2Regs.DBCTL.bit.DEDB_MODE = 0;
EPwm2Regs.DBCTL.bit.HALFCYCLE = 0;
EPwm2Regs.DBCTL.bit.OUTSWAP = 0;
```



There confirmed 4 counts different between Master and Slaves.