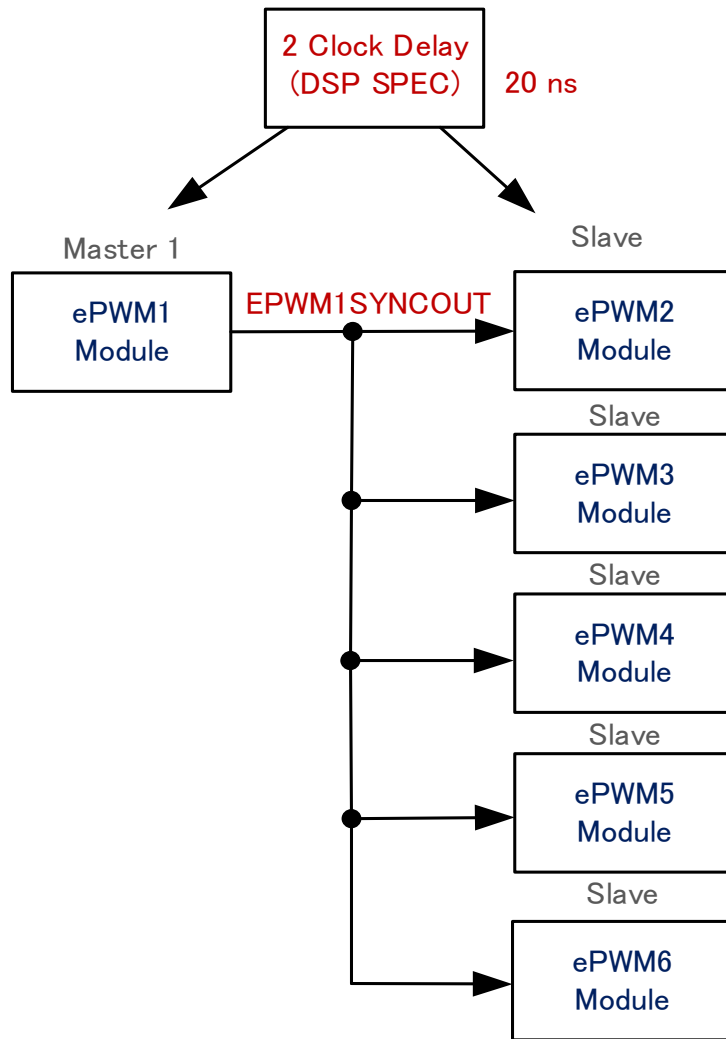




```
TMS320F280049_CLK_FREQUENCY = 100000000;  
Fpwm = 100000;
```

```
EALLOW;
```

```
SyncSocRegs.SYNCSELECT.bit.SYNCOUT = 0;    // 0 -> EPWM1SYNCOUT selected  
SyncSocRegs.SYNCSELECT.bit.EPWM1SYNCIN = 0; // 0 -> EPWM1SYNCOUT selected  
SyncSocRegs.SYNCSELECT.bit.EPWM4SYNCIN = 0; // 0 -> EPWM1SYNCOUT selected  
EDIS;
```

```
// EPWM1 Module Master Setup
```

```
EPwm1Regs.TBPRD = 0.5 * TMS320F280049_CLK_FREQUENCY / Fpwm;  
EPwm1Regs.TBCTR = 0x0000;  
EPwm1Regs.TBPHS.bit.TBPHS = 0;  
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;  
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;  
EPwm1Regs.TBCTL.bit.PRDLT = TB_SHADOW;  
EPwm1Regs.TBCTL.bit.SYNCSEL = TB_CTR_ZERO;  
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;  
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV1;  
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;  
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;  
EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;  
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;  
EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET;  
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;  
EPwm1Regs.AQCTLB.bit.PRDLT = AQ_SET;  
EPwm1Regs.AQCTLB.bit.CBD = AQ_CLEAR;  
EPwm1Regs.DBCTL.bit.OUT_MODE = 0;  
EPwm1Regs.DBCTL.bit.POLSEL = 0;  
EPwm1Regs.DBCTL.bit.IN_MODE = 0;  
EPwm1Regs.DBCTL.bit.SHDWDBFEDMODE = 1;  
EPwm1Regs.DBCTL.bit.SHDWDBREDDMODE = 1;  
EPwm1Regs.DBCTL.bit.DEDB_MODE = 0;  
EPwm1Regs.DBCTL.bit.HALFCYCLE = 0;  
EPwm1Regs.DBCTL.bit.OUTSWAP = 0;
```

```
// EPWM2 Module Slave Setup
```

```
EPwm2Regs.TBPRD = 0.5 * TMS320F280049_CLK_FREQUENCY / Fpwm;  
EPwm2Regs.TBCTR = 0x0000;  
EPwm2Regs.TBPHS.bit.TBPHS = 2;  
EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;  
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE;  
EPwm2Regs.TBCTL.bit.PRDLT = TB_SHADOW;  
EPwm2Regs.TBCTL.bit.SYNCSEL = TB_SYNC_IN;  
EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;  
EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;  
EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;  
EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;  
EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;  
EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;  
EPwm2Regs.AQCTLA.bit.ZRO = AQ_SET;  
EPwm2Regs.AQCTLA.bit.CAU = AQ_CLEAR;  
EPwm2Regs.AQCTLB.bit.PRDLT = AQ_SET;  
EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;  
EPwm2Regs.DBCTL.bit.OUT_MODE = 0;  
EPwm2Regs.DBCTL.bit.POLSEL = 0;  
EPwm2Regs.DBCTL.bit.IN_MODE = 0;  
EPwm2Regs.DBCTL.bit.SHDWDBFEDMODE = 1;  
EPwm2Regs.DBCTL.bit.SHDWDBREDMODE = 1;  
EPwm2Regs.DBCTL.bit.DEDB_MODE = 0;  
EPwm2Regs.DBCTL.bit.HALFCYCLE = 0;  
EPwm2Regs.DBCTL.bit.OUTSWAP = 0;
```

OBC\_DSP\_PROGRAM - 5\_Level\_Inverter/Interface\_Program/f28004x\_usdelay.asm - Code Composer Studio

File Edit View Project Tools Run Scripts Window Help

Quick Access

Debug

5\_Level\_Inverter [Code Composer Studio - Device Debugging]

Texas Instruments XDS100v2 USB Debug Probe\_0/C28xx\_CPU1 (Suspended)

\$/Interface\_Program/f28004x\_usdelay.asm:78:92\$() at f28004x\_usdelay.asm:79 0x0093BE (\$/Interf

Texas Instruments XDS100v2 USB Debug Probe\_0/CLA1\_0 (Disconnected : Unknown)

Variables Expressions Registers

| Expression         | Type             | Value                                 | Address |
|--------------------|------------------|---------------------------------------|---------|
| > EPwm1Regs        | struct EPWM_REGS | {TBCTL={all=18,bit={CTRMODE=2,PHSE... | 0x0000  |
| > EPwm2Regs        | struct EPWM_REGS | {TBCTL={all=6,bit={CTRMODE=2,PHSEN... | 0x0000  |
| > EPwm3Regs        | struct EPWM_REGS | {TBCTL={all=6,bit={CTRMODE=2,PHSEN... | 0x0000  |
| > EPwm4Regs        | struct EPWM_REGS | {TBCTL={all=6,bit={CTRMODE=2,PHSEN... | 0x0000  |
| > EPwm5Regs        | struct EPWM_REGS | {TBCTL={all=6,bit={CTRMODE=2,PHSEN... | 0x0000  |
| > EPwm6Regs        | struct EPWM_REGS | {TBCTL={all=6,bit={CTRMODE=2,PHSEN... | 0x0000  |
| > EPwm7Regs        | struct EPWM_REGS | {TBCTL={all=18,bit={CTRMODE=2,PHSE... | 0x0000  |
| > EPwm8Regs        | struct EPWM_REGS | {TBCTL={all=4,bit={CTRMODE=0,PHSEN... | 0x0000  |
| EPwm1Regs.TBCTR    | unsigned int     | 45                                    | 0x0000  |
| EPwm2Regs.TBCTR    | unsigned int     | 49                                    | 0x0000  |
| EPwm3Regs.TBCTR    | unsigned int     | 49                                    | 0x0000  |
| EPwm4Regs.TBCTR    | unsigned int     | 49                                    | 0x0000  |
| EPwm5Regs.TBCTR    | unsigned int     | 49                                    | 0x0000  |
| EPwm6Regs.TBCTR    | unsigned int     | 49                                    | 0x0000  |
| Add new expression |                  |                                       |         |

Timer\_ISR.c ePWM\_ISR.h ePWM\_ISR.c main.c f28004x\_usd...

```

67; // THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT
68; // (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE
69; // OF THIS SOFTWARE, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.
70; // $
71; ; #####
72
73     .def _F28x_usDelay
74     .sect ".TI.ramfunc"
75
76     .global __F28x_usDelay
77 _F28x_usDelay:
78     SUB     ACC,#1
79     BF     _F28x_usDelay,GEQ    ;; Loop if ACC >= 0

```

Console

5\_Level\_Inverter

C28xx\_CPU1: GEL Output: Memory Map Initialization Complete

C28xx\_CPU1: GEL Output: ... DCSM Initialization Start ...

C28xx\_CPU1: GEL Output: ... DCSM Initialization Done ...

C28xx\_CPU1: GEL Output: ... DCSM Initialization Start ...

C28xx\_CPU1: GEL Output: ... DCSM Initialization Done ...

C28xx\_CPU1: GEL Output: ... DCSM Initialization Start ...

C28xx\_CPU1: GEL Output: ... DCSM Initialization Done ...

Writable Smart Insert 79 : 1

18:00

There confirmed 4 counts different between Master and Slaves.