F28377D General Control Board v1.1: Hardware Description

Version 1.0

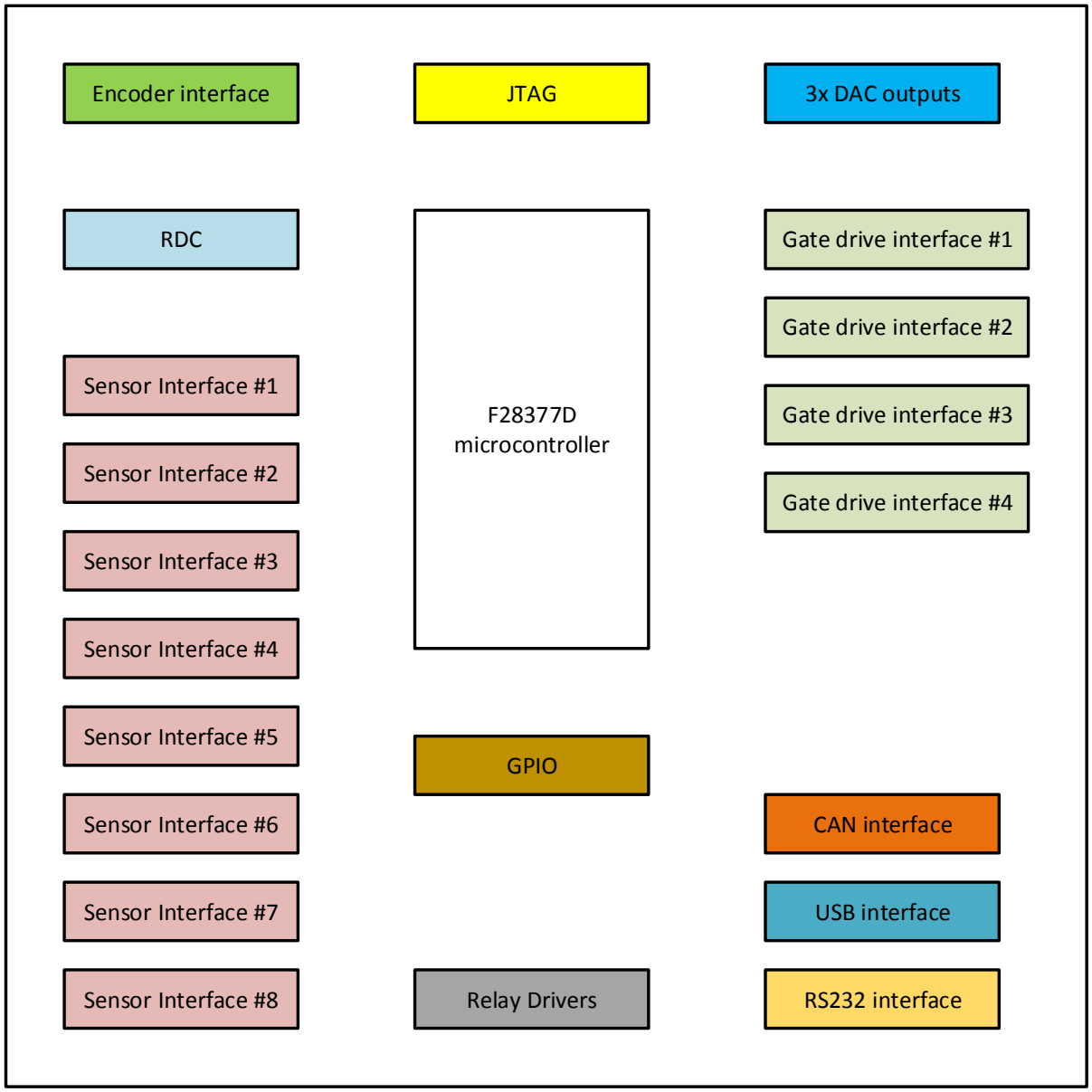

Fig.1: Sub-circuits for GCB

This note should be read in conjunction with the circuit schematic diagram (F28377D General Control Board v1_1.pdf)

For convenience with a multi-sheet schematic, the F28377D is represented with multiple blocks.

Sheet 2: CPU – GPIO

Uncommitted GPIO pins are brought out to connectors J1 and J2 for unspecified digital interfacing purposes. Two LEDs D3 and D4 driven by GPIO31 and GPIO34 via an open-drain buffer U2 (74LVC2G07) are available which can be used to indicate aspects of processor operation. Two

MOSFETs Q1 and Q2 can be used to drive external relays via connector J3. The diodes D1 and D2 protect the MOSFETs from inductive transients due to the relay coil inductance.

Sheet 3: CPU – JTAG, POWER

The JTAG interface is brought out to J4 for connection to a host computer via an external XDS100v2 JTAG emulator. The crystal X1 provides the basic processor clock timing and has a separate isolated ground VSSOSC. The processor reset pin XRS/ is connected to the reset input on the resolver interface U18 (Sheet 9). This results in the resolver interface being reset whenever there is an F28377D reset. The F28377D chip decoupling is also shown on this sheet.

Sheet 4: CPU – ADC

The F28377D has 4 ADC modules and each one has a separate voltage reference input (VREFHIA-VREFHID). The reference voltage of 3V is provided by a precision reference circuit U4 (REF3030). The reference voltage is supplied via quad op-amp connected as 4 voltage followers (U3A-U3D). Each voltage follower has a 2.2uF capacitor connected across its output for noise suppression. The F28377D has 3 DAC output signals which are brought out to J5. A spare analogue input (ADCINA5) is also made available on J5. Clamp diodes (U5) are connected to each signal which in conjunction with resistors (R26-29) prevent the signals exceeding the safe voltage range.

Sheet 5: POWER

The board requires +5V, +15V and -15V power which is brought in on J7. These voltage supplies are then routed through common-mode chokes L2, L4 and L7 which reduce noise from external sources transferring into the sensitive on-board circuits. DC-DC converter U6 is used to produce 3V3 and 1V2 supply voltages. The 1V2 supply is only used by the F28377D. Further supply voltage filtering is provided by the circuits including L5, L6, L8 and L9. LEDs D5, D6 and D7 provide supply health indication. Link blocks J6, J8 and J9 are included to allow supplies to be disconnected for hardware fault finding purposes. The links can also be used to monitor individual supply currents.

Sheet 6: MOSFET DRIVERS

The board makes use of 4 pairs of F28377D PWM outputs. These signals are buffered with high current drivers (SN75372) U7, U8, U9 and U10 to provide a low impedance drive to external gate drive circuits. The high-current drivers also boost the PWM signal amplitude from 3V3 to 15V for improved noise immunity and compatibility with many commercial gate drives. The amplified PWM signals are then routed to ribbon cable header J10. The connector also has two pins routed to GPIO pins which could be used for gate drive fault indication or protection reset.

Sheet 7: RS232, ISOLATED USB

There are two serial interfaces described on this sheet. They make use of the Serial Communication Interfaces SCI-B and SCI-C on the F28377D. SCI-C connects to a transceiver U11 (MAX3221) to provide a non-isolated RS232 interface on connector J11. SCI-B connects to a signal isolator U12 (IL712-3E) which in turn connects to a UART to USB interface U13 (FT230XS). U13 is then connected to mini USB connector J12. The serial interfaces can be used for communication with a host PC and a GUI. Data transfer activity can be observed with LEDs D8 and D9.

Sheet 8: ENCODER, CAN BUS

Many incremental optical encoders use RS-422 differential line type output signals. The encoder interface therefore includes a compatible differential line receiver U14 (AM26LV32CD). The encoder is connected to J13 which includes a 5V supply to energise the electronics within the encoder device. The output signals from U14 are routed to the EQEP-A quadrature encoder interface on the F28377D.

This sheet also shows two CAN-bus interfaces which are routed to the CAN pins on the F28377D. Each interface comprises a CAN transceiver (SN65HVD235) U15 and U16 which connects to J14 and J15 respectively.

Sheet 9: RESOLVER

The resolver interface is based on the AD2S1210 RDC device U18 which is configured for communication with the F28377D via its SPI-A interface. There are also some other digital input signals driven from F28377D GPIO signals. The differential excitation outputs for the resolver rotor winding are provided by two high-current op-amps U17 (AD8397). The resolver is connected via J16.

The sine and cosine input circuitry includes a differential-mode filter, common-mode filter and a transient suppressor U20 (NUP4201MR6). If the input filters are required then the choice of cut-off frequency will need to take into account the impact of phase shift on resolver accuracy. The default component selection does not include any input filtering. In order to achieve the specified accuracy, it is important that the resolver sine and cosine input signals do not exceed the input range of the AD2S1210. To cater for different resolver turns ratios, R78 is selected to set the input attenuation level. As mentioned earlier, the AD2S1210 reset input is connected to the F28377D reset pin which ensures a AD2S1210 reset whenever there is a an F28377D reset.

As detailed in the AD2S1210 data-sheet, there are two modes of operation determined by the inputs A0 and A1. These signals are driven by software via the F28377D GPIO. Similarly, the inputs SAMPLE/, RES0 and RES1 are driven by GPIO.

Sheet 10: ANALOGUE INPUT (1 & 2)

A flexible sensor interface is included to allow connection of a variety of current and voltage sensors to the microcontroller ADC inputs. This board has 8 sensor inputs which are connected via J17 and J18. Power for sensors is available at J19 which includes +5V, +15V and -15V supplies.

To prevent potential ground loops and consequent noise it is desireable that these supplies are used instead of an external power source. All sensor supplies have local decoupling capacitors. Some sensors require a load resistor to convert a current output to a voltage. A load resistor network is provided for this. A capacitor in parallel with the load resistor can also be fitted to provide low pass filtering.

The voltage from the load resistor is then routed to a TL084 op-amp U21. The op-amp is configured as a non-inverting amplifier. The TL084 provides a gain option for sensors with low voltage outputs. The amplifier output is routed to a potential divider and offset shift circuit. The offset shift circuit is used to convert a bipolar signal range to a unipolar range compatible with the 0-3V ADC input range.

For greater dc stability the offset shift circuit uses a 2.5V precision reference source U23 (REF3025). The REF3025 has a max current of 25mA. Care must be taken when choosing the potential divider resistors that the REF3025 is not overloaded. A capacitor is included at the output of the potential divider to provide low pass filtering. The ADC input is protected from over or under voltage by Schottky clamp diodes U22. Some sensors produce a unipolar signal range. If this type of sensor is used then the resistors connecting to the 2.5V reference can be omitted.

When interfacing to many sensors, the op-amp may not be needed. If this is the case then the TL084 can be omitted. By appropriate use of the feedback resistor network, a direct through connection can be made to the ADC input. A resistor is included between the op-amp inputs. This resistor would not be fitted when the op-amp is used. If the TL084 is omitted then this resistor provides a path through and forms part of the attenuator circuit. As the TL084 package contains 4 op-amps this requires that 4 sensor channels would all need to have this configuration.

Sheets 11 to 13 contain sensor interface circuitry similar to that described for sheet 10.