

NOTES:**1) USB Differential Pairs - 90 Ohm**

- (A) USB-DM & USB-DP
- (B) USB0_GPIO-42 & USB0_GPIO-43
- (C) MCU_GPIO-42 & MCU_GPIO-43

2) EMIF - External Memory Interface Impedance Matching from J1 to U1

- (A) MCU_GPIO-39:41, MCU_GPIO-44:52, MCU_GPIO-86:94 - Address [0:21]
- (B) MCU_GPIO-85, MCU_GPIO-83:53 - Data [0:31]
- (C) MCU_GPIO-30 - Clock
- (D) MCU_GPIO-37, 31, 29 - Read/Write/ClkEn Pins
- (E) MCU_GPIO-32, 34, 35, 28 - Chip Select Pins

3) ADC Differential Pair Impedance Matching

- (A) HSEC_ADC even pins should match with HSEC_ADC + 1 pin (ie HSEC_ADC-C2 should match with HSEC_ADC-C3)
- (B) MCU_ADC even pins should match with MCU_ADC + 1 pin (ie MCU_ADC-A0 should match with MCU_ADC-A1)

REVISION RECORD

WHO:	SCH REV:	PCB REV:	NOTES:	DATE:
TI-BL	R1.0	R1.0	Draft	05-Jun-2013
TI-BL	R1.1	R1.1	Edited SVS circuitry (U3,U4); Changed power supply (U14) resistors Changed F28377D (U1) pinout and connector pinout (J1) Changed ADC VREFHI circuitry (U17,U13) and switches (SW3, SW4)	24-Oct-2013
TI-BL	R1.1 ASSY A	R1.1 R1.2	R16: 2K2 to 0R, R72: 0R0 to 100K, R74: 0R0 to 10K X1: Move to crystal with lower ESR U1: Swap VREFLOB and VREFLOD to match datasheet U1: Rename ADCINCALO & CAL1 to ADCIN14 & 15 Net Rename: HSEC_ADC-CALO & CAL1 to HSEC_ADCIN14 & 15 Net Rename: MCU_ADC-CALO & CAL1 to MCU_ADCIN14 & 15	09-May-2014
TI-BL	R1.3	R1.3	Shrank the xds100 circuitry (the F28377D has no EMU0/EMU1) Added an external connector Changed USB circuitry: - Better/safer interface to USB-VBUS - Added TPD4S012 ESD protection diodes - Added a resistor which, when removed, reduces the bus capacitance below the USB spec Changed ADC diodes to TPD4E001 Changed voltage supervision circuitry Added a schottky diode between VDD_1V2 and VDD_3V3 to help ensure that VDD_3V3 is > VDD_1V2 Changed ADC voltage reference circuitry Reannotation of resistors and capacitors	17-Sept-2015

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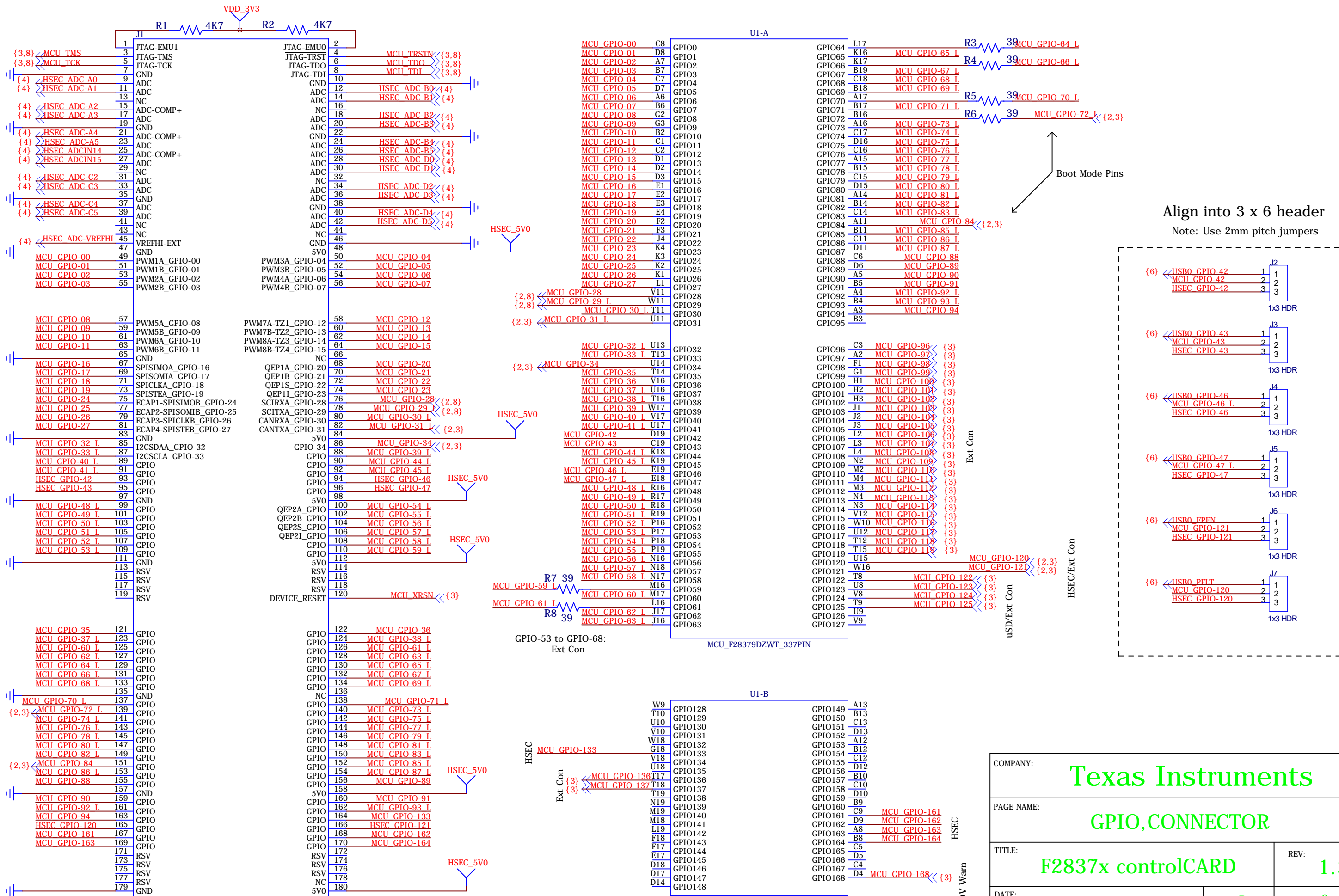
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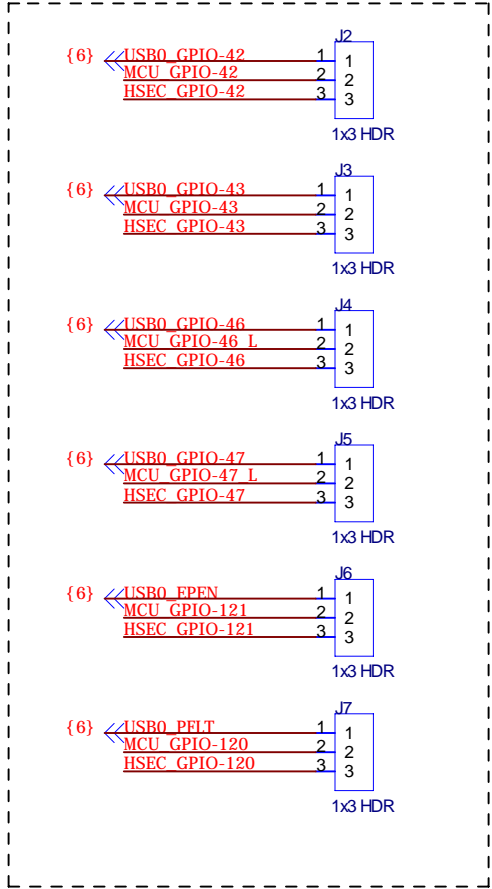
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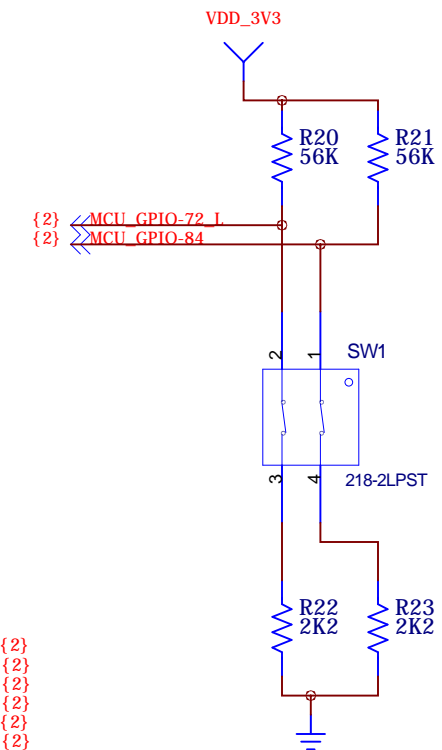
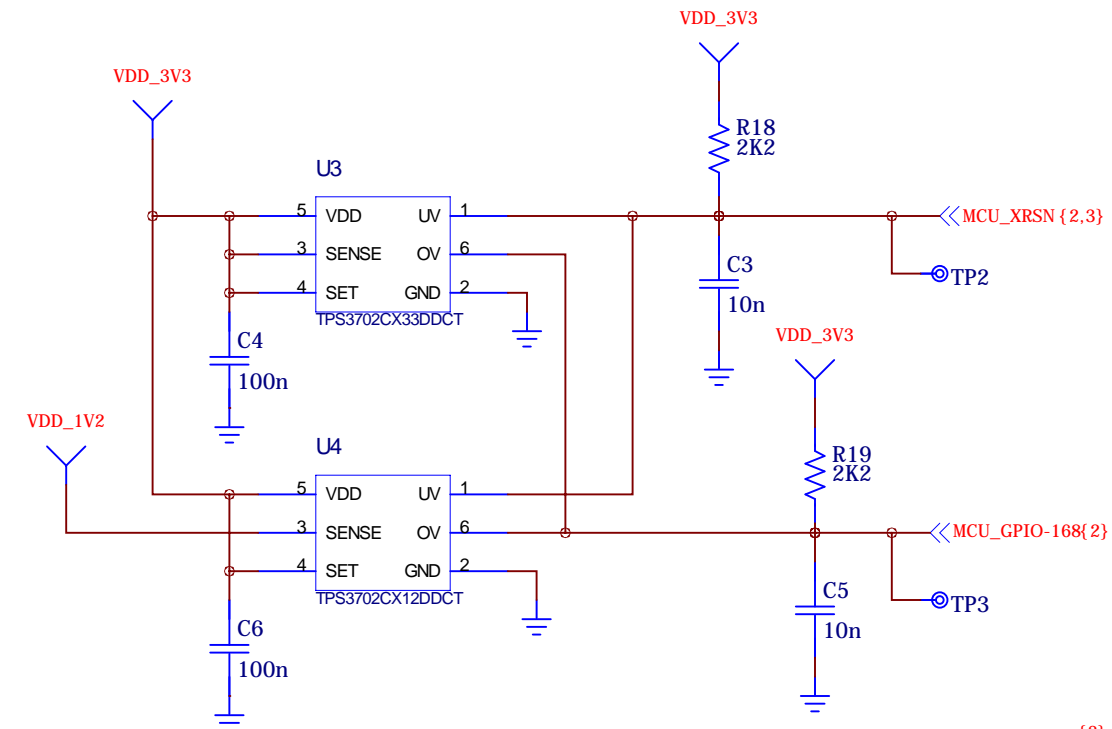
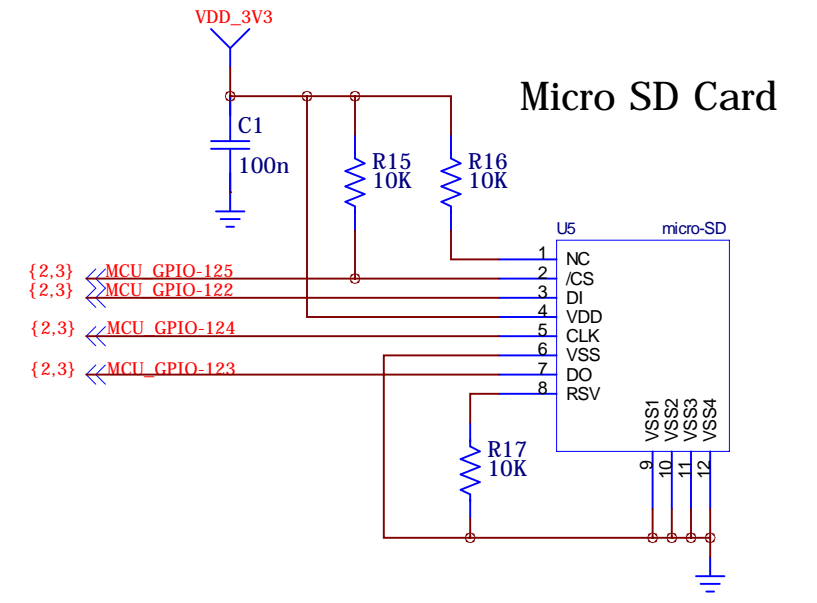
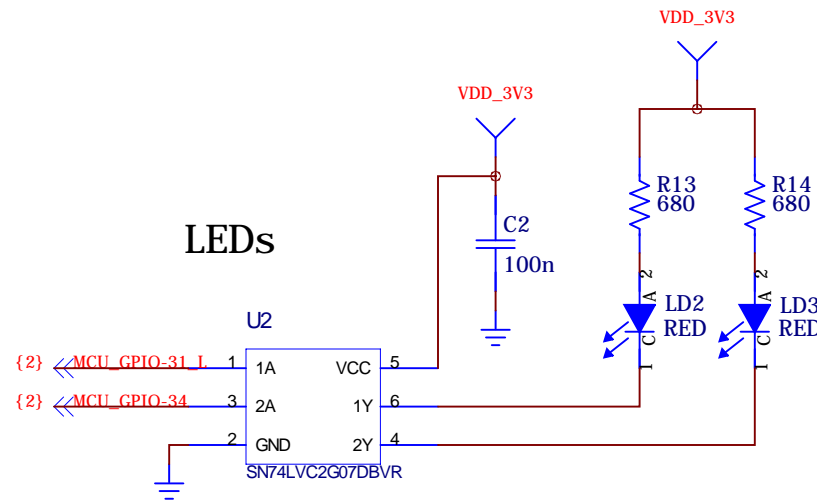
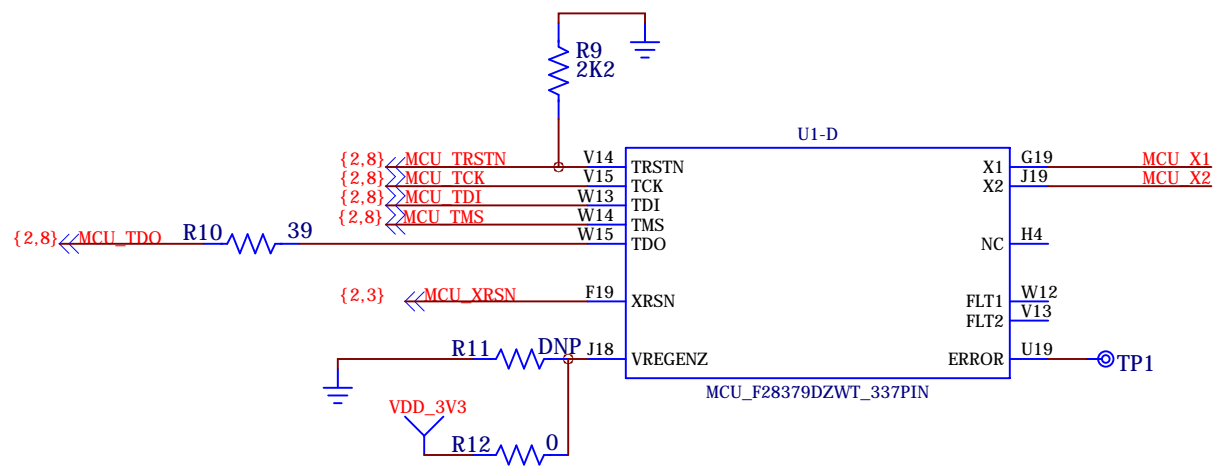


Align into 3 x 6 header

Note: Use 2mm pitch jumpers

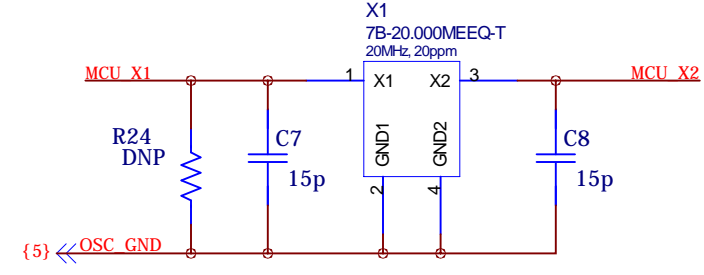


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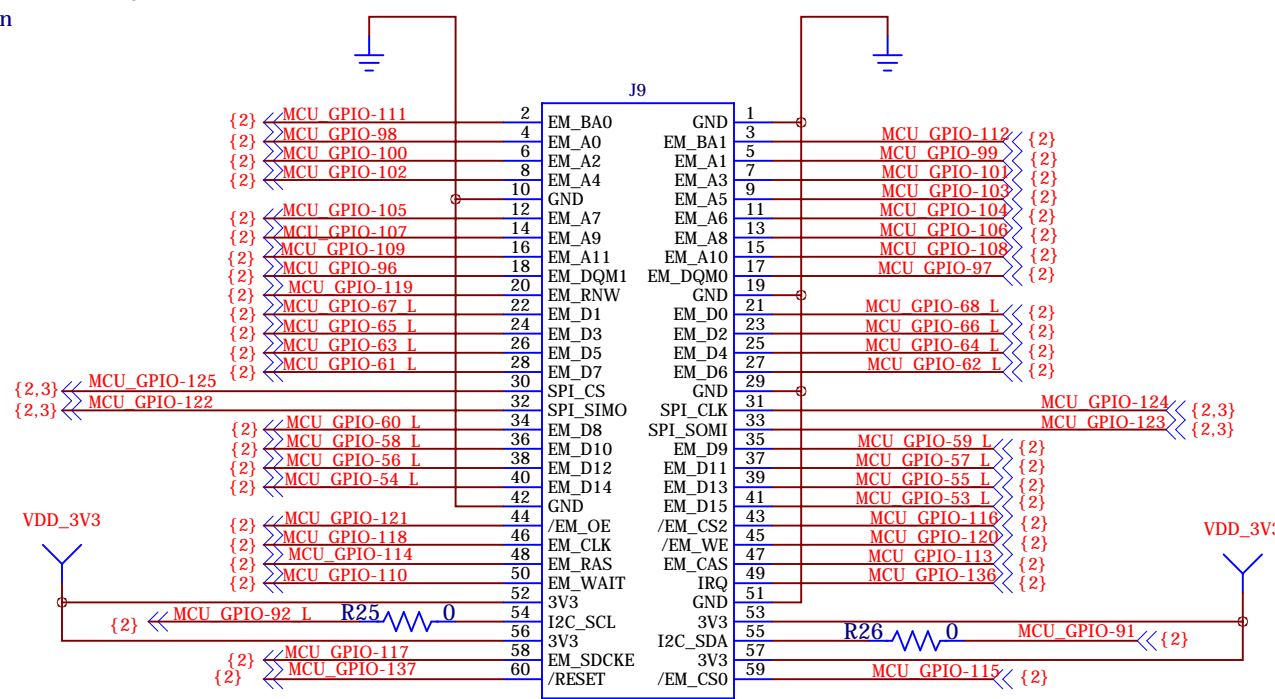


*SW1 placed upside-down (so UP is open (1), DOWN is closed (0))

F2837x Clock



External Connector Option



Selected Boot Mode Chart

(see datasheet for other boot modes and more information)

Mode #	GPIO72	GPIO84	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI
02	1	0	Wait Boot Mode
03	1	1	Get Mode (Flash by default)

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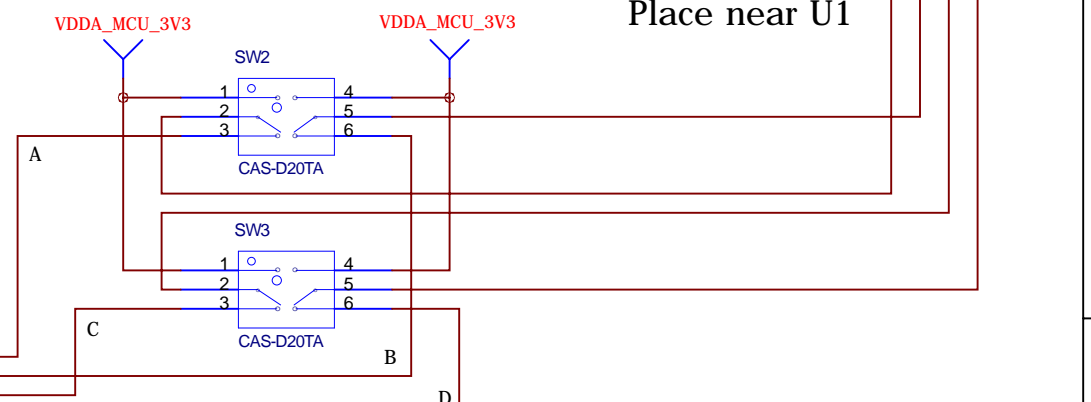
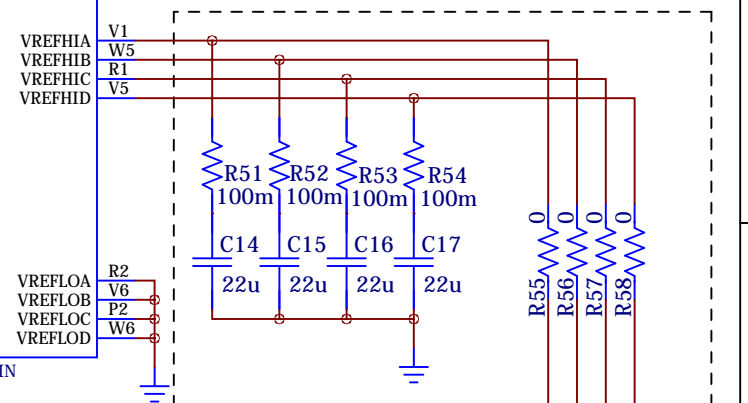
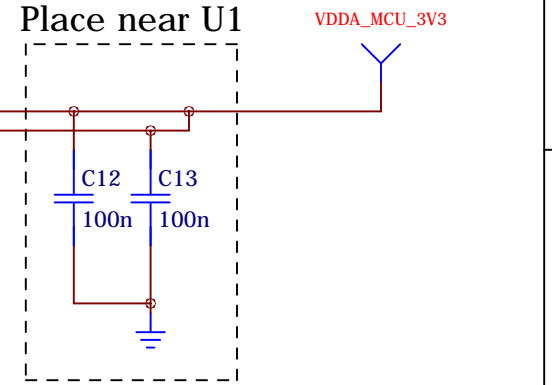
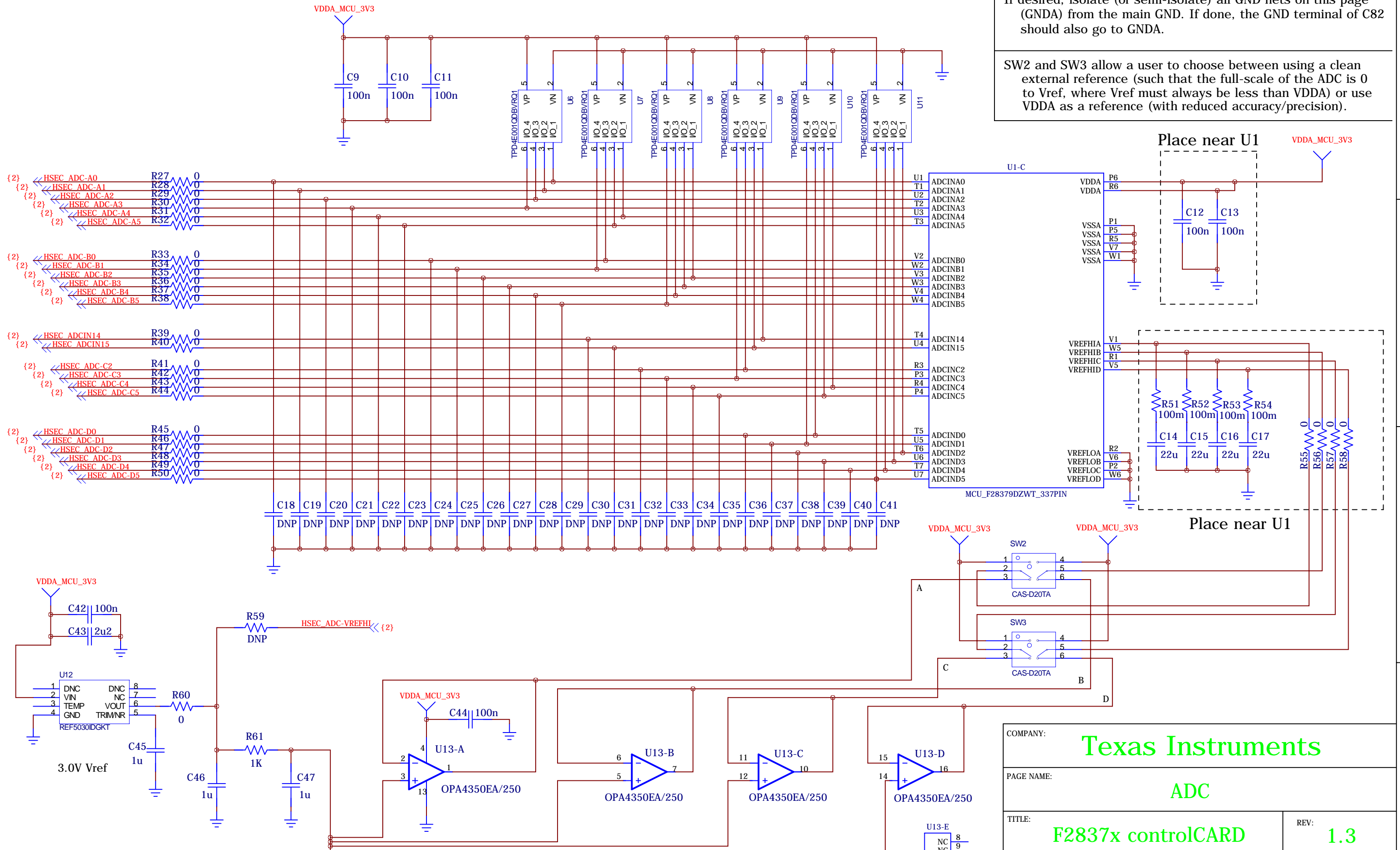
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If desired, isolate (or semi-isolate) all GND nets on this page (GNDA) from the main GND. If done, the GND terminal of C82 should also go to GNDA.

SW2 and SW3 allow a user to choose between using a clean external reference (such that the full-scale of the ADC is 0 to Vref, where Vref must always be less than VDDA) or use VDDA as a reference (with reduced accuracy/precision).



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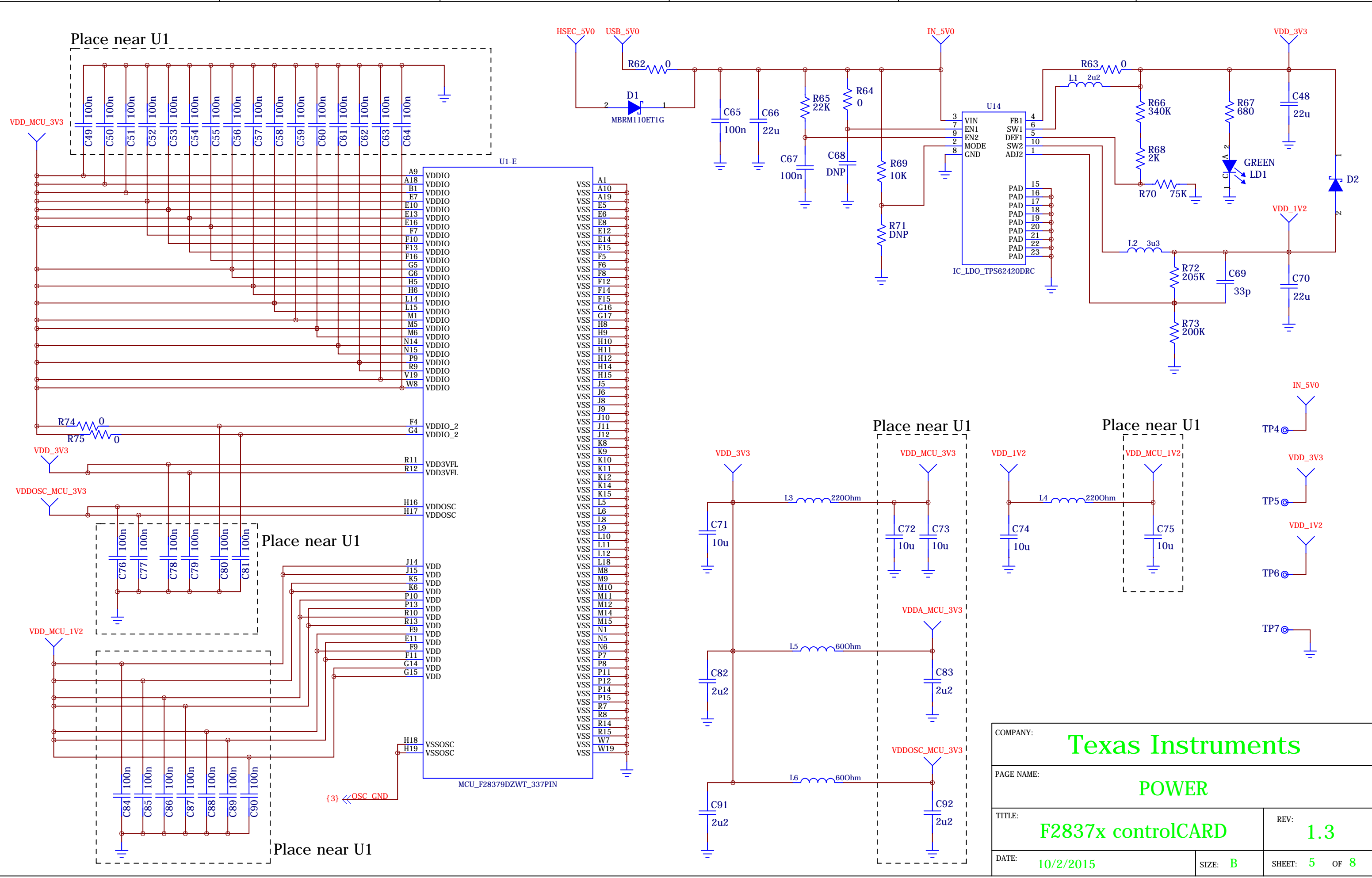
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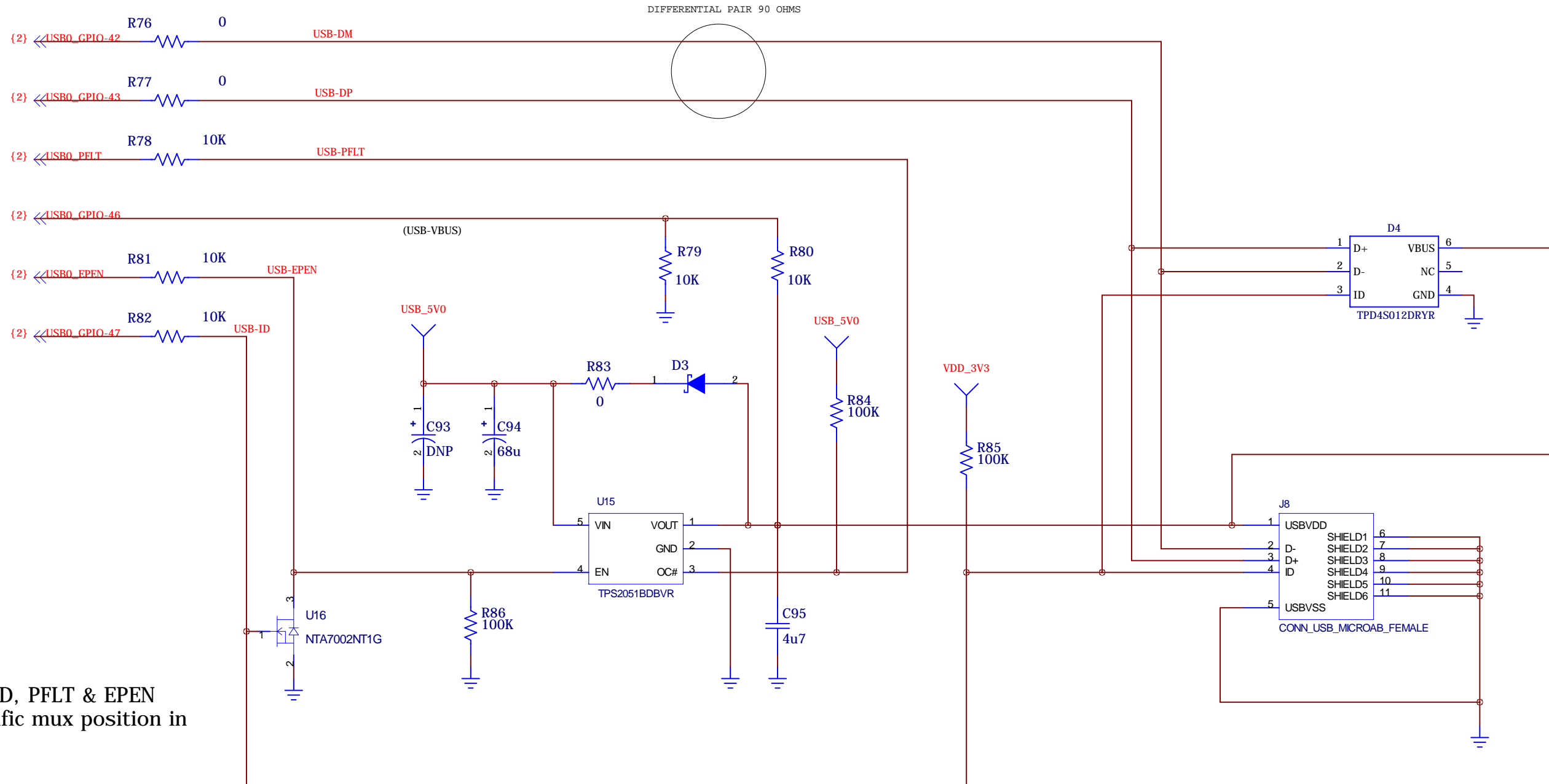
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NOTE: USB VBUS, ID, PFLT & EPEN do not have a specific mux position in this device.

In this controlCARD, a standard GPIO is used to detect changes to these signals.

R83 is populated to allow a customer to evaluate the controlCARD without a baseboard if they desire. USB specifies the total bus capacitance on any device as 10uF max. R83 should be depopulated in most end applications.

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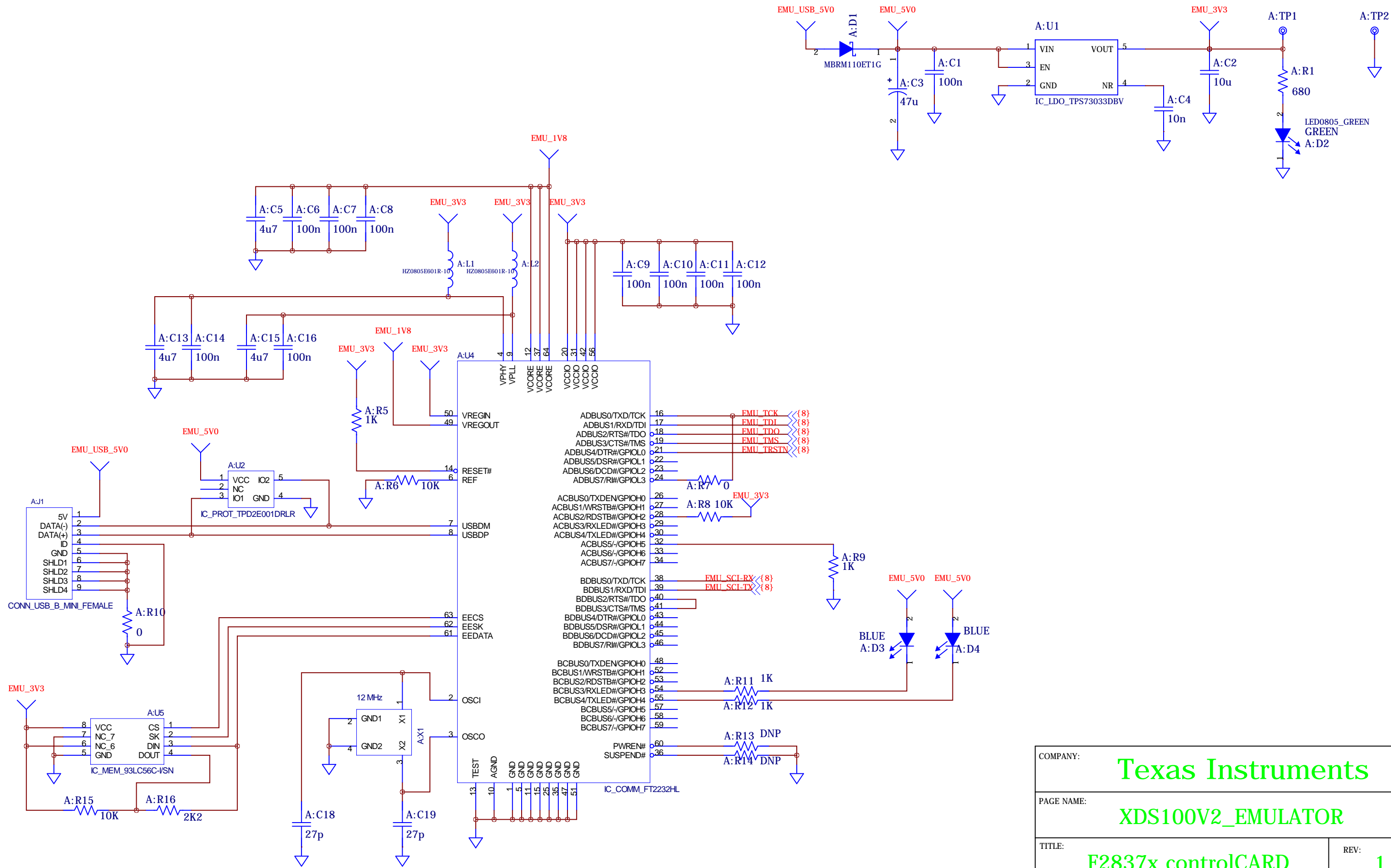
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COMPANY:		Texas Instruments	
PAGE NAME:		XDS100V2_EMULATOR	
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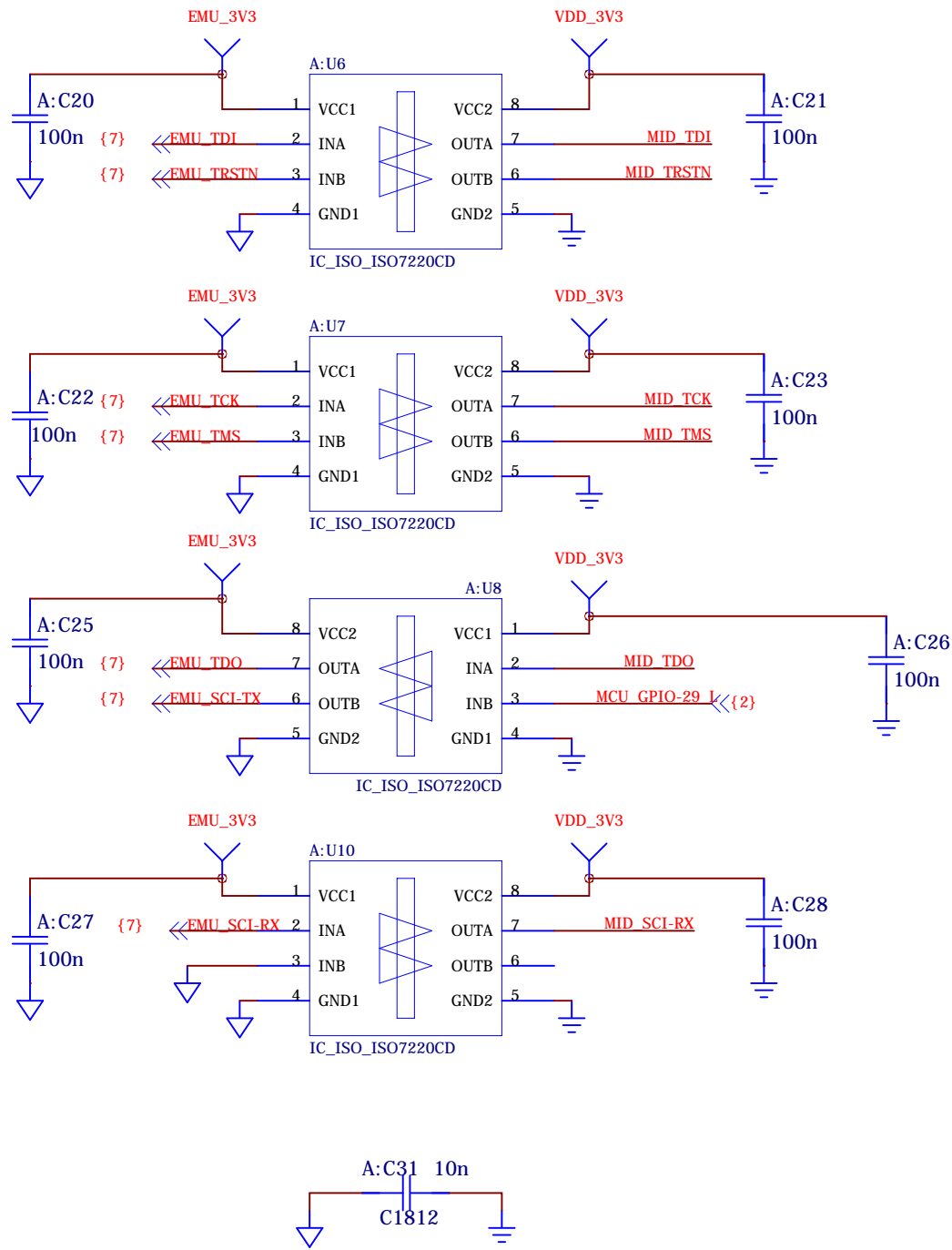
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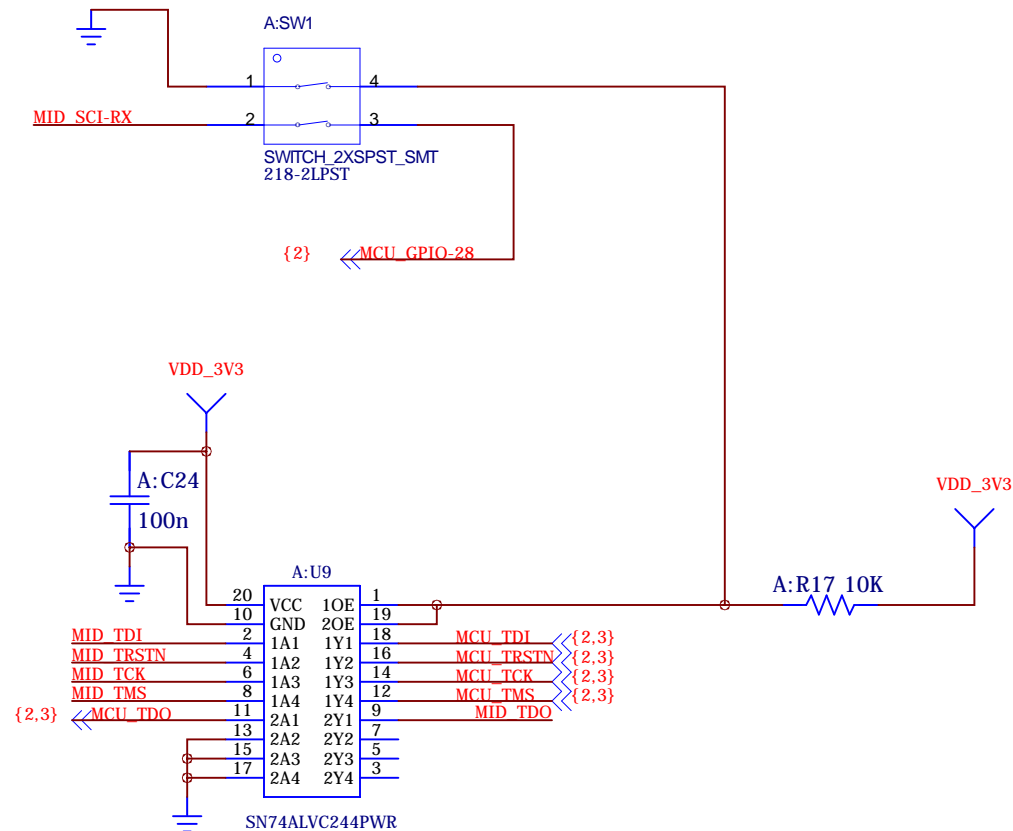
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A



A:SW1 - Emulation & GPIO28 Switch

- Pos 1 ON: Use xds100v2 emulator that is on the cCARD
- Pos 1 OFF: Boot from FLASH/peripheral (see boot mode switch) OR use emulator on baseboard
- Pos 2 ON: GPIO28 will be controlled by the USB-to-UART adapter on the FTDI chip
- Pos 2 OFF: GPIO-28 can be controlled by a pin in HSEC connector



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