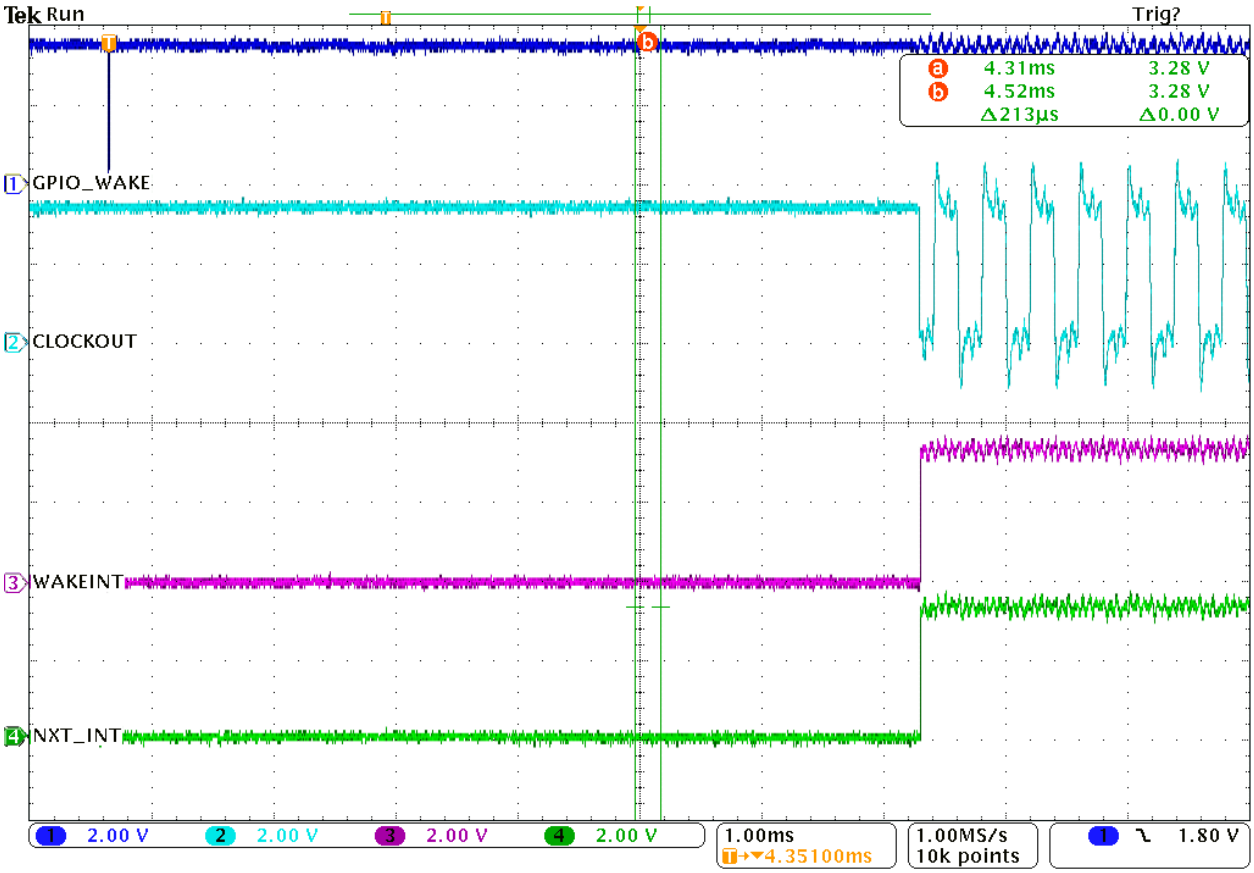
HALT mode wakeup behavior

Case	PIEIER1.8	IER	INTM	Observation
0	0	0	0 (EINT)	Neither the WAKEINT_ISR, nor the instruction following IDLE is executed. CLKOUT appears (after the PLL lock time), but code is just stuck at IDLE. Single-stepping/free-running does not increment the PC. SYSCLKOUT after wakeup = 100 MHz.
1	0	0	1 (DINT)	
2	0	1	0 (EINT)	
3	0	1	1 (DINT)	
4	1	0	0 (EINT)	
5	1	0	1 (DINT)	
6	1	1	0 (EINT)	Upon wakeup, WAKEINT_ISR is executed first, followed by the instruction after IDLE. (tek002.bmp)
7	1	1	1 (DINT)	WAKEINT_ISR is not executed. The instruction following IDLE is executed. (tek001.bmp)

Conclusions:

1. If PIEIER1.8 = 0, device does not exit HALT mode properly.
2. For device to exit HALT mode properly, the following conditions should be met:
   PIEIER1.8 = 1
   IER = 0x0001
3. If the above conditions are met,
   (i) WAKE_INT ISR will be executed first, followed by the instruction(s) after IDLE, if INTM = 0.
   (ii) WAKE_INT ISR will not be executed and instruction(s) after IDLE will be executed, if INTM = 1.

Case 6:



PIEIER1.8 = 1, IER = 0x0001, INTM = 0. WAKE_INT ISR is executed first, followed by the instruction(s) after IDLE.

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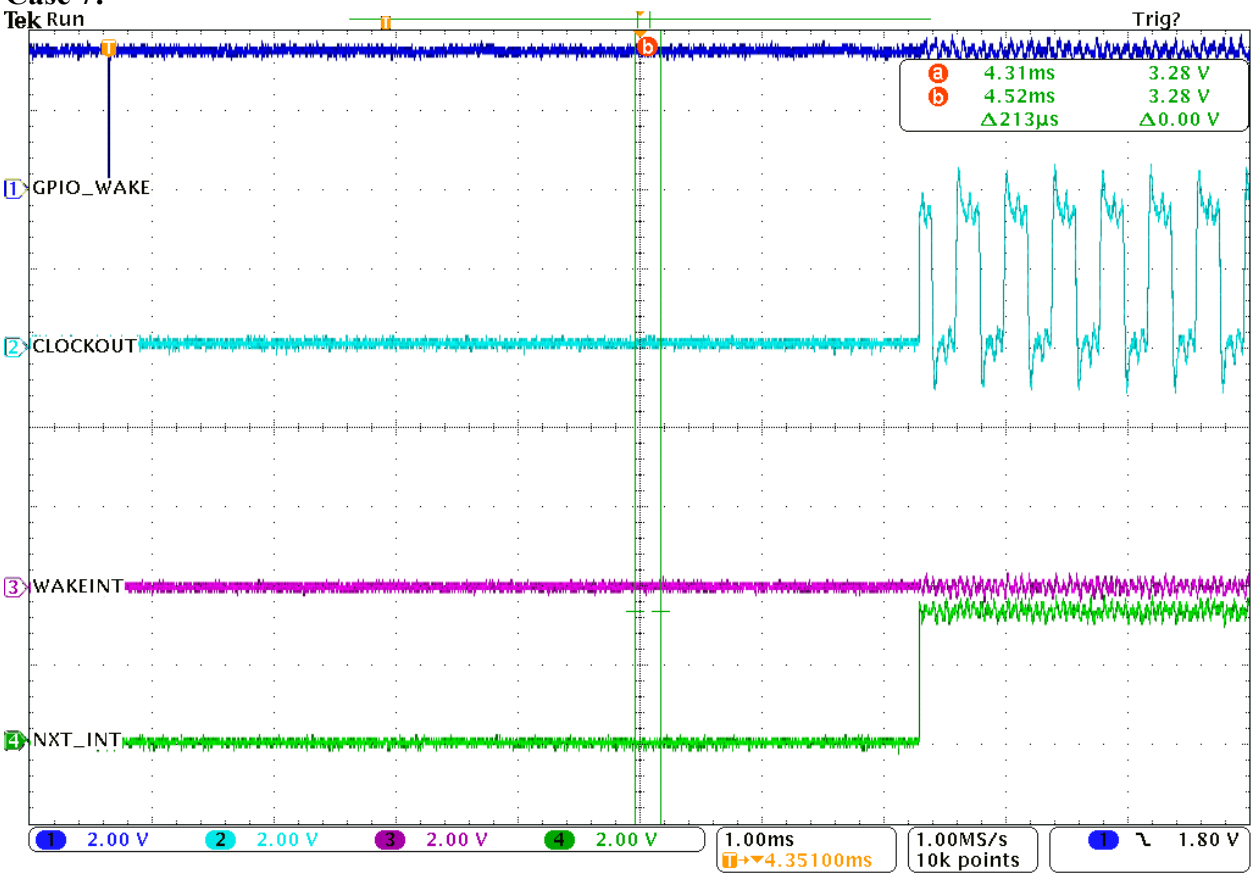
Case 7:



PIEIER1.8 = 1, IER = 0x0001, INTM = 1. WAKEINT_ISR is not executed. The instruction following IDLE is executed.

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