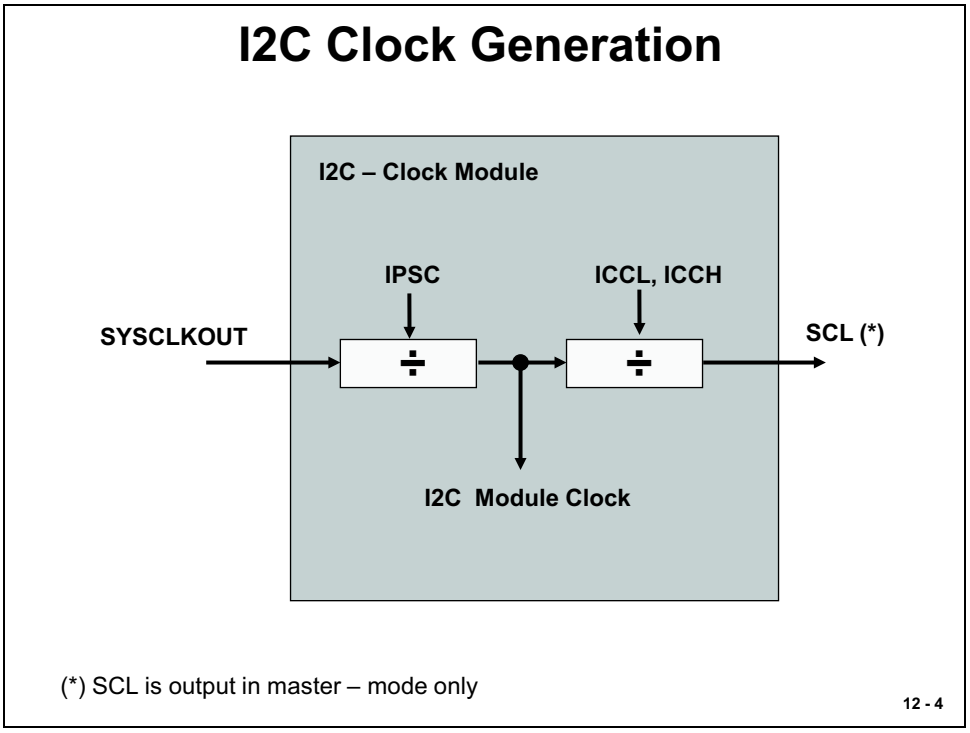
I2C Clock Generation

As shown in Slide 12-4, the I2C input clock is equivalent to the CPU clock (SYSCLKOUT) and is then divided twice more inside the I2C module to produce the module clock and the master SCL clock.



The I2C module clock determines the frequency at which the I2C module operates. A programmable pre-scaler in the I2C module divides down the I2C input clock to produce the module clock. To specify the divide-down value, initialize the IPSC field of the pre-scaler register, I2CPSC. The resulting frequency should be in the range of 7 - 12 MHz and is given by:

$$I2C\_Module\_Clock = \frac{SYSCLKOUT}{(IPSC + 1)}$$

IPSC must be initialized only while the I2C module is in the reset state (IRS = 0 in I2CMDR). The pre-scaled frequency takes effect only when IRS is changed to 1. Changing the IPSC value while IRS = 1 has no effect.

The master clock appears on the SCL pin when the I2C module is configured to be a master on the I2C-bus. This clock controls the timing of communication between the I2C module and a slave. As shown in slide 12-4, a second clock divider in the I2C module divides down the module clock to produce the master clock. The clock divider uses the ICCL value of I2CCLKL to divide down the low portion of the module clock signal and uses the ICCH value of I2CCLKH to divide down the high portion of the module clock signal.

Example for I2C-clock calculation:

The period of the master clock (T_{MASTER}) is a multiple of the period of the I2C module clock:

$$T_{MASTER} = \frac{(IPSC+1)[(ICCL+d)+(ICCH+d)]}{SYSCLKOUT}$$

Parameter d is a systematic offset, which depends on the device type.

Example: Set I2C-Master clock to 50 kHz for a 150 MHz device

(1) Set I2C module clock to 10MHz:

$$10MHz = \frac{100MHz}{(IPSC+1)};$$ IPSC = 14

(2) Set I2C Master clock to 20µs; use d = 5

$$20\mu s = \frac{(14+1)[(ICCL+5)+(ICCH+5)]}{150MHz}$$

ICCL + ICCH = 190;

To produce an I2C master clock with a duty cycle of 50% set:

- IPSC = 14
- ICCL = 95
- ICCH = 95

The following table give some more options for the I2C clock unit:

SYSCLKOUT	100 MHz	100MHz	150MHz	150MHz
I2C-clock	IPSC	ICCL / ICCH	IPSC	ICCL / ICCH
50 kHz	9	95 / 95	14	95 /95
100 kHz	9	45 / 45	14	45 /45
400 kHz	9	10 / 5	14	10 / 5