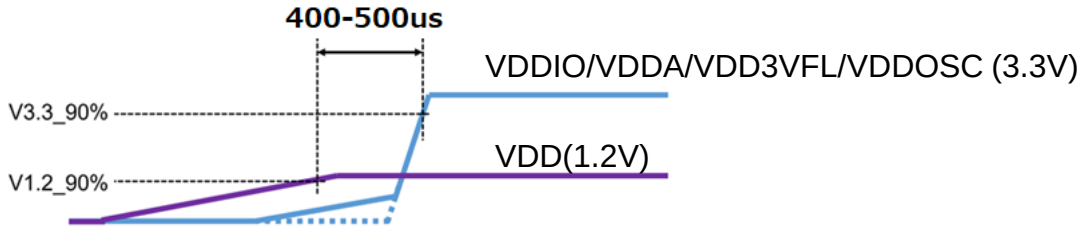
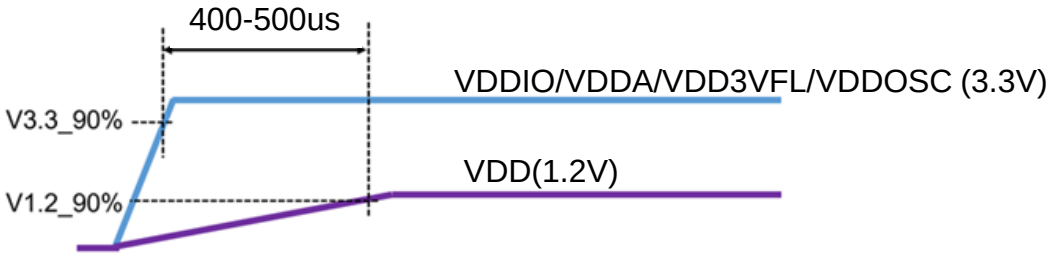
TMS430F28377D:
Inquiry about Power up sequence

Customer is develop the next generation of their system with TMS320F28377DZWTT, they noticed there is the issue on power-up sequence in their system. According to customer's comments, their power-up-sequence is as follows. This means, VDDIO is powered up after VDD(1.2V) is powered up. As the result, customer seems to observed the leakage on VDDIO power rails.



Therefore, customer plans to modify above power sequence as follows. However, customer has some inquiries about this power-up sequence (next page).



According to the datasheet “8.9.1.3 VDD Requirements”, there are following descriptions as you know.

8.9.1.3 V_{DD} Requirements

The internal VREG is not supported. The VREGENZ pin must be tied to V_{DDIO} and an external source used to supply 1.2 V to V_{DD}. During the ramp, V_{DD} should be kept no more than 0.3 V above V_{DDIO}.

V_{DDOSC} and V_{DD} must be powered on and off at the same time. V_{DDOSC} should not be powered on when V_{DD} is off. For applications not powering V_{DDOSC} and V_{DD} at the same time, see the "INTOSC: V_{DDOSC} Powered Without V_{DD} Can Cause INTOSC Frequency Drift" advisory in the *TMS320F2837xD Dual-Core MCUs Silicon Errata* .

1. Regarding the improved power-up sequence, VDDIO(3.3V) and VDD(1.2V) is powered up at the same time, but, there is difference in the time to actually power-up(90% voltage). This period is 400-500us. Would you think any issue for this behavior?
2. Customer is asking if they need to adjust power-up(90% voltage) time as same time? But, it seems difficult to adjust this timing.
3. Regarding above “VDDOSC(3.3V) and VDD(1.2V) must be powered on and off at the same time.”, customer is afraid that it may be spec violation. Would you think any issue for this point?