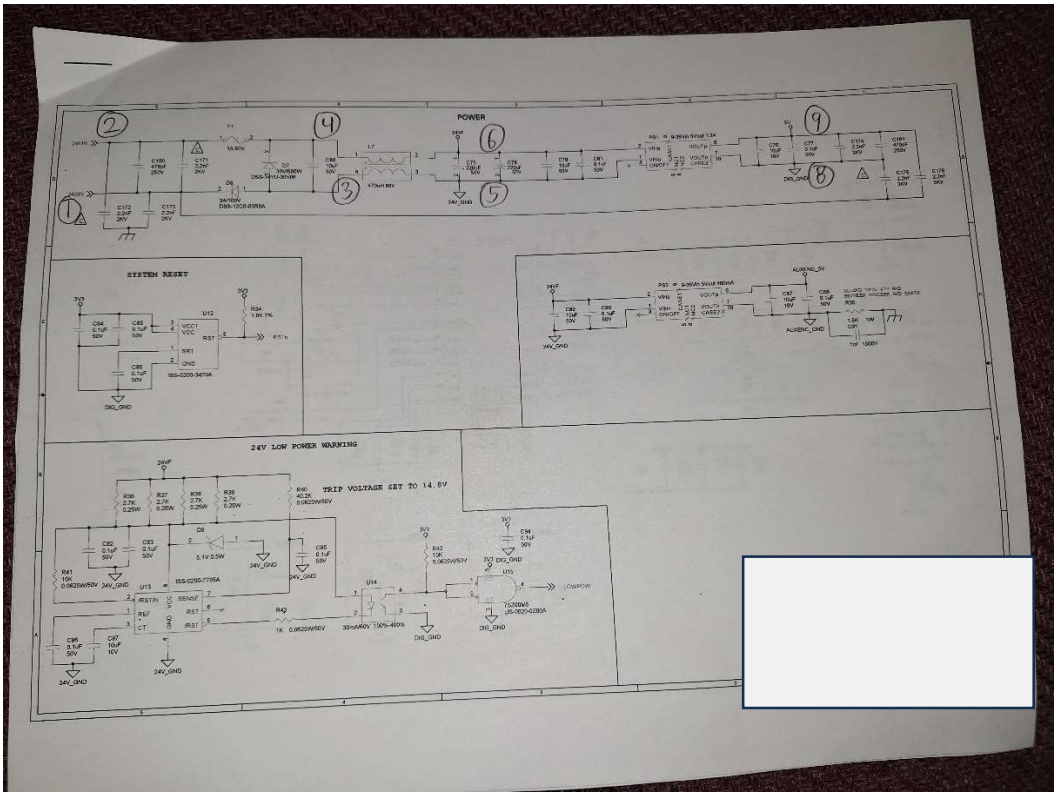
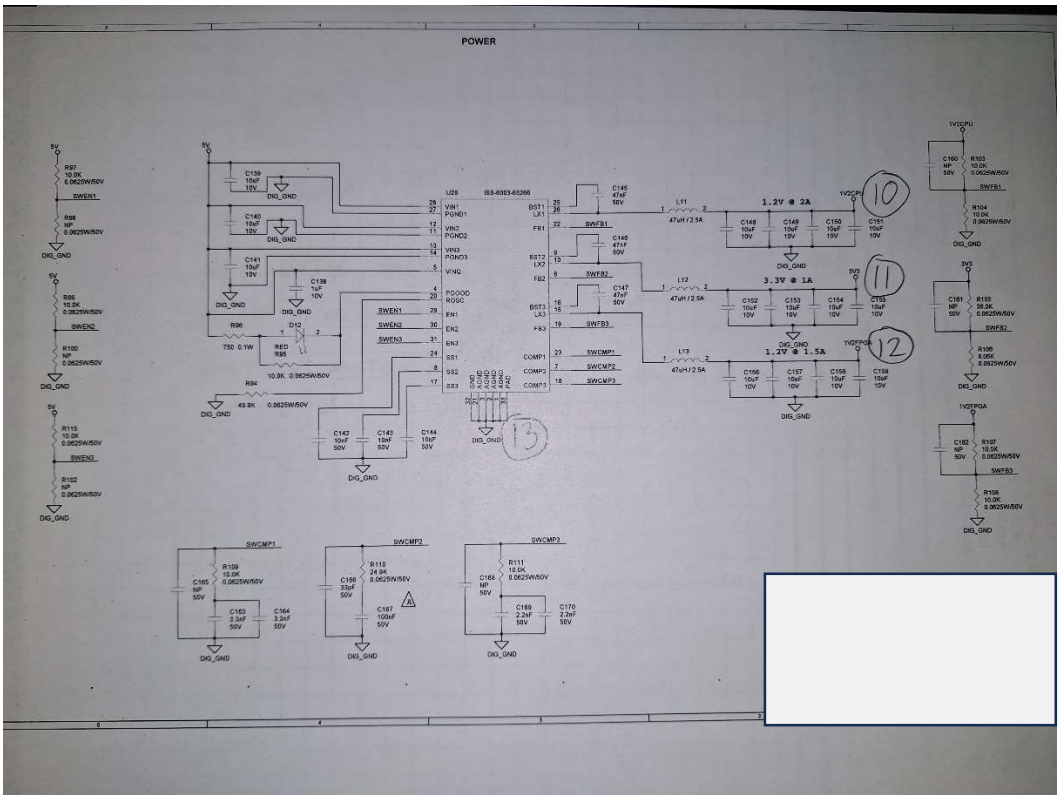
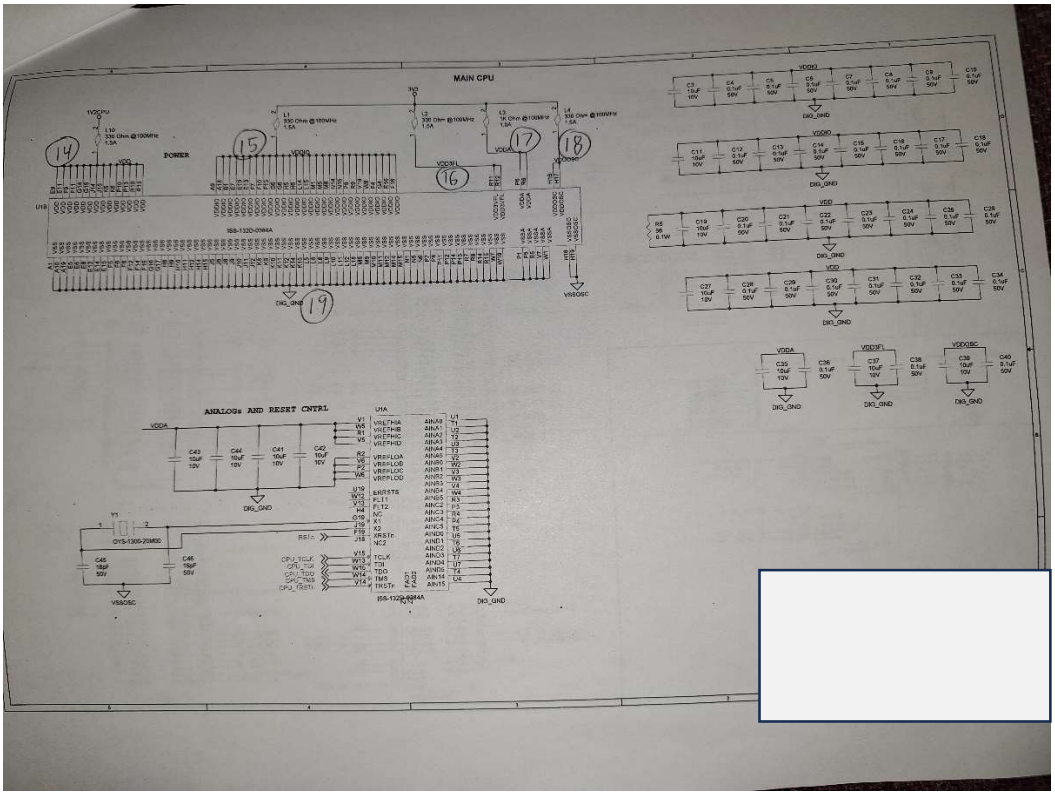
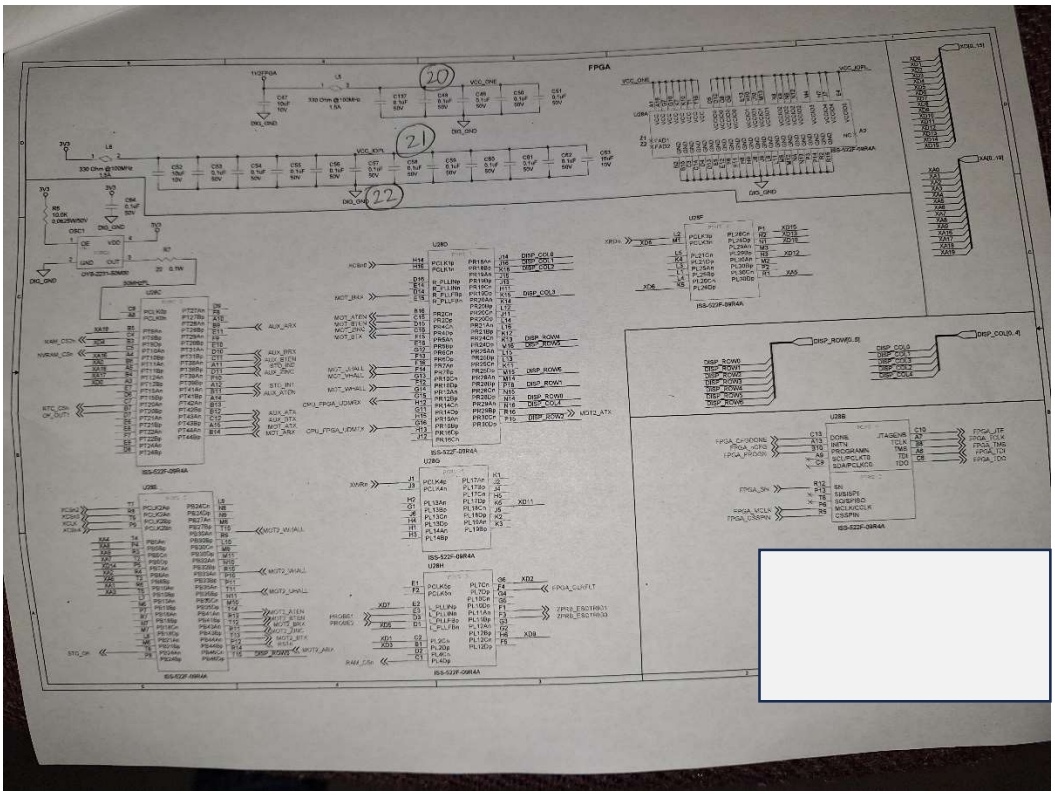
After modifications to filtering on 24V input on control board, results are shown here.

Added components marked by Rev C markers, Test points shown in circled numbers.

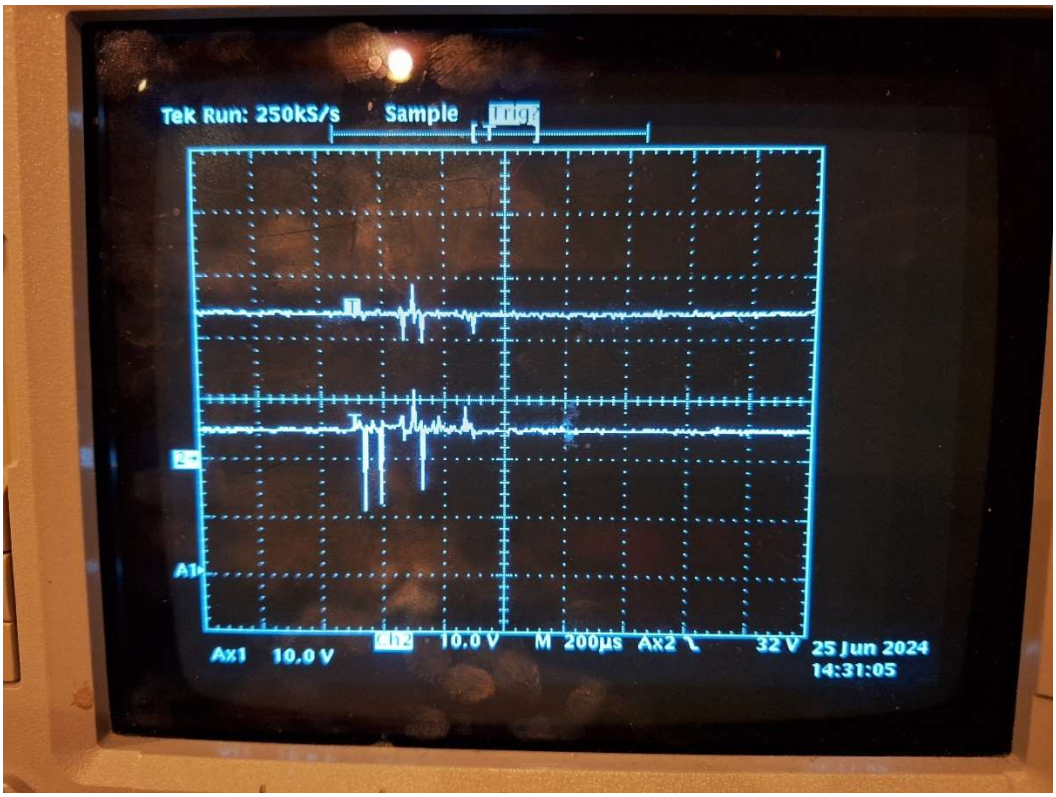




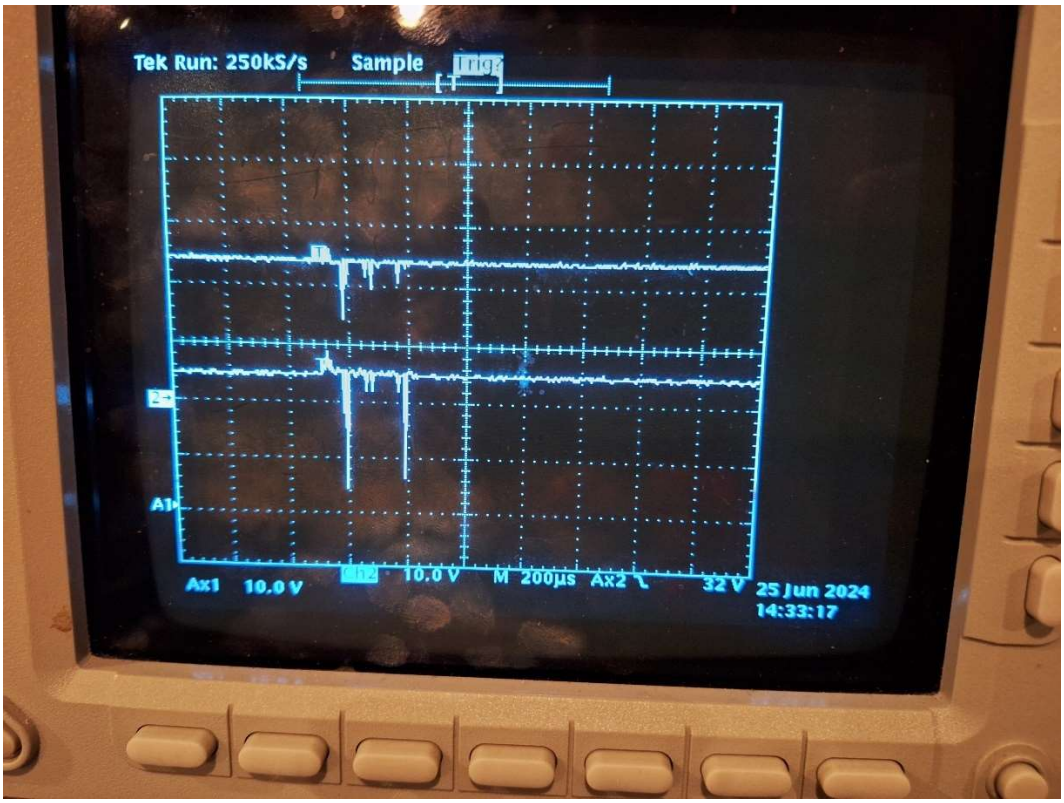

MAIN CPU
POWER
ANALOGs AND RESET CNTRL
DIG_GND
VSSOSC


FPGA
DIG_GND

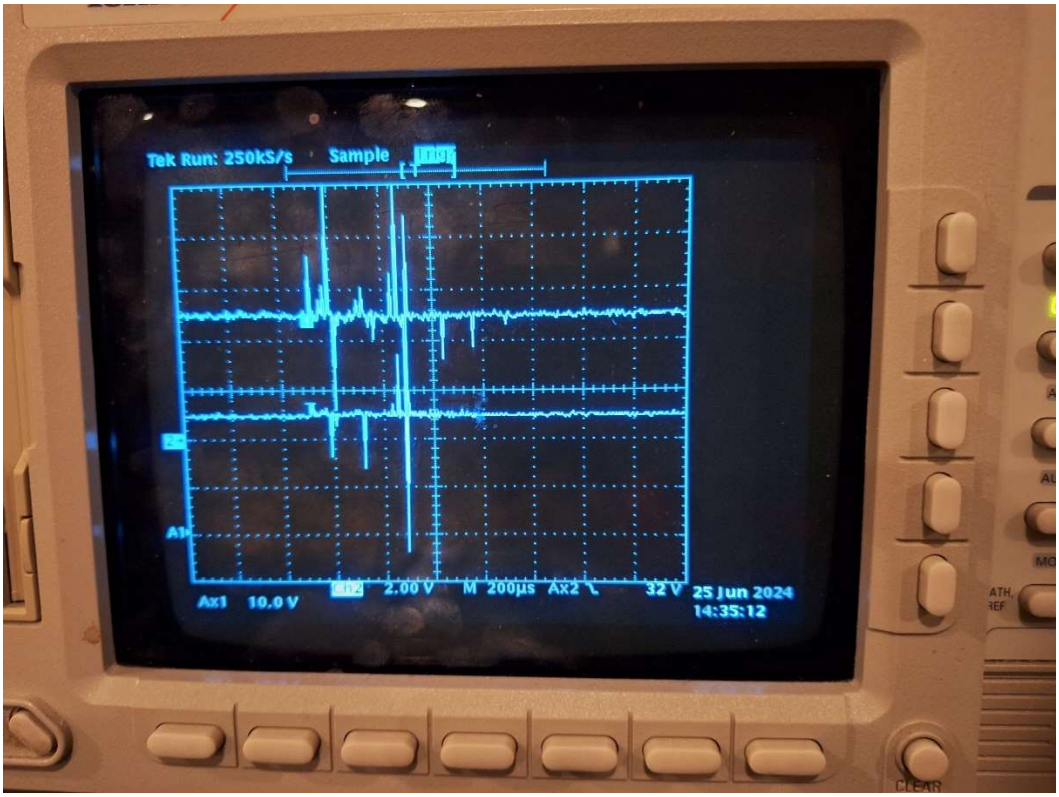
Channel AX1 – 2,1 Channel 2 – 4,3



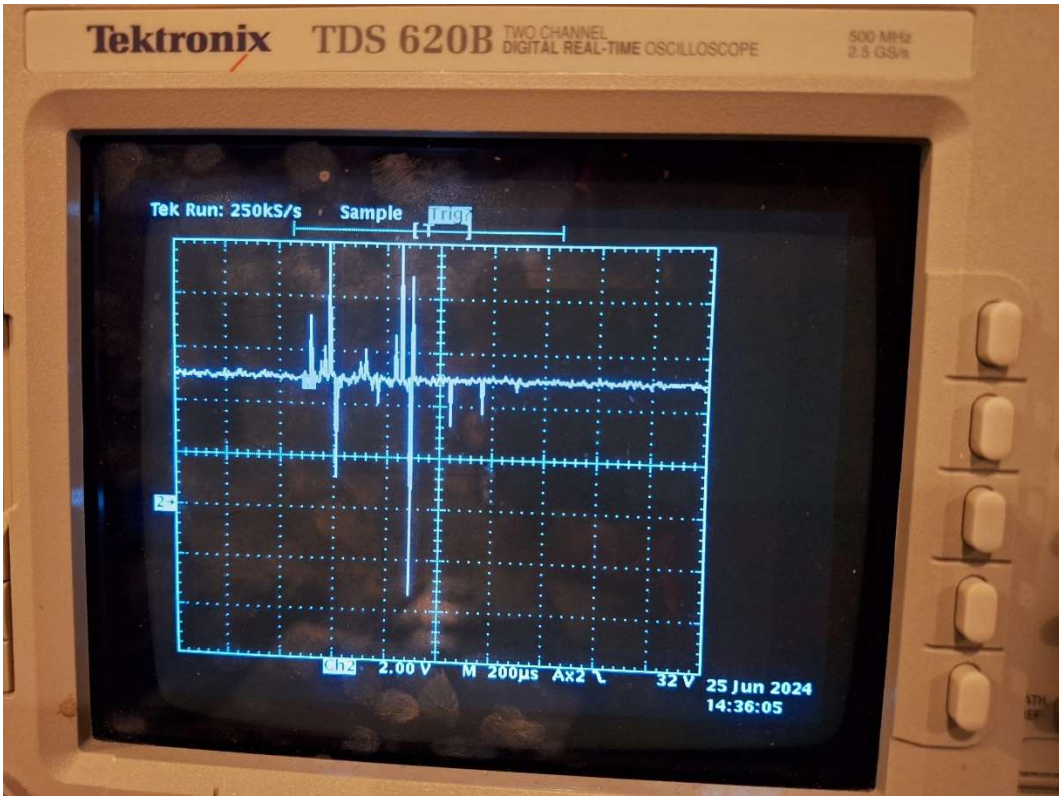
Channel AX1 – 2,1 Channel 2 – 6,5



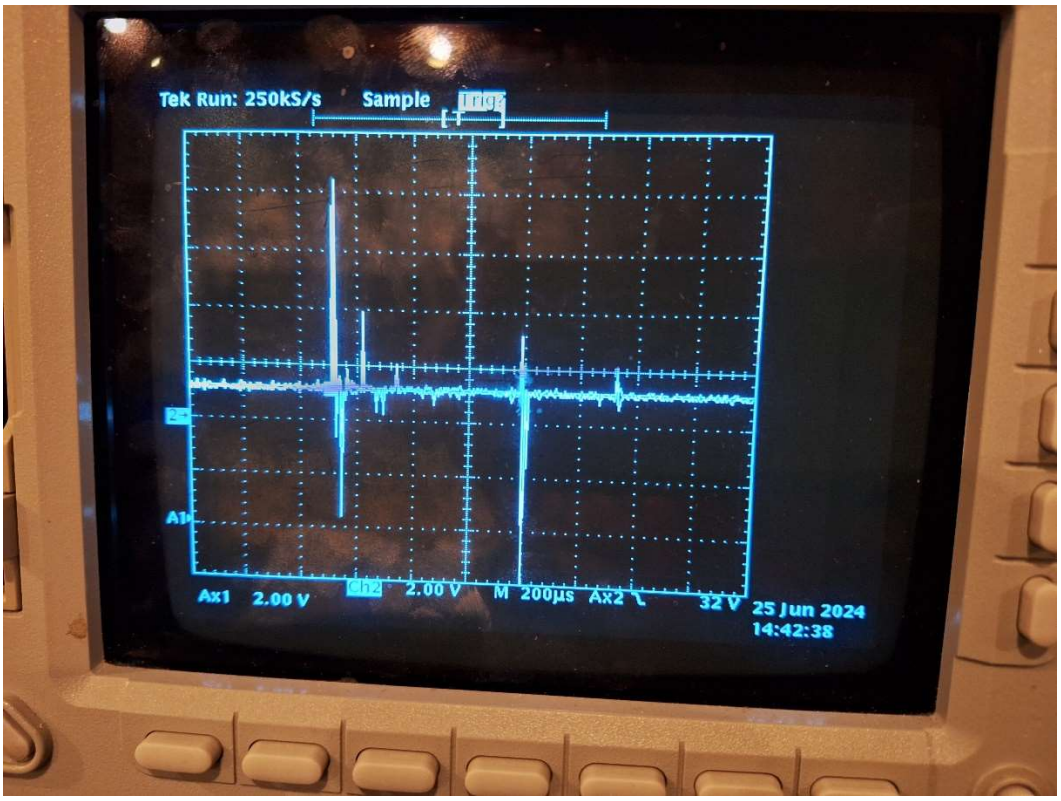
Channel AX1 – 2,1 Channel 2 – 9,8



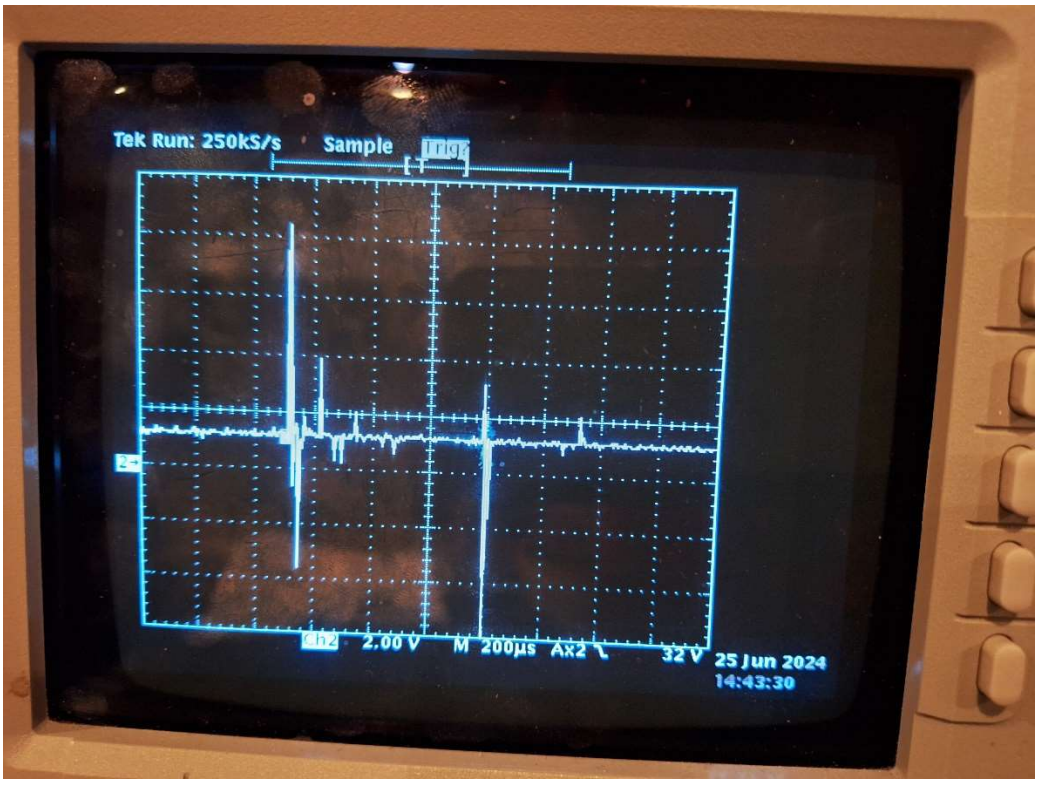
Same capture as above, Channel AX1 – OFF Channel 2 – 4,3



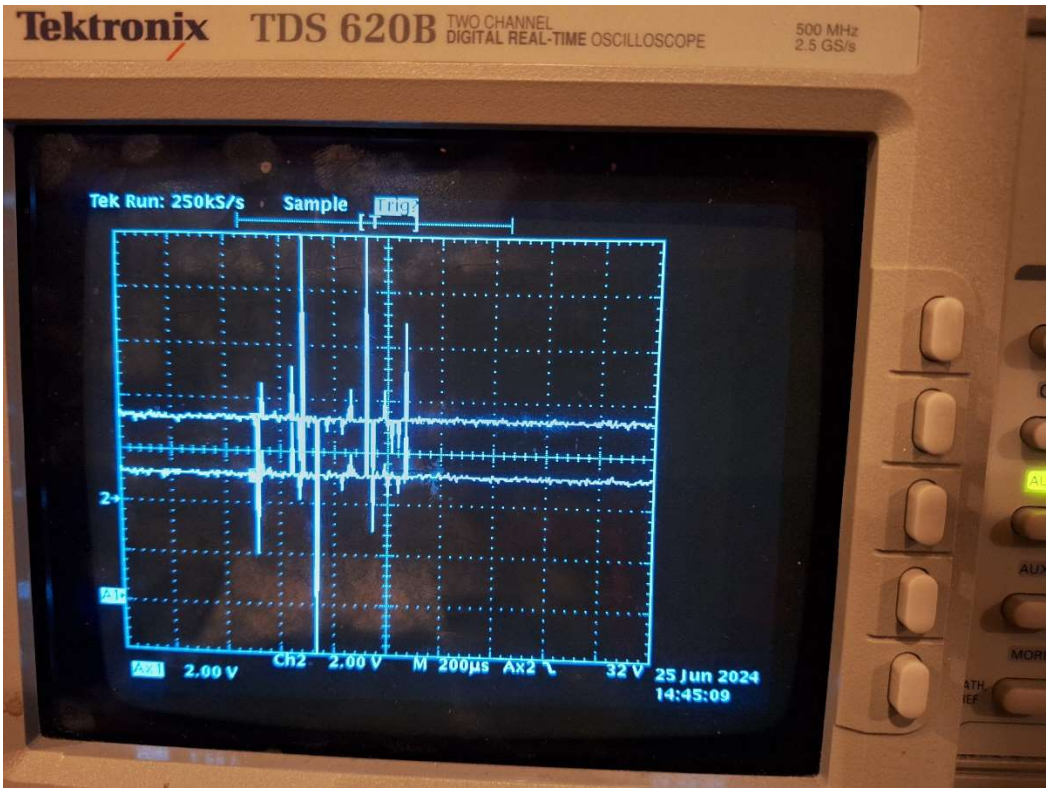
Channel AX1 – 9,8 Channel 2 – 10,13



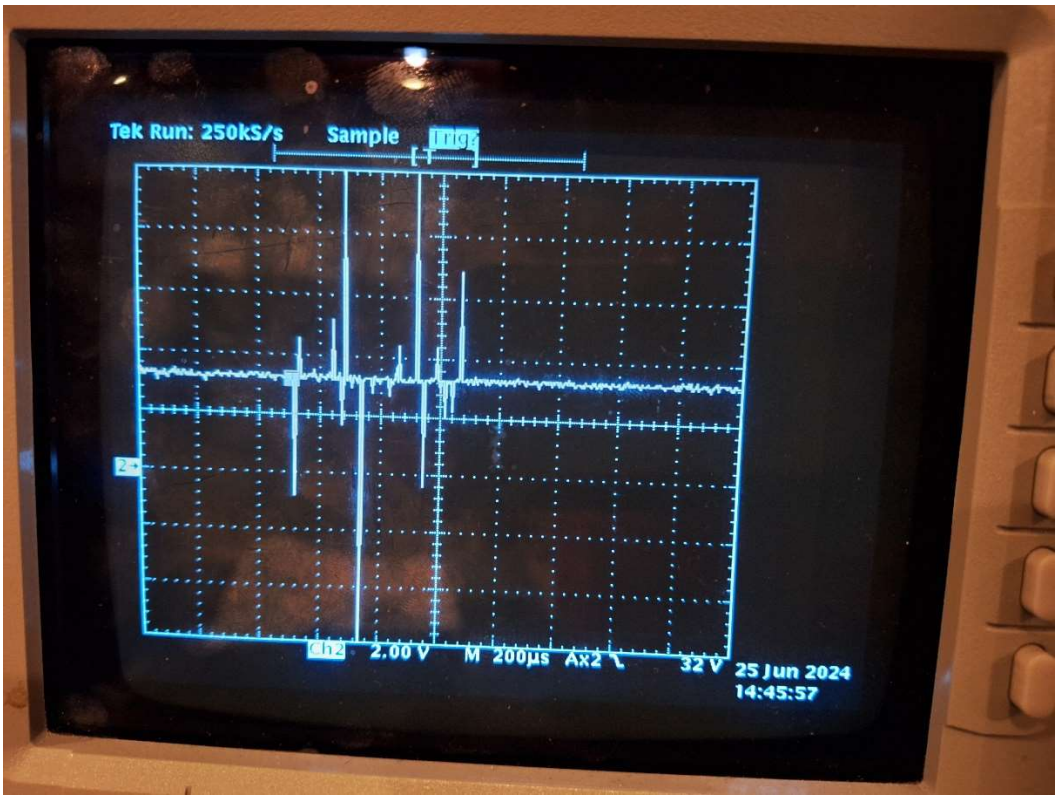
Same capture as above, Channel AX1 – OFF Channel 2 – 10,13



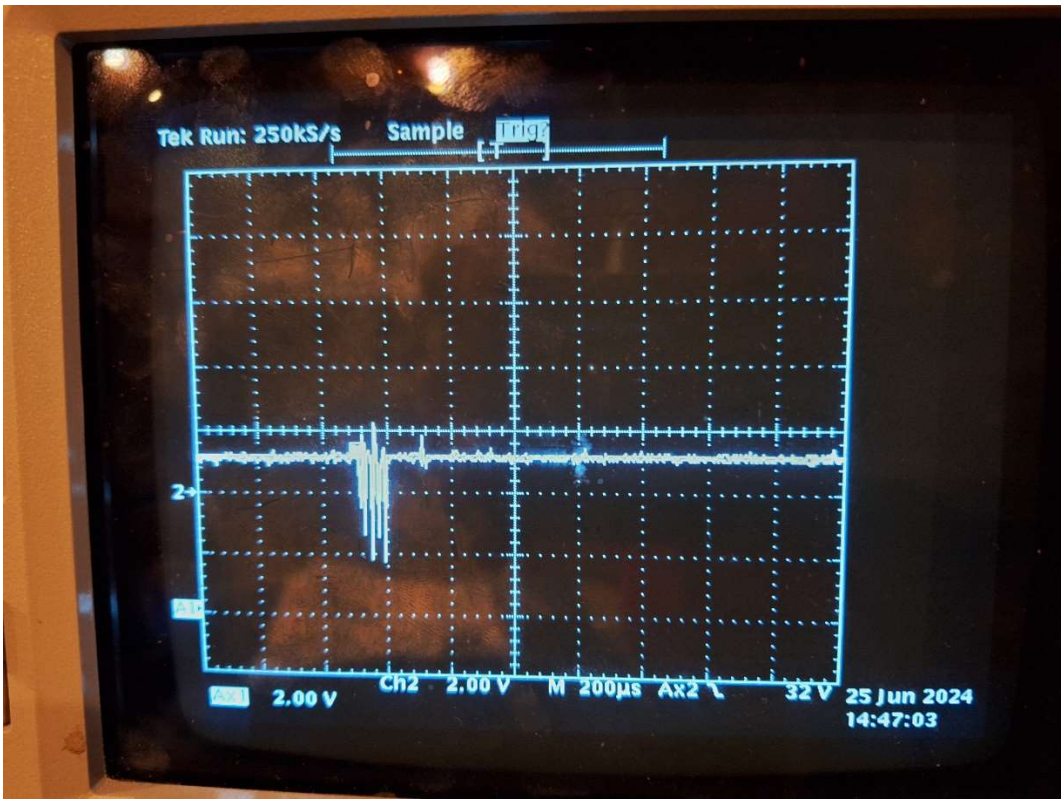
Channel AX1 – 9,8 Channel 2 – 11,13



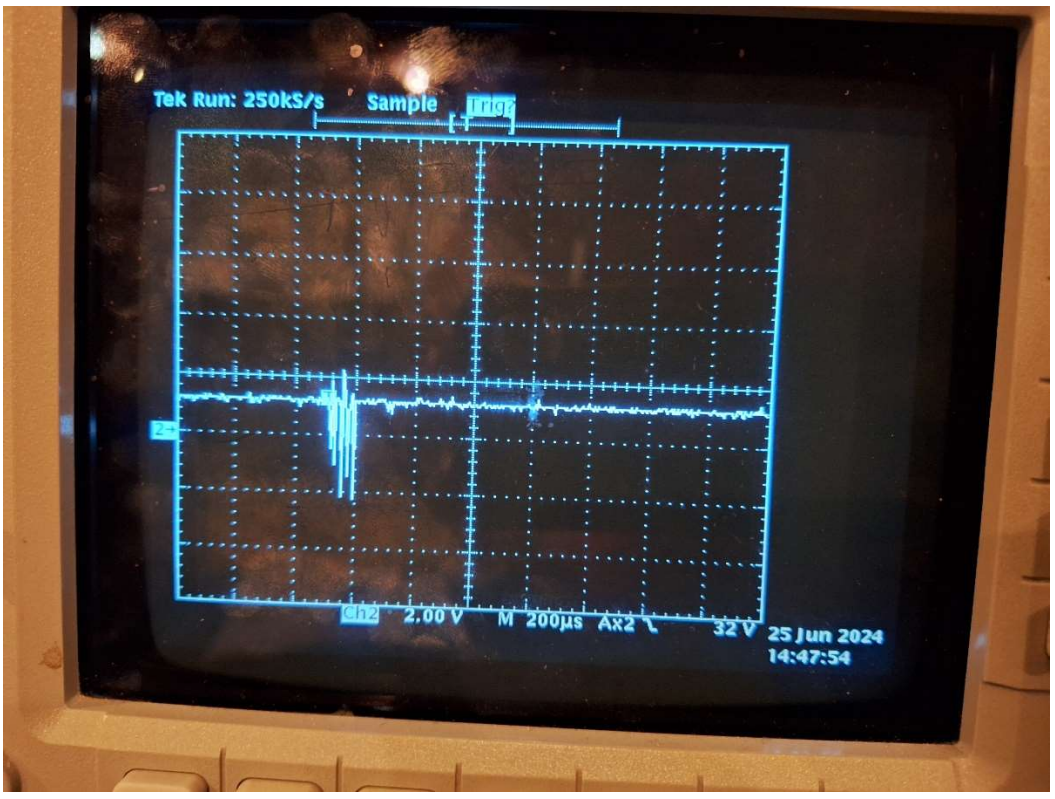
Same capture as above, Channel AX1 – OFF Channel 2 – 11,13



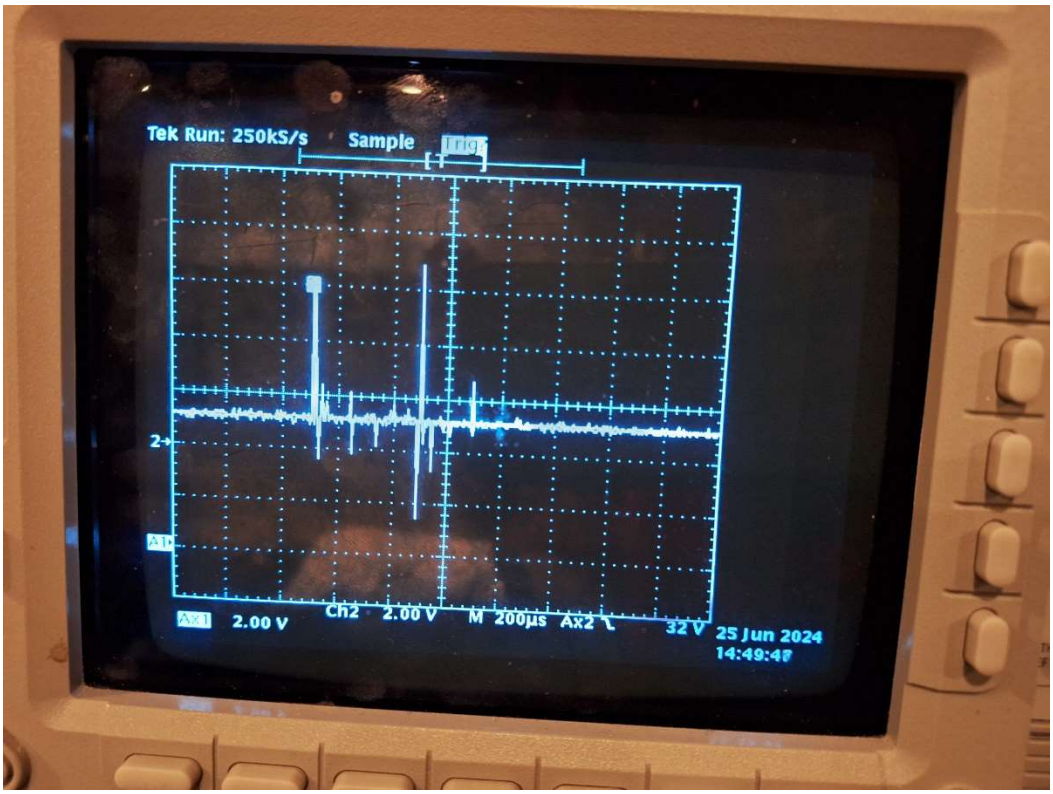
Channel AX1 – 9,8 Channel 2 – 12,13



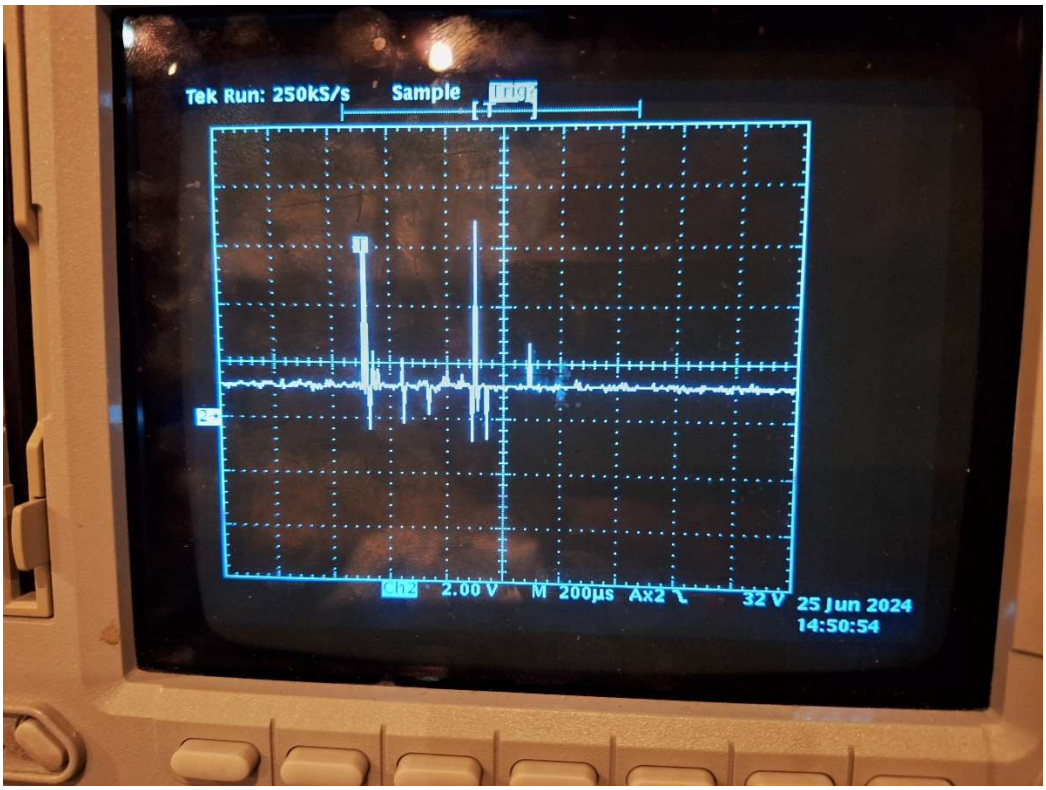
Same capture as above, Channel AX1 – OFF Channel 2 – 12,13



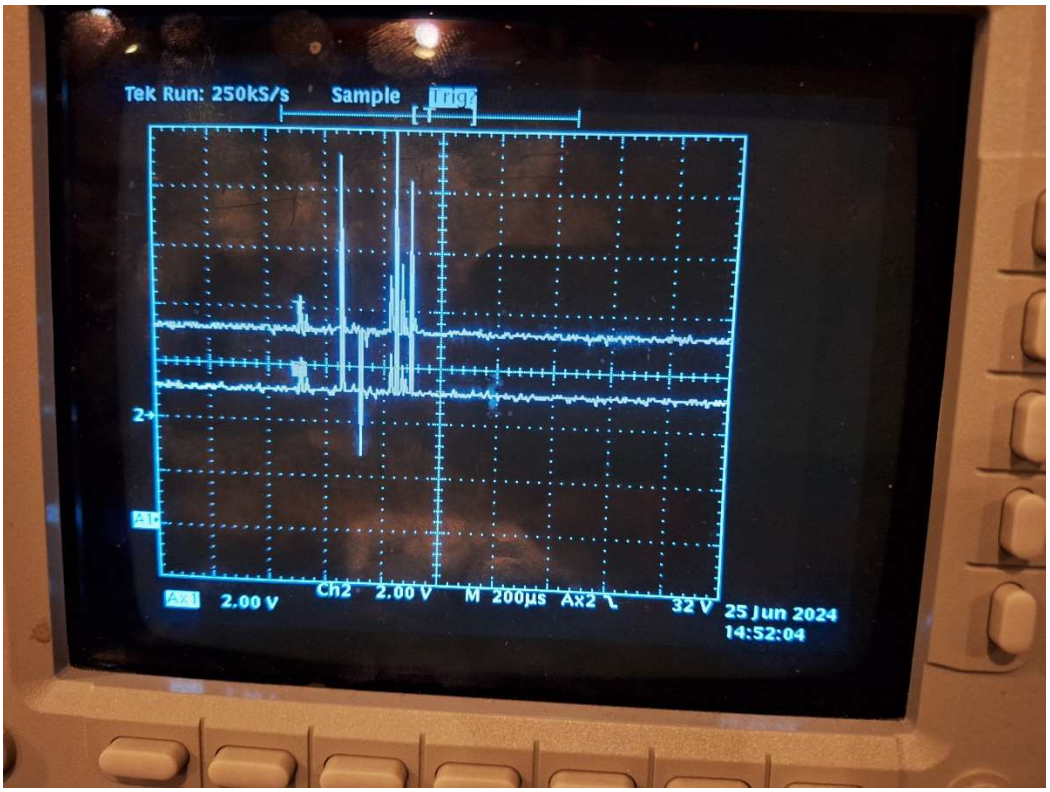
Channel AX1 – 9,8 Channel 2 – 14,19



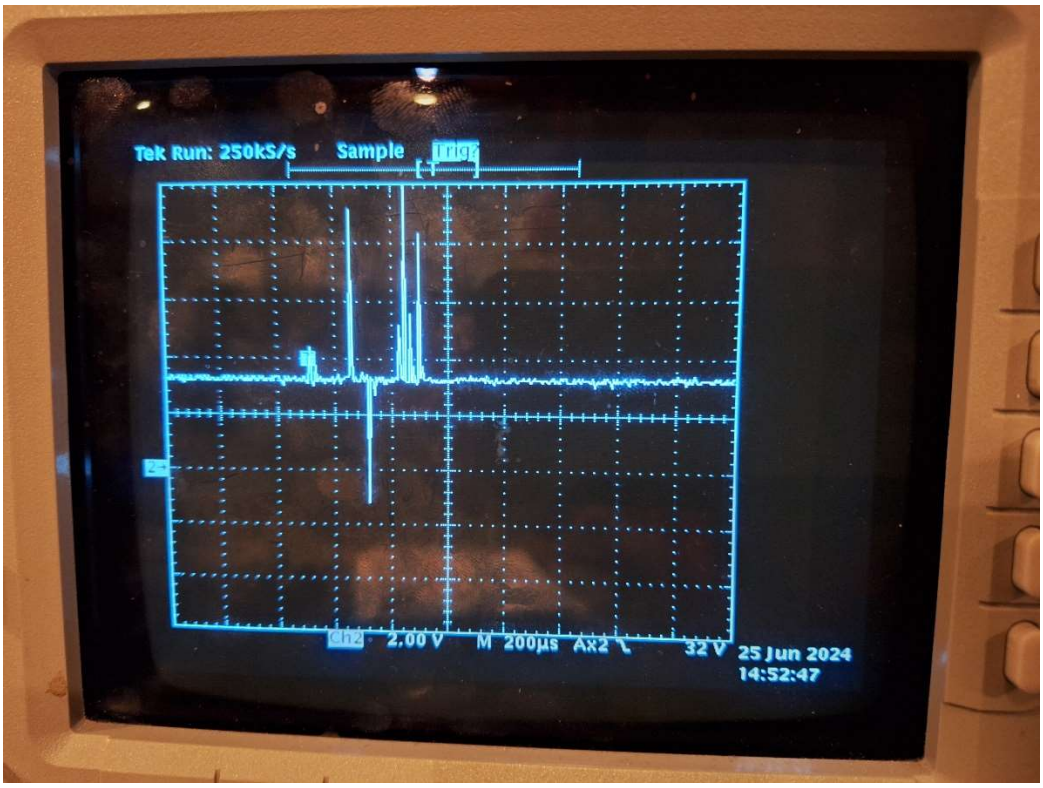
Same capture as above, Channel AX1 – OFF Channel 2 – 14,19



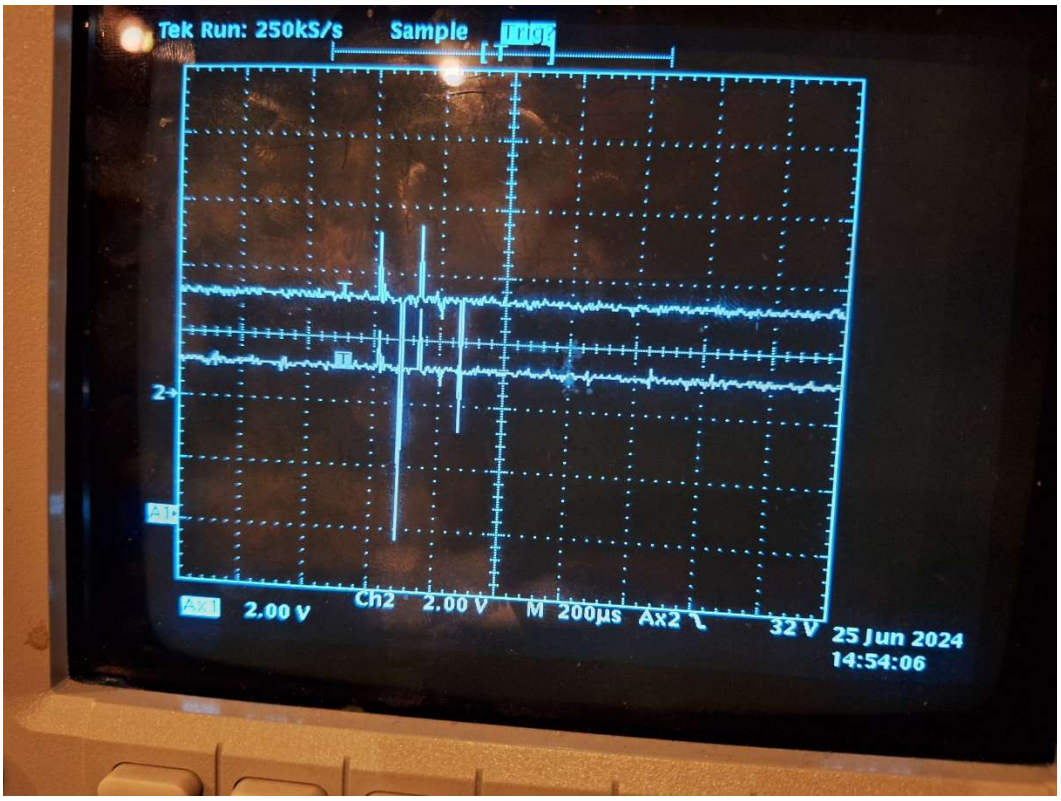
Channel AX1 – 9,8 Channel 2 – 15,19



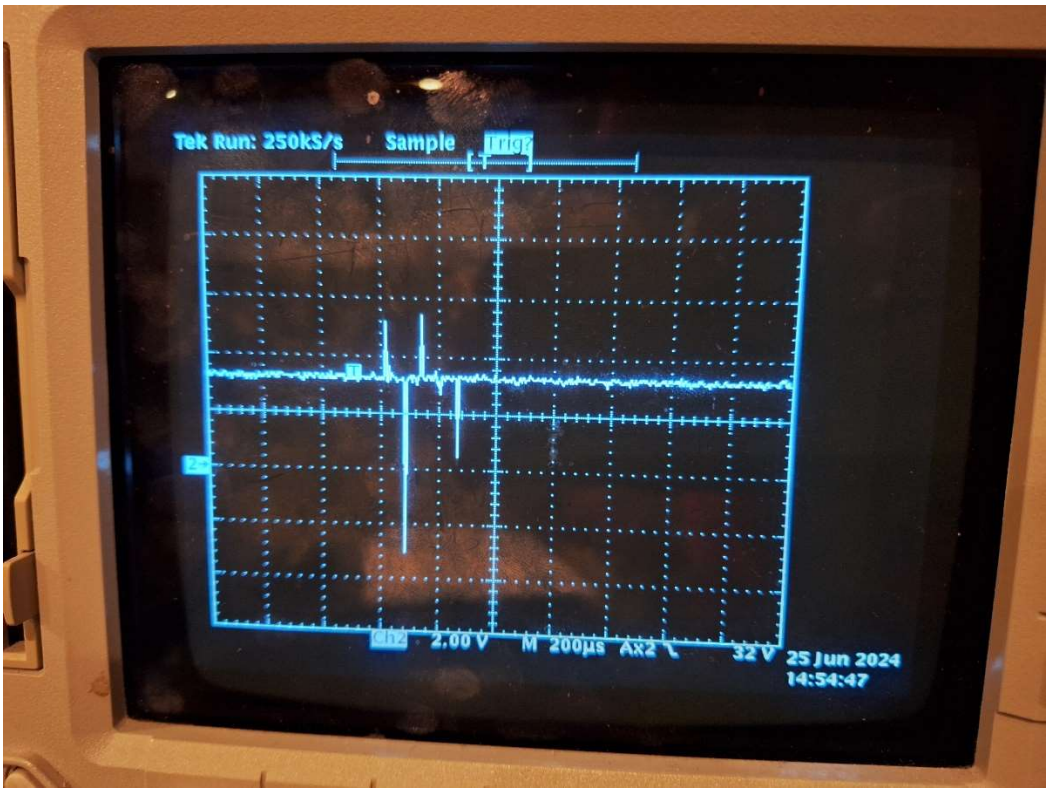
Same capture as above, Channel AX1 – OFF Channel 2 – 15,19



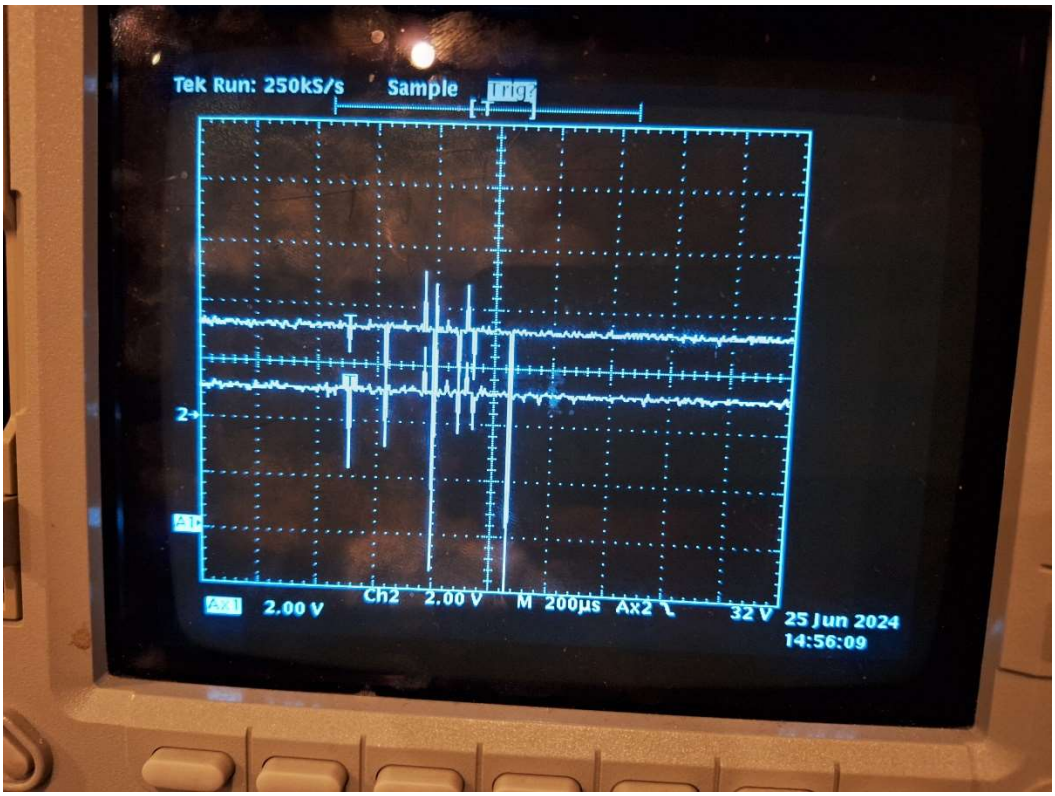
Channel AX1 – 9,8 Channel 2 – 16,19



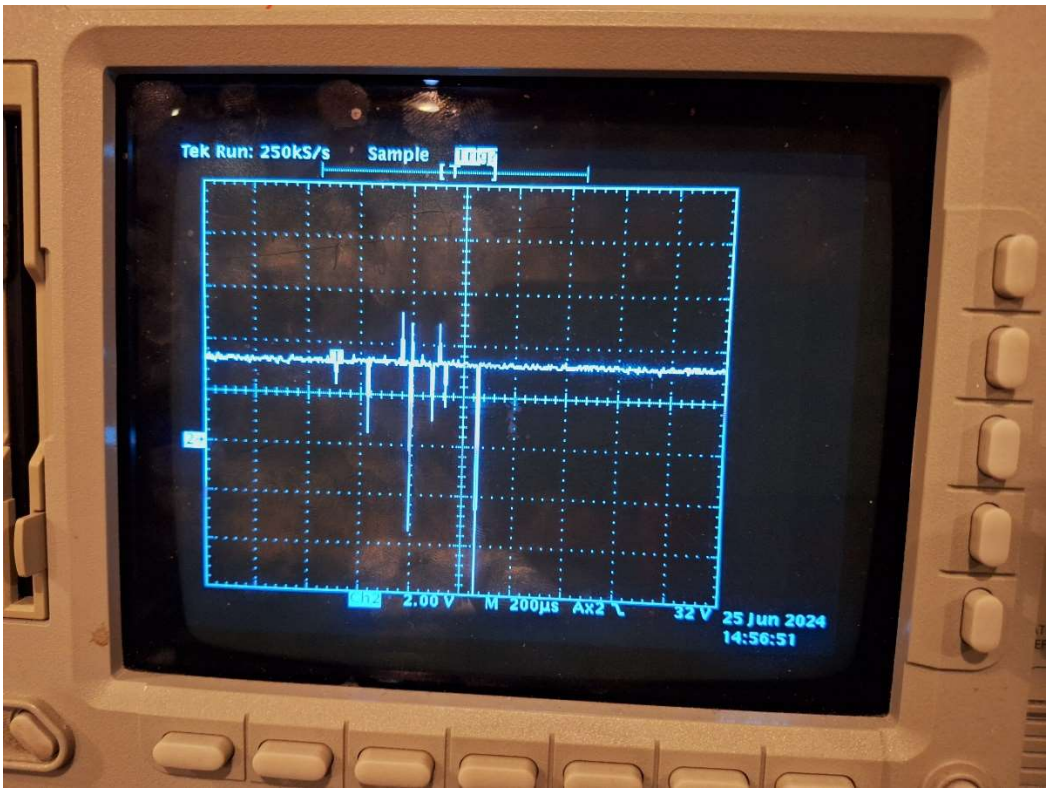
Same capture as above, Channel AX1 – OFF Channel 2 – 16,19



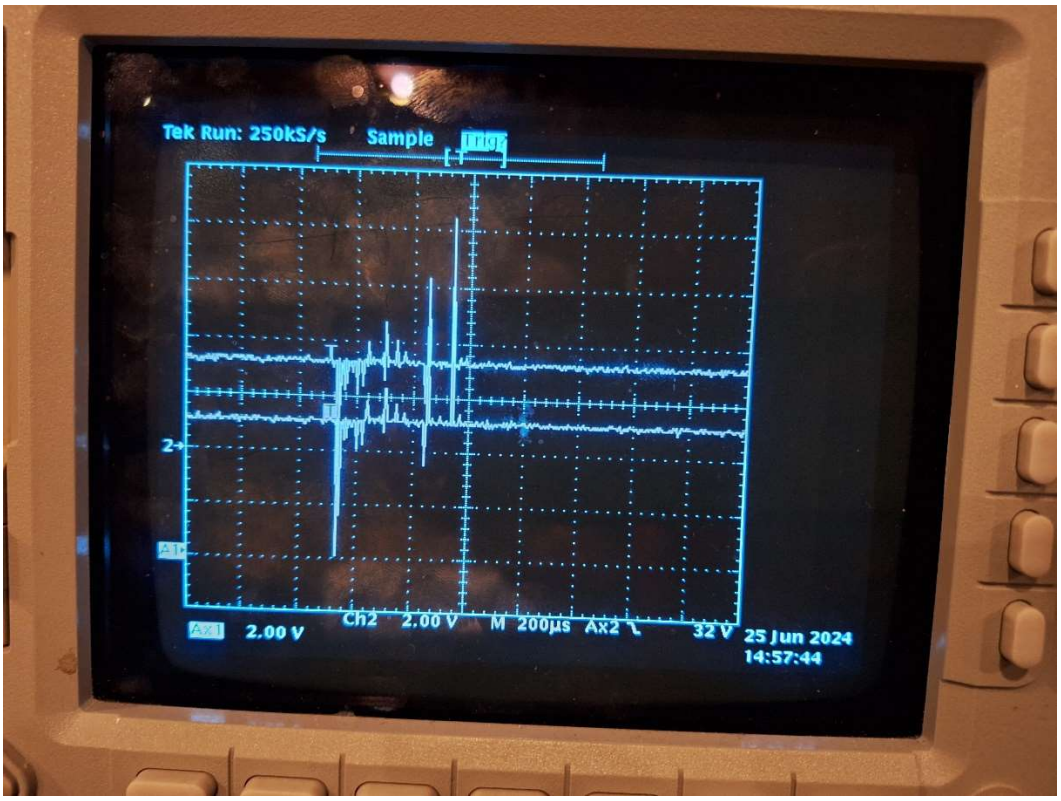
Channel AX1 – 9,8 Channel 2 – 17,19



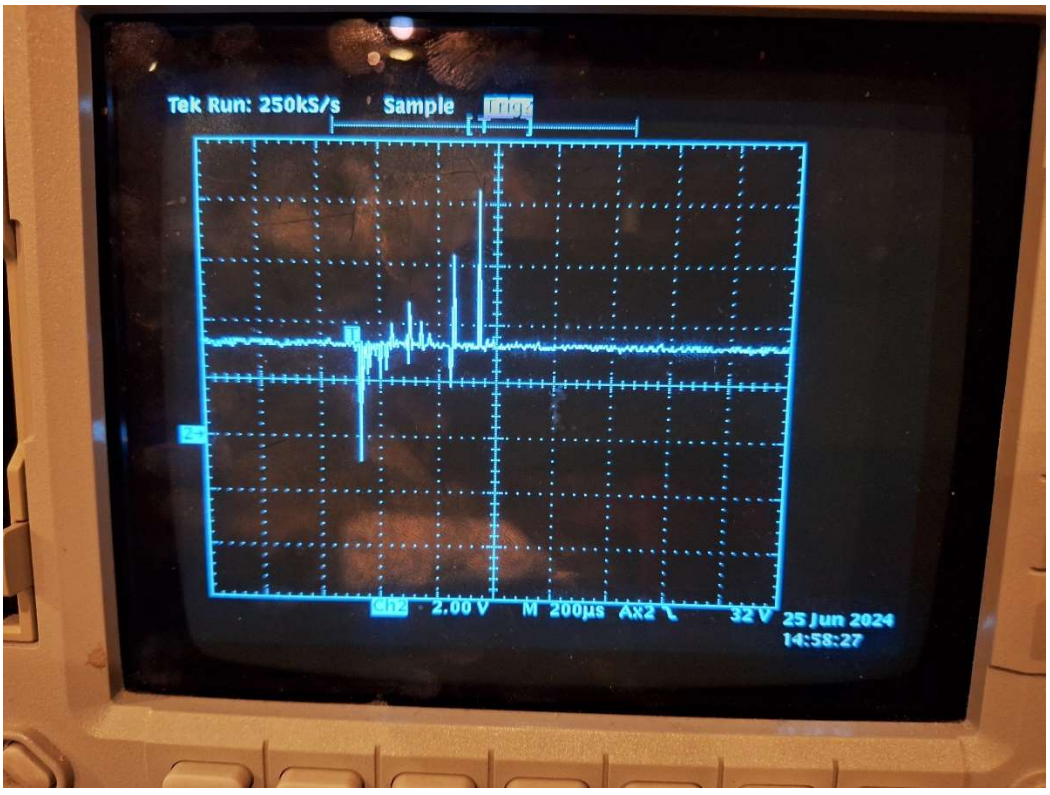
Same capture as above, Channel AX1 – OFF Channel 2 – 17,19



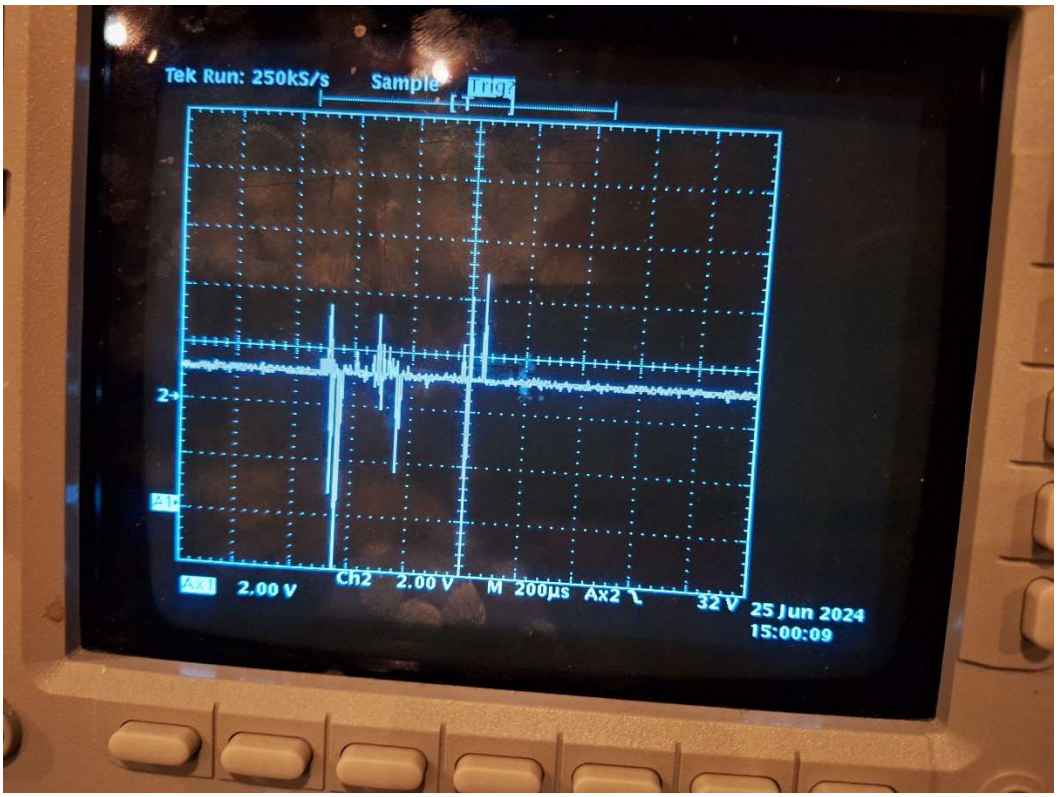
Channel AX1 – 9,8 Channel 2 – 18,19



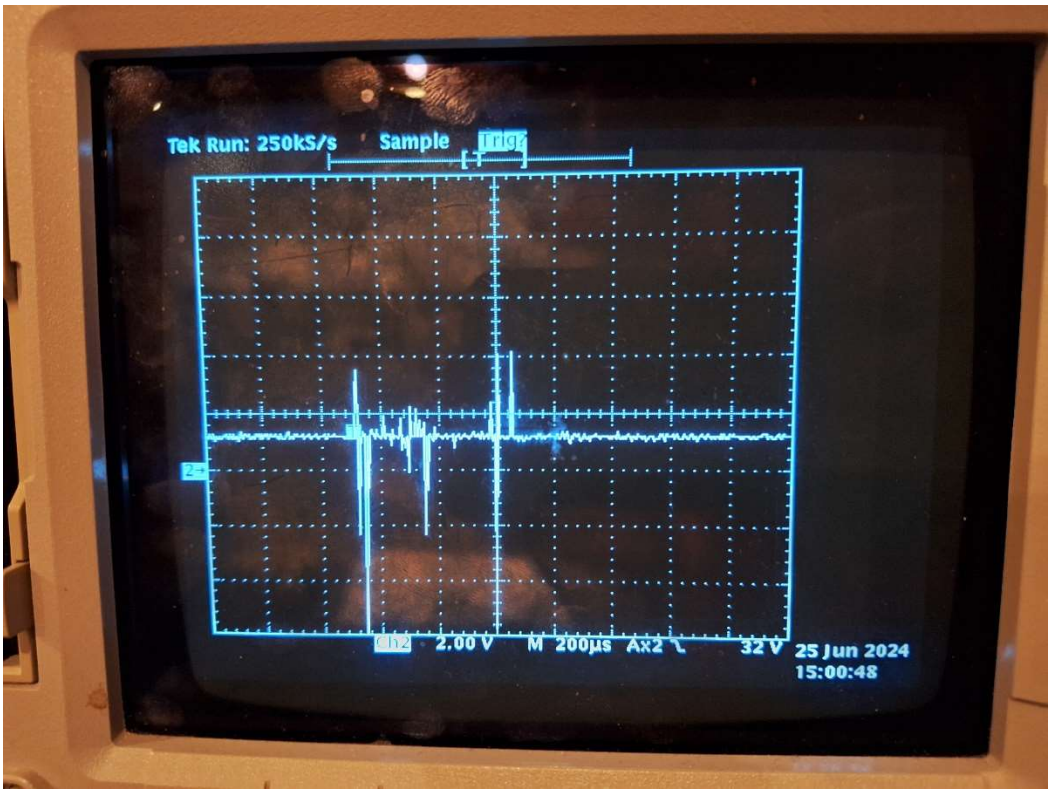
Same capture as above, Channel AX1 – OFF Channel 2 – 18,19



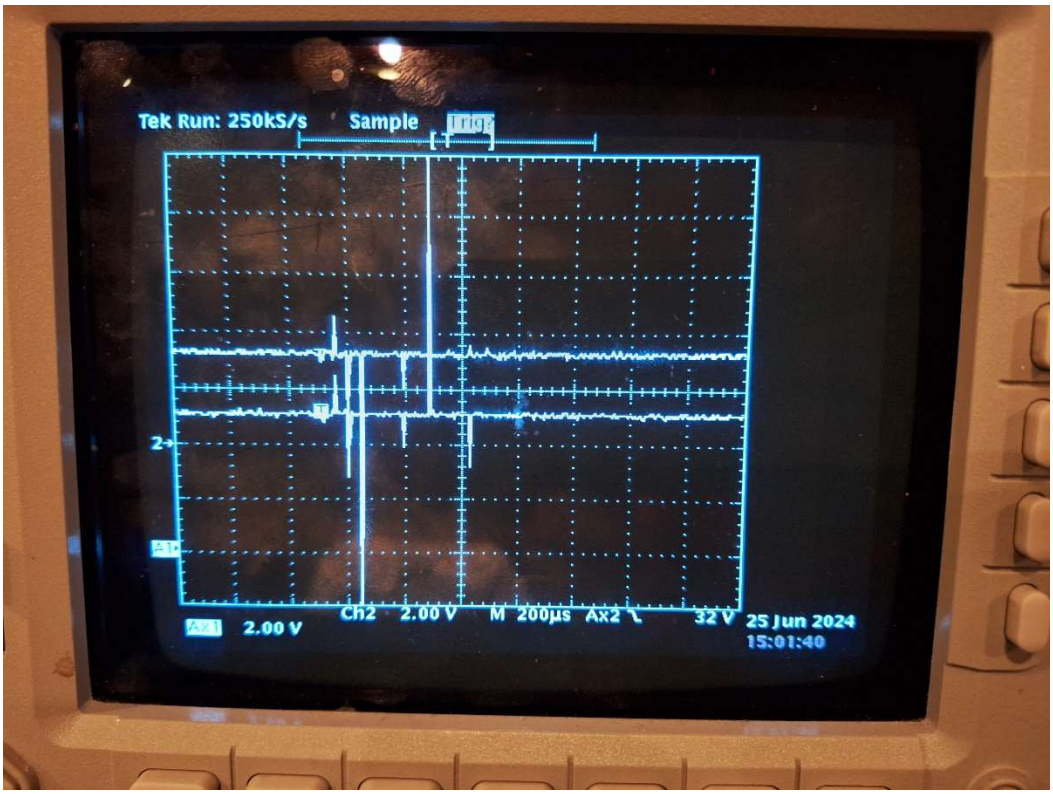
Channel AX1 – 9,8 Channel 2 – 20,22



Same capture as above, Channel AX1 – OFF Channel 2 – 20,22



Channel AX1 – 9,8 Channel 2 – 21,22



Same capture as above, Channel AX1 – OFF Channel 2 – 21,22