



FINAL 8D REPORT

2024-09-29 - Rev. A

QEM-CCR-2409-00926 [CGD-2021070301 /]

Chengdu CRP Robot Technology Co., Ltd.

TI Device: TMS320F28377DZWTT

TI Information – Selective Disclosure



Customer Name:	Chengdu CRP Robot Technology Co., Ltd.	Customer Contact:	Chen Hui
Customer Site:		End Customer	CHENGDU CRP ROBOT TECHNOLOGY CO., LTD.
Event Type / Origin of Detection:	Field Failure [mile / km]	Customer Contact(s)	chenhui@crprobot.com
Customer Production Date:		E-mail:	
Customer P/N:			
RMA# / SCAR#	CGD-2021070301	TI P/N or Device Type:	TMS320F28377DZWTT
Customer Tracking:		TI QEM Event:	QEM-CCR-2409-00926
Quantity of Received Unit(s):	3	Unit Receive Date:	2024-09-26
Customer Notification Date:	2024-09-18	Current Action:	

EXECUTIVE SUMMARY:

TI received **3** unit(s) of TI PN: **TMS320F28377DZWTT** (Customer P/N:) with customer provided issue description in Customer Issue Description.

TI analysis verified the issue: Electrically Induced Physical Damage (EIPD) was confirmed, and the cause was judged to be **Electrical Overstress (EOS)**.

Note: Abbreviations used in this report are listed in Appendix 2.

D1) TEAM MEMBERS:

TI Team Members	Process Role	Email
Cindy Wu	Event Owner	cindy-wu@ti.com

D2) DESCRIPTION OF NONCONFORMITY:

Identification of TI's Material						
TI Part Number:	TMS320F28377DZWTT					
Unit ID	Customer Unit ID	LTC	Assembly Lot #	Assembly Site	Fab Lot #	Fab Site
1		23ADEPW	2150686PHI	PHI	SPR1M	UMI
2		23ADEYW	2119541PHI	PHI	SPR1M	UMI
3		85ATV4W	8280853WCW	WAA	8019199	



The following customer provided issue description was extracted from the information submitted by the customer with the returned TI device and was entered into TI's Quality Event Management System (QEM):

Customer Issue Description:

Customer reported issue at: Field Failure [mile / km]

Issue type: Electrical | Issue type details: After the completion of the production assembly

TMS320F28377DZWTT normal operation for a period of time (a year, a few months), there is a program that does not run. As a rule of thumb, we first examined the crystal oscillator (a passive crystal oscillator) and found that it did not oscillate.

While troubleshooting multiple problematic boards, we encountered the following:

1. When trying to use the oscilloscope to observe whether the crystal oscillator is working, just touch the load capacitor with the oscilloscope probe, and the board will start to work normally, and the program will run as expected. This is the case with some boards.

2. On the circuit board in question, using the BGA rework station heating chip will also cause the circuit board to work normally and the program to run as expected. When the high temperature is 12 hours later, it is abnormal.

3. By replacing the new crystal oscillator or alternating the crystal oscillator, it is still found that the crystal oscillator does not oscillate.

4. After replacing the TMS320F28377DZWTT chip, the board functions normally.

6. After exchanging and soldering the abnormal chip with the normal chip, it is found that the fault follows the chip.

7. Under high temperature conditions (about 55?C), the failure rate increases significantly.

8. After power failure, the normal chip measurement: the resistance of X1 and GND is about 16.6M, and the resistance of abnormal: X1 and GND is about 330k.

9.On the circuit of the chip, it is still in an abnormal state after a 2 - megohm resistor is connected in parallel between X1 and X2. After increasing the resistance to 5 megohms, it returns to normal. However, it becomes abnormal again after running at a high temperature for 2 - 3 hours.

10. When the capacitors on X1 and X2 are replaced with 18 picofarads and 22 picofarads respectively, the crystal oscillator still cannot start oscillating. After replacing the capacitors with 8 picofarads and 12 picofarads, the crystal oscillator starts oscillating and the chip runs normally. But it becomes abnormal again after running at a high temperature for 2 - 3 hours.

11. After the capacitance is restored to 12P and 15p, the chip is normal again, and it is abnormal again after about a few minutes.

12.Later we found that the normal operation that could have been restored with a brief touch of the chip with an oscilloscope or multimeter probe is no longer restored, or more difficult to recover

13.After discovering that briefly touching the chip with an oscilloscope or multimeter probe did not restore normal operation, we left the chip for some time. As of today, the chip still does not return to normal operation. Additionally, the resistance between X1 and GND has changed from 330 k? to 3.3 k?. | Summary: 1.Provide clear photos of the top and bottom markings of the suspected device, as well as

photos of the TI label affixed to the original shipping carton/box/bag or reel. 2.We have cumulatively used 31,244 pieces of the TMS320F28377DZWTT chip. There are about 50

pieces with actual failures. These failures are not early field failures (EFFA). They all suddenly fail after a period of normal use (one year or a few months).

3. If the device has experienced EIPD, it is hoped that further failure analysis can be carried out.

TI Issue Description:

• Physical Verification Results

Units	Pass/Fai	I Description
1	Pass	No anomaly from external package

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Units	Pass/Fa	il Description
2	Pass	No anomaly from external package
3	Pass	No anomaly from external package

• Curve Trace Verification Results

Units	Pass/Fa	il Description
1	Fail	Multiple pin short to VSS
2	Fail	Multiple pin short to VSS
3	Fail	Multiple pin short to VSS

D3) IMPLEMENT AND VERIFY CONTAINMENT ACTIONS:

TI maintains an ongoing record of returns by lot number to track the number of returned TI devices for a single manufacturing lot.

TI has reviewed the return history for this unit's manufacturing lot and has not found evidence that this unit represents a sample of a larger, systemic issue with this particular production lot. Consequently, TI did not implement any additional containment actions for this production lot during initial investigation of the customer return.

The Lot Trace Code (LTC) and manufacturing date are listed below:

Units	Manufacture Date
1	03/2022
2	03/2022
3	05/2018

Containment Actions Description	Owner(s)	Date
 Review the return history of wafer fab lot(s) SPR1M 		
8019199	ті	2024-09-26
• Results: The customer return history for this fab lot(s) did not indicate an abnormal risk for the customer reported issue on the returned unit.		
 Review the lot history incl. test yield performance of assembly lot(s) 2150686PHI 		
8280853WCW	ТІ	2024-09-26
• Results: No abnormalities were noted in the assembly lot(s) history that would indicate a systemic issue exists with this lot.		



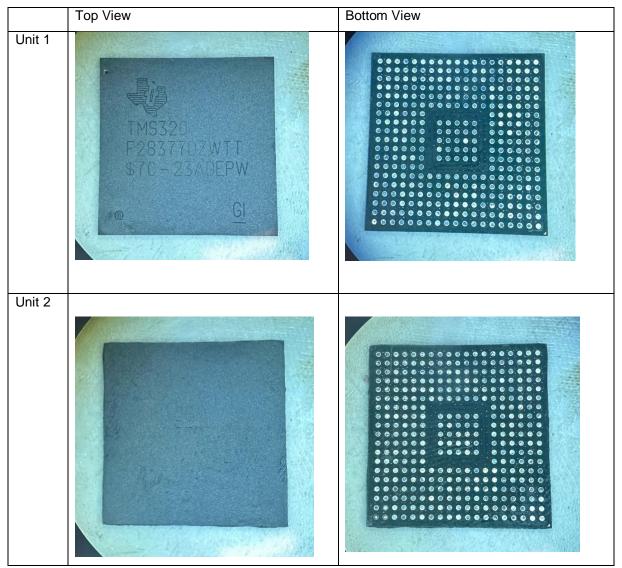
D4) DEFINE AND VERIFY ROOT CAUSE:

Failure Analysis Actions:

In order to determine root cause, failure analysis was conducted which included the following Failure Analysis methods:

• External Package Examination:

The returned unit was inspected under optical microscope. No anomaly was observed from external package.



TI Device: TMS320F28377DZWTT

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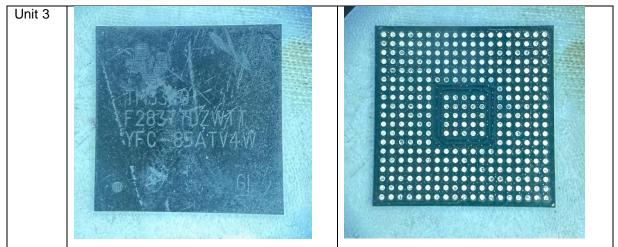
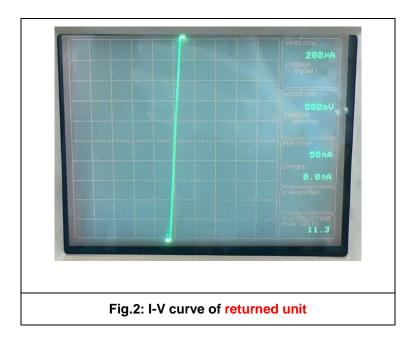


Fig.1: Optical view of the returned unit.

• Electrical Characterization:

Curve trace analysis was performed on the returned unit. Multiple pin short (GPIO16, VREFLOD, VDDA, VDDIO, VDD, GPIO57, GPIO139, X1) to VSS was verified.





• Signature Analysis:

Please refer to below previous FA results of customer return with similar pin short failure mode, Electrical Induced Physical Damage (EIPD) /EOS damage found. Here is the picture extracted from the report:

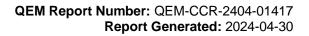
• Failure Isolation:

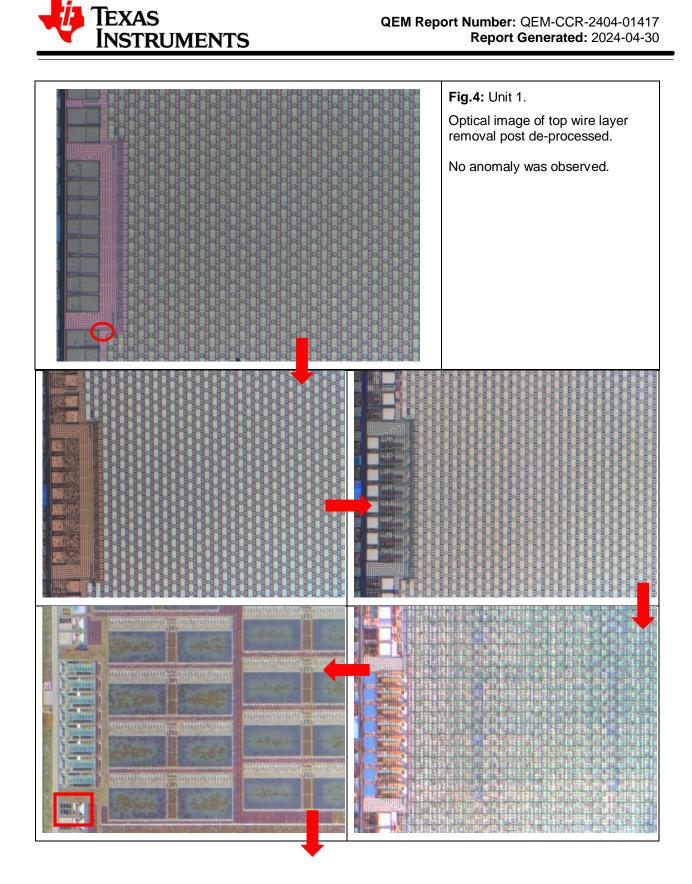
No visible damage or defect was observed at die surface on the failing unit 1. Hot spot was observed when performing failure isolation by Thermo isolation analysis.

Fig.3: Unit 1.
Thermo isolation analysis.
Hot spot (red part) at red arrow was observed.

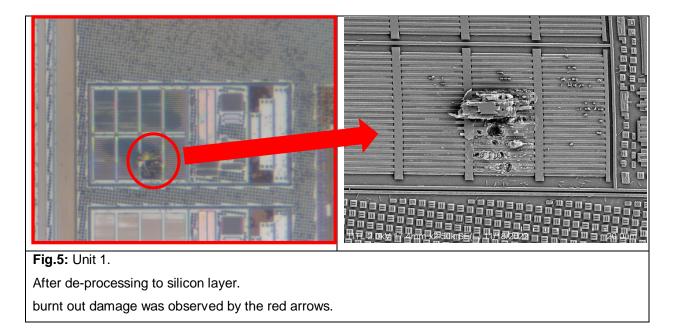
• De-processing and Visual:

The failing unit 1 was de-processed layer down to silicon. Electrically Induced Physical Damage (EIPD) in the form of burnt out damage was observed by de-processing.









• Conclusion:

The customer return unit was confirmed multiple pin short to VSS, TI electrical testing verified the issue and the root cause was determined to be most likely **Electrically Induced Physical Damage (EIPD)**, which is caused by some over-voltage or over-current condition or Electrical Overstress (EOS).

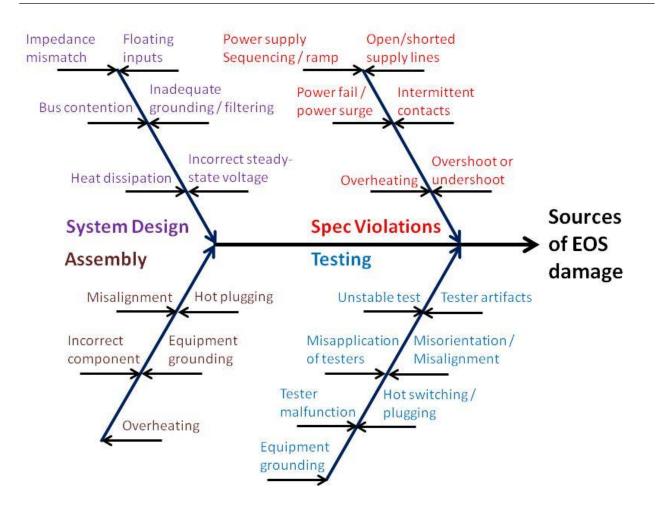
Per JEDEC document JEP155, which is available at <u>www.jedec.org</u>, an ESD-HBM (Electro-Static Discharge - Human Body Model) level of 500V means that "basic ESD control methods allow safe manufacturing with proven margin." Per JEDEC document JEP157, which is available at <u>www.jedec.org</u>, an ESD-CDM (Electro-Static Discharge - Charged Device Model) level of 250V means that "basic ESD control methods with grounding of metallic machine parts and control of insulators" allow safe manufacturing. Based on the above criteria from industry standard documents, the ESD qualification level of the failing pins, and the known industry manufacturing capability for ESD controls, component-level ESD is judged to not be a likely root cause.

Based on evidence obtained from failure analysis, Electrical Overstress (EOS) is the most likely cause of the Electrically Induced Physical Damage (EIPD).

In addition, based on the characteristics of this issue, a manufacturing non-conformance is judged to be unlikely.

Therefore, it appears probable that the customer reported issue was caused by EOS in the application environment, and TI recommends that the customer evaluate the application environment for sources of transient or steady-state Electrical Overstress. Detailed analysis and measurement of the customer's board environment and the customer's test environment will be required to identify the specific cause of EOS. Please consult the below fishbone diagram for a listing of such possible causes.





D5) DEFINE AND IMPLEMENT CORRECTIVE ACTIONS:

It is recommended that the customer evaluate the possible causes of EOS in the application environment based on the above fishbone diagram.

D6) VALIDATE CORRECTIVE ACTIONS:

The above-listed causes have been observed to be possible causes of EOS and – when properly guarded against – can effectively eliminate sources of EOS.

D7) PREVENT RECURRENCE AND IMPROVE QUALITY SYSTEM:

The customer has been informed of the possible conditions that could lead to the confirmed EIPD. It is recommended that the following best practices be incorporated into board / system assembly and test flows and board / system design to avoid future cases of EOS.

Application Parameters

 Perform measurements of the application system, both under operating conditions and under testing conditions:



- Confirm application complies with all Absolute Maximum Ratings and Recommended Operating Conditions in the datasheet (including voltage, current, timing, and temperature measurements);
- Confirm power sequencing datasheet requirements are followed for each device in the application;
- o Confirm datasheet ramp rate requirements are followed for each device in the application;
- Confirm that nodes on the board are operating at the intended voltage;
 - Specifically, confirm that pairs of nodes that are intended to be at the same potential are at the same potential;
- Confirm power supply lines and signal lines are free of excessive noise;
- Confirm power supply lines and signal lines are free of voltage spikes (positive or negative).

Test Flow

- Avoid hot switching:
 - Only connect / disconnect board-under-test when power is off;
 - Ensure bypass capacitors are fully discharged before disconnecting board-under-test;
 - Make sure relays and switches are connected / disconnected only when power is completely off;
 - Avoid hot switching between tests:
 - Do not change voltage values or current ranges while the power supply is connected or on;
 - Do not turn off supplies between tests without allowing enough time for capacitors to discharge before starting the next test;
 - Do not use spring-loaded contacts that are at different heights, which could cause connection to any live supplies with undetermined sequences.
- Include voltage / current clamps to safeguard against datasheet violations.
- Manage test procedures:
 - Follow documented release process for test programs / procedures;
 - Audit test programs / procedures before release;
 - Maintain test programs / procedures under revision control.

Test equipment

- Prevent poorly connected, misaligned, and rotated test connections:
 - o Confirm mechanical safeguards exist to prevent accidental disconnect during test;
 - Use connectors that only permit one-way orientation.
- Ensure that equipment has adequate grounding;
- Ensure that power sources are adequately conditioned / filtered;
- Follow regular schedule of diagnostics, maintenance, and calibration;
- Ensure that test equipment meets testing and safety requirements;
- Properly route and shield all sources of electrical energy;
- Shield board-under-test from mechanical hazards.

Assembly Flow

- Prevent poorly connected, misaligned, and rotated components
 - Use x-ray and/or optical inspection equipment;
 - Place markers in silk screen to show proper device polarity / orientation;
 - Use connectors that only permit one-way orientation.

System Design

• Place electrical filters as close as possible to the device where the protection is needed;



- Select and place bypass capacitors to optimize the power supply performance and avoid unwanted resonance;
- Use well-regulated power supplies appropriate to the design;
- Use power supplies with overvoltage protection;
- Ensure voltage / current sources are capable of tolerating initial surge current;
- Ensure the design complies with all datasheet values, including power sequencing and ramp-rate requirements;
- If the system is designed for a hot-plugging application (e.g., USB), ensure the design tolerates side effects of hot plugging, such as inrush current and voltage sag;
- Minimize inductance in power supply connections in order to minimize radiated and conducted emissions;
- Design power circuits to prevent backwards current flow;
- Minimize overshoot and undershoot by using appropriate clamping devices;
- Avoid contention between output drivers;
- Avoid floating inputs, even for unused pins (e.g., by using pull-up / pull-down resistors);
- Select proper connectors between boards;
- Ensure proper heat dissipation;
- Distribute total board impedance as uniformly as possible;
- Ensure power routes are capable of sourcing adequate currents;
- Ensure impedance match between transmission line and load;
- Avoid ground loops;
- Use ground shields along signal paths to minimize crosstalk effects;
- Minimize impedance between separate ground planes;
- Review corner cases in software and eliminate undefined cases;
- Include error handling routines in software.

D8) CLOSURE:

TI Report Approver	Role
Cindy Wu	FQE

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Appendix 2 (TI Abbreviations):

Abbreviation	Definition
, is all official	Eight Disciplines (8Ds) Problem Solving is a method developed at Ford Motor Company used to approach and to resolve problems. Its purpose is to
8D	Eight beginne (constraints) in the second and the s
05	based on statistical analysis of the problem and on the origin of the problem by determining the root causes.
A/T	Assembly Test Site
A-B-A swap	The A-B-A swap method is used to investigate whether the observed issue is caused by non-TI part related aspects on the board.
ACO	Assembly County of Origin
AEO	Analog Engineering Operations
AFM	Atomic Force Microscope
AIZU	Ti internal abbreviation for TI Aizu, Japan Wafer Fab
APC	Advanced Process Control
ASO	Auvarieur Frocess Control
ATE	Automated Test Equipment or Final Test
ATSS	Assembly Test Spec System
Batch #	Manufacturing Batch = SAP Batch number
BICOM	Complementary Bi Polar
BCP	Business Continuity Program and Crisis Management
BOAC	Bond Over Active Circuit (BOAC)
C/T	Curve Tracer (C/T), a typical initial verification analysis measurement equipment for voltage vs. current curves
CA	Corrective action (CA): the action taken to help eliminate the root cause
CAPA	Corrective Action & Preventive Action
Carrier	Carrier is a pocket tape, tray, tube, or other fixture used to store and transport devices and components.
CCO	Chip County of Origin
CDA	Code for TI Chengdu, China Assembly Site
CDA	Compressed Dry Air
CDM	Charged Device Model (an ESD Test)
CFAB	TI internal abbreviation for TI Chengdu, China Wafer Fab
CIP	Continuous Improvement Process
CLARK	TI internal abbreviation for TI Pampanga (Clark), Philippines A/T Site
CMP	Chemical Mechanical Polishing
CMS	Change Management System
COO	County of Origin
COP	Crystal Originated Particle(s)
COP	Customer Oriented Process
Cover Tape	Cover Tape is a clear or transparent tape
cpk	Capability Index-Centering
CPW	Chips Per Water
CQE	Customer Quality Engineer
CRCT	Customer Return Cycle Time
CRU	
	Customer Returned Unit
CSO	Chip Site of Origin
CT	Cold Temperature
CT, C/T	Cycle Time
CU3	Code for TI Chengdu, China Wafer Fab
CU6	
	Code for TI Malacca (Melaka), Malaysia A/T Site
CUA	Code for TI Maine (Portland), USA Wafer Fab
CV	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement
CV CVD	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition
CV CVD D/N	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note
CV CVD D/N DARC	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating
CV CVD D/N DARC DC	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week).
CV CVD D/N DARC DC DDAO	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab)
CV CVD D/N DARC DC DDAO Desiccant	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture.
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CV CVD D/N DARC DC DDAO Desiccant DFAB	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI internal abbreviation for TI Dallas, USA Wafer Fab DFAB
CV CVD D/N DARC DC DDAO Desiccant DFAB Die	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI internal abbreviation for TI Dallas, USA Wafer Fab DFAB During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a Die.
CV CVD D/N DARC DC DDAO Desiccant DFAB Die DIP	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI Internal abbreviation for TI Dallas, USA Wafer Fab DFAB During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a Die. Dual-In-Line Package Deionized Water
CV CVD D/N DARC DC DDAO Desiccant DFAB Die DIP DIP DIW DLN	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI internal abbreviation for TI Dallas, USA Wafer Fab DFAB Dual-In-Line Package Deionized Water Code for TI Dallas, USA Wafer Fab DFAB
CV CVD D/N DARC DC DDAO Desiccant DFAB Die DIP DIP DIW	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI Internal abbreviation for TI Dallas, USA Wafer Fab DFAB Dual-In-Line Package Deionized Water Code for TI Dallas, USA Wafer Fab DFAB Dielectric Anti-reflective Counce Dielective Stimulation (DLS) can be used for failure isolation of functional failures dependent on voltage, temperature, frequency,using TTL
CV CVD D/N DARC DC DDAO Desiccant DFAB Die DIP DIP DIW DLN DLS	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI Internal abbreviation for TI Dallas, USA Wafer Fab DFAB During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a Die. Dual-Line Package Deionized Water Code for TI Dallas, USA Wafer Fab DFAB Dynamic Laser Stimulation (DLS) can be used for failure isolation of functional failures dependent on voltage, temperature, frequency,using TTL input of XIVA.
CV CVD D/N DARC DDAC DDAO DEsiccant DFAB Die DIP DIP DIW DLN DLN DLS DM5	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI Internal abbreviation for TI Dallas, USA Wafer Fab DFAB During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a Die. Dual-In-Line Package Deionized Water Code for TI Dallas, USA Wafer Fab DFAB Dynamic Laser Stimulation (DLS) can be used for failure isolation of functional failures dependent on voltage, temperature, frequency,using TTL input of XIVA. Code for TI Dallas, USA Wafer Fab DMOS5
CV CVD D/N DARC DC DDAO Desiccant DFAB Die DIP DIP DIP DIP DLN DLN DLS DM5 DM6	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI internal abbreviation for TI Dallas, USA Wafer Fab DFAB During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a Die. Dual-In-Line Package Deionized Water Code for TI Dallas, USA Wafer Fab DFAB Dynamic Laser Stimulation (DLS) can be used for failure isolation of functional failures dependent on voltage, temperature, frequency,using TTL input of XIVA. Code for TI Dallas, USA Wafer Fab DMOS5 Code for TI Dallas, USA Wafer Fab DMOS5
CV CVD D/N DARC DC DDAO DEsiccant DFAB Die DIP DIW DLN DLN DLS DM5	Code for TI Maine (Portland), USA Wafer Fab Capacitance-Voltage Measurement Chemical Vapor Deposition Delivery Note Dielectric Anti-reflective Coating Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week). TI Dallas Device Analysis Organization (Lab) Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture. TI Internal abbreviation for TI Dallas, USA Wafer Fab DFAB During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a Die. Dual-In-Line Package Deionized Water Code for TI Dallas, USA Wafer Fab DFAB Dynamic Laser Stimulation (DLS) can be used for failure isolation of functional failures dependent on voltage, temperature, frequency,using TTL input of XIVA. Code for TI Dallas, USA Wafer Fab DMOS5

TI Information – Selective Disclosure



Open International Design Park Mission DF Design Textor DF Estimation Textor DF Estimation Textor DF Estimation	Abbreviation	Definition
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BMU Obsep 101 Status DCM Explaneting Charge Mok EELS Explaneting Charge Mok EMM Explaneting Charge Mok ESD Explaneting Charge Mok ESD <td></td> <td></td>		
ECN Ensertial Councy Book Editation Councy Book Expension ELS Expension		
ECU Electrical Course Unit Encryp Engress Area Spectroscopy (EDX) Encryp Engress Area Spectroscopy (EDX) Electroscop Targers Area Spectroscopy Exact Targers Area Spectroscopy Exact Targers Area Spectroscopy Electroscop Elect		
EXX Energy Dispersion X-ray Spectroscopy (EXX) EE Explanes Enginetics EX Explanes Enginetics EX Explanes Enginetics EV Explanes Enginetics EV Explanes Enginetics EV Explanes Enginetics EV Explanes Enginetics EVA Explanes Enginetics EVA </td <td></td> <td></td>		
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MES Manufacturing Execution System MEX Code for TI Aguascalientes, Mexico A/T Site (FMX)		
MEX Code for TI Aguascalientes, Mexico A/T Site (FMX)		
MFAB II internal abbreviation for II Main (Portland), USA Wafer Fab		
	MFAB	I Internal abbreviation for II Main (Portland), USA Wafer Fab

TI Information – Selective Disclosure



Number Main Factor, Provi MPT Main Factor, Prove MMT Main Factor, Prove MMT Main Factor, Prove MMT Main Factor, Prove Marcon, Main Factor, Prove MMT Main Factor, Prove Main Factor, Pr	Abbreviation	Definition
IMP Main Factor, Four MG Manufactoria MG Manufactoria MG Costs for TMine, Aspen Wards Tab (* 190m) MHB Costs for TMine, Aspen Wards Tab (* 190m) MHB Costs for TMine, Aspen Wards Tab (* 190m) MHB Costs for TAble, Aspen Wards Tab (* 190m) MHD Main Factoria MHA Costs for TAble, Langer, Mangua AT Six MAL Costs for TAble, Langer, Mangua AT Six MG Main Factoria MGS Main Factoria MG Main		
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MLO Multiple layer MA Manufacturing Autoring Consultation MA Manufacturing Autoring Consultation MASSET Model Statuting Consultation Technology I MASSET Model Statuting Consultation MASSET Model Statuting Consultation MARS Notation Marka Conde Statuting Consultation MARS Notation Marka Conde Statuting Consultation MARS Notation Marka Conde Statuting Consultation MARS Open Technological statuping Consultation MARS Notation Marka Conde Statuping Consultation MARS Open Technological statuping Consultation MARS Opent Technological statuping Consu		
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RT Room Temperature		
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TI Information – Selective Disclosure



Abbreviation	Definition
RTM	Release to market
RTO	Rapid Thermal Oxidation
RTP	Rapid Thermal Processing
RTV	Ramp to Volume
SACVD	Sub-Atmospheric Chemical - Vapor Deposition
SAM	Scanning Acoustic Microscopy; using ultrasonic waves to check for delamination.
SBE	Strategic Business Entity
SCI	Sub Collector Implant
SCM	Scanning Capacitance Microscopy
SCR	Standard Change Request
Scribe Line	Thin non-functional spacing is between neighboring Dies on a wafer where a saw can safely cut the wafer without damaging the circuits.
SD	Source-Drain (NSD,PSD)
SEM	Scanning Electron Microscope; imaging defects / damages beyond the resolution of an optical microscope
SFAB	Tl internal abbreviation for Tl Sherman, USA Wafer Fab
SFC ShDAO	Statistical Factory Control TI Shanghai Device Analysis Organization (Lab)
SHE	Code for TI Sheman, USA Wafer Fab
Shelf Life	Length of time that a Ti part may be stored in controlled environment before mounted onto applications.
SIMS	Secondary lon Mass Spectroscopy
SMC	Statistic Machine Control or Scribe line Monitoring Chip
SMD	Surface Mount Device
SMIF	Standard Mechanical Interface
sMPY	Standardized Multiprobe Yield
SMS	Semiconductor Manufacturing System
SO	Sales Order
SOF	State of Finish
SOG	Spin on Glass
SPC	Statistical Process Control
SRP	Spreading Resistance Probe
SS	Sample Size
STC	Unique tracking number on the TI label (1T) for each shipping container.
STI	Shallow Trench isolation
STM	Scanning Tunneling Microscope (Microscopy)
SVDAO	TI Santa Clara Device Analysis Organization (Lab)
SWR T&R	Special Work Request The tape-and-reel (T&R) configuration is used for transport and storage
TAI	Code for TI Taiwan A/T Site
tbd	To be done / defined
TCI	Test Coverage Issue/Improvement
TDAO	TI Tucson Device Analysis Organization (Lab)
TDBD	Time to Dielectric Breakdown
TEM	Transmission Electron Microscope
TFR	Thin Film Resistor
TICL	TI internal abbreviation for TI Pampanga (Clark), Philippines A/T Site
TID	TI Freising, Germany Wafer Fab
TID	Code for Texas Instruments Deutschland
TIEM	TI internal abbreviation for TI Malacca (Melaka), Malaysia A/T Site
TIM	TI internal abbreviation for TI Kuala Lumpur, Malaysia A/T Site
TIMS	Tool Interdiction and Monitoring System Therein the second s
TIPI	Tl internal abbreviation for Tl Baguio, Philippines A/T Site
	TI internal abbreviation for TI Taiwan A/T Site Code for Texas Instruments Warrenville
TMG	Code for Texas instruments waterthile Technology and Manufacturing Group
TMX	Thintenay and Manufacturing Group Contents, Mexico A/T Site (FMX)
TNI	Trouble Not Identified; TI's investigation does not confirm the customer problem.
UPW	Ultra-Pure water
V/I	Voltage (V) vs. Current (I) verification
Via-n	Connection between Metal Levels n and n+1
VPD	Vapor Phase Decomposition
VPO	Versaport Pod Opener
VTN	Voltage Threshold N
VTP	Voltage Threshold P
W/F	Wafer Fab
WEE	Wafer Edge Exposure
WIC	Workplace Inventory Control
WIP	Work In Process
WLP	Wafer Level Package
WLR XIVA (LSIM)	Wafer Level Reliability
	Laser Signal Injection Microscopy (LSIM) is a current sensing technique Externally Induced Voltage Alterations Electromagnetic radiation that differentially penetrates structures and creates images of these structures on photographic film or a fluorescent screen.
X-RAY	Electomagnetic raciation that onlinetimating perietrates structures and creates images or these structures on photographic time or a nucleoscent screen. These images are called diagnostic x rays.
YE	Yield Enhancement