FINAL 8D REPORT

2024-09-29 – Rev. A

QEM-CCR-2409-00926
[CGD-2021070301 /]

Chengdu CRP Robot Technology Co., Ltd.

TI Device: TMS320F28377DZWTT

Customer Name:	Chengdu CRP Robot Technology Co., Ltd.	**Customer Contact:**	Chen Hui
Customer Site:		**End Customer**	CHENGDU CRP ROBOT TECHNOLOGY CO., LTD.
Event Type / Origin of Detection:	Field Failure [mile / km]	**Customer Contact(s) E-mail:**	chenhui@crprobot.com
Customer Production Date:			
Customer P/N:			
RMA# / SCAR#	CGD-2021070301	**TI P/N or Device Type:**	TMS320F28377DZWTT
Customer Tracking:		**TI QEM Event:**	QEM-CCR-2409-00926
Quantity of Received Unit(s):	3	**Unit Receive Date:**	2024-09-26
Customer Notification Date:	2024-09-18	**Current Action:**	

EXECUTIVE SUMMARY:

TI received **3** unit(s) of TI PN: **TMS320F28377DZWTT** (Customer P/N:) with customer provided issue description in Customer Issue Description.

TI analysis verified the issue: Electrically Induced Physical Damage (EIPD) was confirmed, and the cause was judged to be **Electrical Overstress (EOS).**

Note: Abbreviations used in this report are listed in Appendix 2.

D1) TEAM MEMBERS:

TI Team Members	Process Role	Email
Cindy Wu	Event Owner	cindy-wu@ti.com

D2) DESCRIPTION OF NONCONFORMITY:

Identification of TI's Material						
TI Part Number:	TMS320F28377DZWTT					
Unit ID	**Customer Unit ID**	**LTC**	**Assembly Lot #**	**Assembly Site**	**Fab Lot #**	**Fab Site**
1		23ADEPW	2150686PHI	PHI	SPR1M	UMI
2		23ADEYW	2119541PHI	PHI	SPR1M	UMI
3		85ATV4W	8280853WCW	WAA	8019199	

The following customer provided issue description was extracted from the information submitted by the customer with the returned TI device and was entered into TI's Quality Event Management System (QEM):

Customer Issue Description:

Customer reported issue at: **Field Failure [mile / km]**

Issue type: Electrical | Issue type details: After the completion of the production assembly TMS320F28377DZWTT normal operation for a period of time (a year, a few months), there is a program that does not run. As a rule of thumb, we first examined the crystal oscillator (a passive crystal oscillator) and found that it did not oscillate.
While troubleshooting multiple problematic boards, we encountered the following:
1. When trying to use the oscilloscope to observe whether the crystal oscillator is working, just touch the load capacitor with the oscilloscope probe, and the board will start to work normally, and the program will run as expected. This is the case with some boards.
2. On the circuit board in question, using the BGA rework station heating chip will also cause the circuit board to work normally and the program to run as expected. When the high temperature is 12 hours later, it is abnormal.
3. By replacing the new crystal oscillator or alternating the crystal oscillator, it is still found that the crystal oscillator does not oscillate.
4. After replacing the TMS320F28377DZWTT chip, the board functions normally.
6. After exchanging and soldering the abnormal chip with the normal chip, it is found that the fault follows the chip.
7. Under high temperature conditions (about 55?C), the failure rate increases significantly.
8. After power failure, the normal chip measurement: the resistance of X1 and GND is about 16.6M, and the resistance of abnormal: X1 and GND is about 330k.
9.On the circuit of the chip, it is still in an abnormal state after a 2 - megohm resistor is connected in parallel between X1 and X2. After increasing the resistance to 5 megohms, it returns to normal. However, it becomes abnormal again after running at a high temperature for 2 - 3 hours.
10. When the capacitors on X1 and X2 are replaced with 18 picofarads and 22 picofarads respectively, the crystal oscillator still cannot start oscillating. After replacing the capacitors with 8 picofarads and 12 picofarads, the crystal oscillator starts oscillating and the chip runs normally. But it becomes abnormal again after running at a high temperature for 2 - 3 hours.
11. After the capacitance is restored to 12P and 15p, the chip is normal again, and it is abnormal again after about a few minutes.
12.Later we found that the normal operation that could have been restored with a brief touch of the chip with an oscilloscope or multimeter probe is no longer restored, or more difficult to recover
13.After discovering that briefly touching the chip with an oscilloscope or multimeter probe did not restore normal operation, we left the chip for some time. As of today, the chip still does not return to normal operation. Additionally, the resistance between X1 and GND has changed from 330 k? to 3.3 k?. |
Summary: 1.Provide clear photos of the top and bottom markings of the suspected device, as well as photos of the TI label affixed to the original shipping carton/box/bag or reel.
2.We have cumulatively used 31,244 pieces of the TMS320F28377DZWTT chip. There are about 50 pieces with actual failures. These failures are not early field failures (EFFA). They all suddenly fail after a period of normal use (one year or a few months).
3.If the device has experienced EIPD, it is hoped that further failure analysis can be carried out.

TI Issue Description:

- **Physical Verification Results**

Units	Pass/Fail	Description
1	Pass	No anomaly from external package

Units	Pass/Fail	Description
2	Pass	No anomaly from external package
3	Pass	No anomaly from external package

- **Curve Trace Verification Results**

Units	Pass/Fail	Description
1	Fail	Multiple pin short to VSS
2	Fail	Multiple pin short to VSS
3	Fail	Multiple pin short to VSS

D3) IMPLEMENT AND VERIFY CONTAINMENT ACTIONS:

TI maintains an ongoing record of returns by lot number to track the number of returned TI devices for a single manufacturing lot.

TI has reviewed the return history for this unit's manufacturing lot and has not found evidence that this unit represents a sample of a larger, systemic issue with this particular production lot. Consequently, TI did not implement any additional containment actions for this production lot during initial investigation of the customer return.

The Lot Trace Code (LTC) and manufacturing date are listed below:

Units	Manufacture Date
1	03/2022
2	03/2022
3	05/2018

Containment Actions Description	Owner(s)	Date
1. Review the return history of wafer fab lot(s) **SPR1M** **8019199** • **Results:** The customer return history for this fab lot(s) did not indicate an abnormal risk for the customer reported issue on the returned unit.	TI	2024-09-26
2. Review the lot history incl. test yield performance of assembly lot(s) **2150686PHI** **8280853WCW** • **Results:** No abnormalities were noted in the assembly lot(s) history that would indicate a systemic issue exists with this lot.	TI	2024-09-26

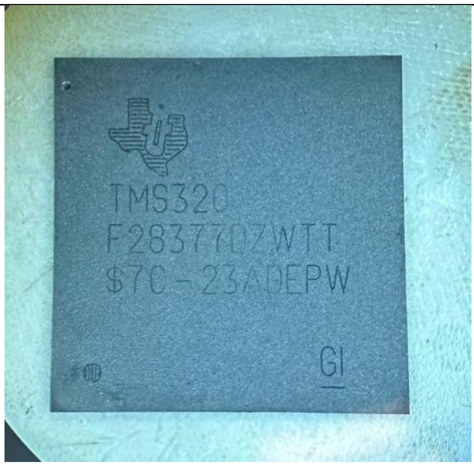
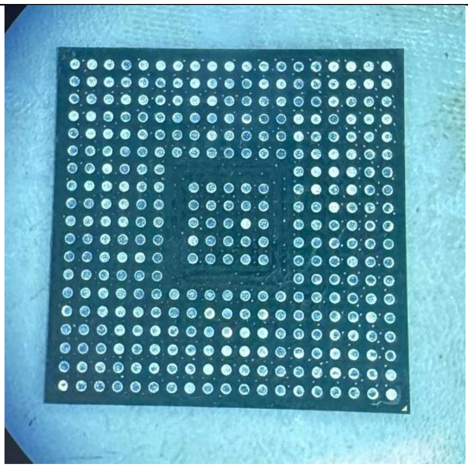
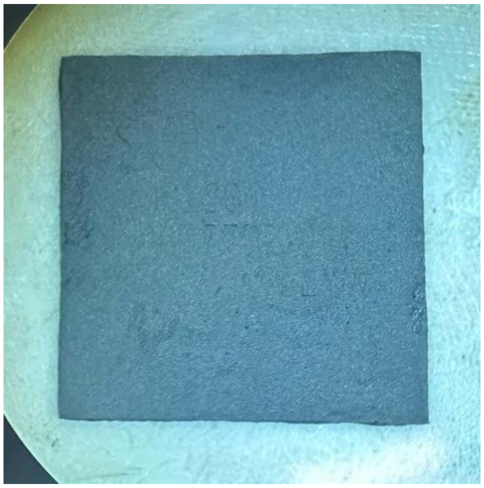
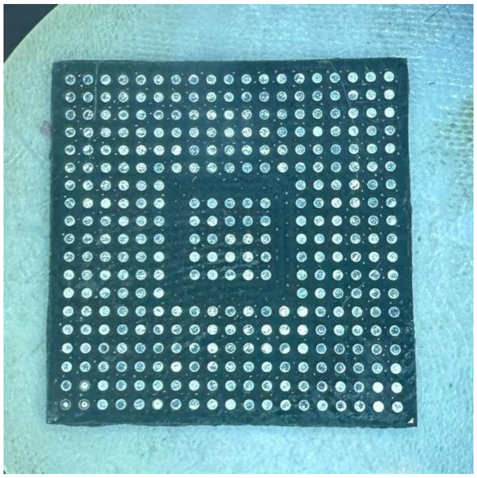
D4) DEFINE AND VERIFY ROOT CAUSE:

Failure Analysis Actions:

In order to determine root cause, failure analysis was conducted which included the following Failure Analysis methods:

- **External Package Examination:**

  The returned unit was inspected under optical microscope. No anomaly was observed from external package.

	Top View	Bottom View
Unit 1		
Unit 2		

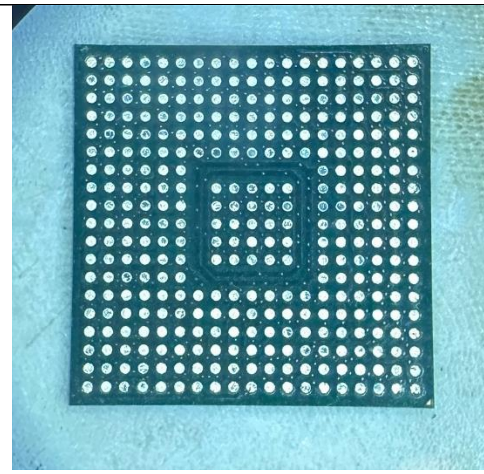
Unit 3		

Fig.1: Optical view of the returned unit.

- **Electrical Characterization:**

  Curve trace analysis was performed on the returned unit. Multiple pin short (GPIO16, VREFLOD, VDDA, VDDIO, VDD, GPIO57, GPIO139, X1) to VSS was verified.

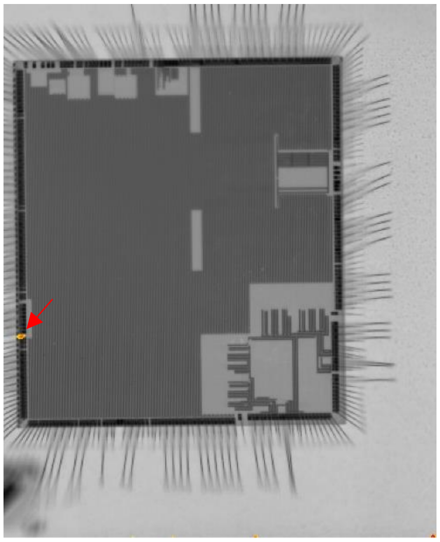
Fig.2: I-V curve of returned unit

- **Signature Analysis:**

Please refer to below previous FA results of customer return with similar pin short failure mode, Electrical Induced Physical Damage (EIPD) /EOS damage found. Here is the picture extracted from the report:

- **Failure Isolation:**

No visible damage or defect was observed at die surface on the failing unit 1. Hot spot was observed when performing failure isolation by Thermo isolation analysis.

	**Fig.3:** Unit 1. Thermo isolation analysis. Hot spot (red part) at red arrow was observed.

- **De-processing and Visual:**

The failing unit 1 was de-processed layer down to silicon. Electrically Induced Physical Damage (EIPD) in the form of burnt out damage was observed by de-processing.

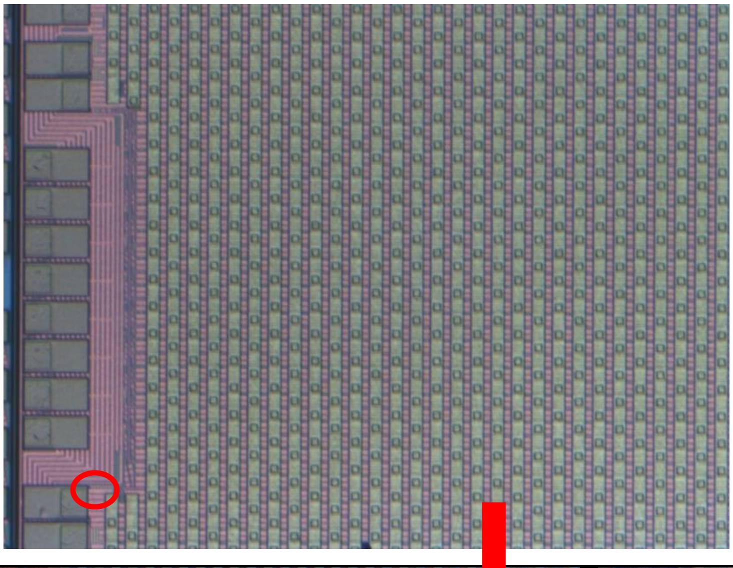
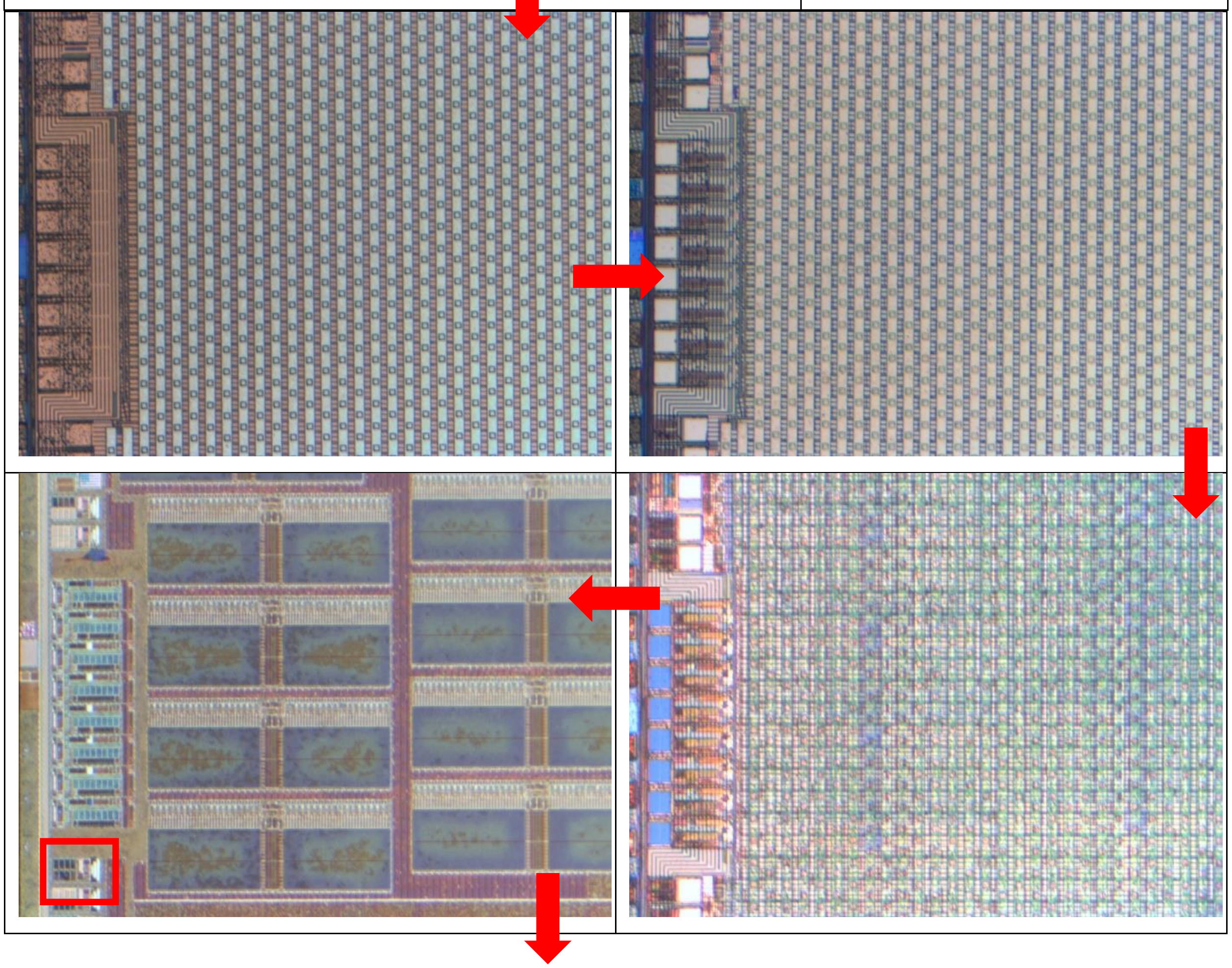


Fig.4: Unit 1.

Optical image of top wire layer removal post de-processed.

No anomaly was observed.



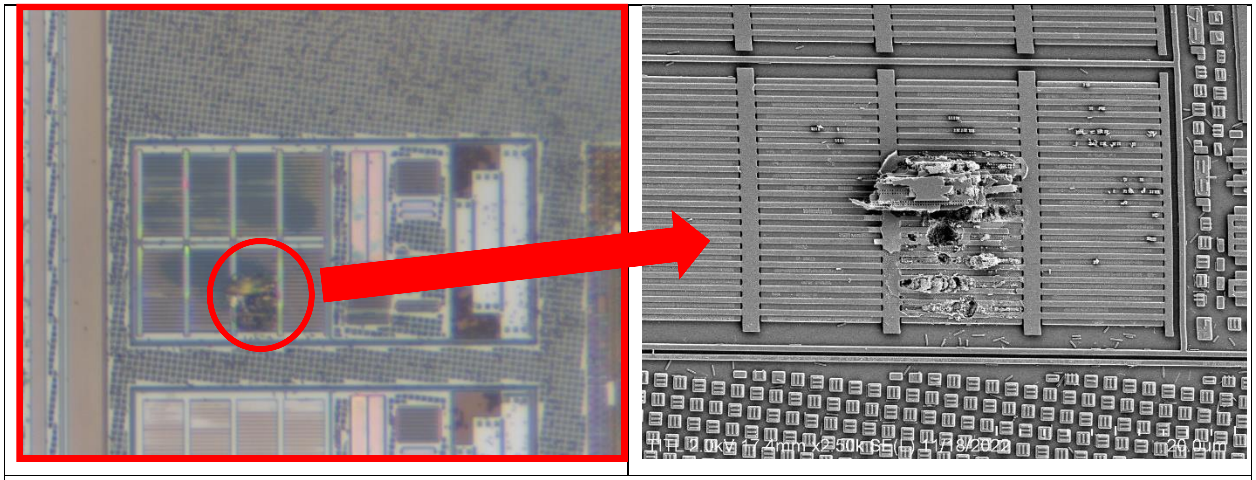


Fig.5: Unit 1.

After de-processing to silicon layer.

burnt out damage was observed by the red arrows.

- **Conclusion:**

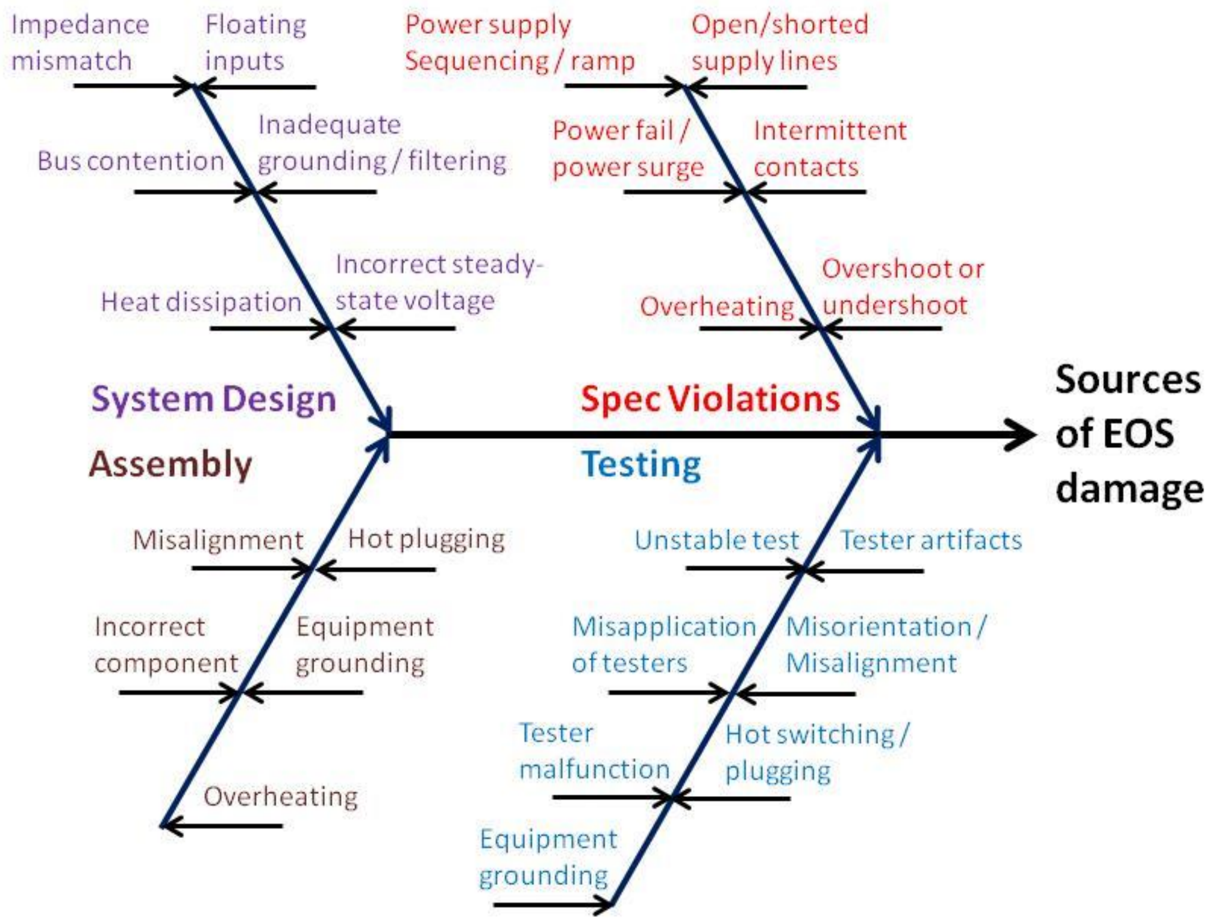
The customer return unit was confirmed multiple pin short to VSS, TI electrical testing verified the issue and the root cause was determined to be most likely **Electrically Induced Physical Damage (EIPD)**, which is caused by some over-voltage or over-current condition or Electrical Overstress (EOS).

Per JEDEC document JEP155, which is available at www.jedec.org, an ESD-HBM (Electro-Static Discharge - Human Body Model) level of 500V means that "basic ESD control methods allow safe manufacturing with proven margin." Per JEDEC document JEP157, which is available at www.jedec.org, an ESD-CDM (Electro-Static Discharge - Charged Device Model) level of 250V means that "basic ESD control methods with grounding of metallic machine parts and control of insulators" allow safe manufacturing. Based on the above criteria from industry standard documents, the ESD qualification level of the failing pins, and the known industry manufacturing capability for ESD controls, component-level ESD is judged to not be a likely root cause.

Based on evidence obtained from failure analysis, Electrical Overstress (EOS) is the most likely cause of the Electrically Induced Physical Damage (EIPD).

In addition, based on the characteristics of this issue, a manufacturing non-conformance is judged to be unlikely.

Therefore, it appears probable that the customer reported issue was caused by EOS in the application environment, and TI recommends that the customer evaluate the application environment for sources of transient or steady-state Electrical Overstress. Detailed analysis and measurement of the customer's board environment and the customer's test environment will be required to identify the specific cause of EOS. Please consult the below fishbone diagram for a listing of such possible causes.



D5) DEFINE AND IMPLEMENT CORRECTIVE ACTIONS:

It is recommended that the customer evaluate the possible causes of EOS in the application environment based on the above fishbone diagram.

D6) VALIDATE CORRECTIVE ACTIONS:

The above-listed causes have been observed to be possible causes of EOS and – when properly guarded against – can effectively eliminate sources of EOS.

D7) PREVENT RECURRENCE AND IMPROVE QUALITY SYSTEM:

The customer has been informed of the possible conditions that could lead to the confirmed EIPD. It is recommended that the following best practices be incorporated into board / system assembly and test flows and board / system design to avoid future cases of EOS.

Application Parameters

- Perform measurements of the application system, both under operating conditions and under testing conditions:

  - Confirm application complies with all Absolute Maximum Ratings and Recommended Operating Conditions in the datasheet (including voltage, current, timing, and temperature measurements);
  - Confirm power sequencing datasheet requirements are followed for each device in the application;
  - Confirm datasheet ramp rate requirements are followed for each device in the application;
  - Confirm that nodes on the board are operating at the intended voltage;
    - Specifically, confirm that pairs of nodes that are intended to be at the same potential are at the same potential;
  - Confirm power supply lines and signal lines are free of excessive noise;
  - Confirm power supply lines and signal lines are free of voltage spikes (positive or negative).

<u>Test Flow</u>

- Avoid hot switching:
  - Only connect / disconnect board-under-test when power is off;
  - Ensure bypass capacitors are fully discharged before disconnecting board-under-test;
  - Make sure relays and switches are connected / disconnected only when power is completely off;
  - Avoid hot switching between tests:
    - Do not change voltage values or current ranges while the power supply is connected or on;
    - Do not turn off supplies between tests without allowing enough time for capacitors to discharge before starting the next test;
    - Do not use spring-loaded contacts that are at different heights, which could cause connection to any live supplies with undetermined sequences.
- Include voltage / current clamps to safeguard against datasheet violations.
- Manage test procedures:
  - Follow documented release process for test programs / procedures;
  - Audit test programs / procedures before release;
  - Maintain test programs / procedures under revision control.

<u>Test equipment</u>

- Prevent poorly connected, misaligned, and rotated test connections:
  - Confirm mechanical safeguards exist to prevent accidental disconnect during test;
  - Use connectors that only permit one-way orientation.
- Ensure that equipment has adequate grounding;
- Ensure that power sources are adequately conditioned / filtered;
- Follow regular schedule of diagnostics, maintenance, and calibration;
- Ensure that test equipment meets testing and safety requirements;
- Properly route and shield all sources of electrical energy;
- Shield board-under-test from mechanical hazards.

<u>Assembly Flow</u>

- Prevent poorly connected, misaligned, and rotated components
  - Use x-ray and/or optical inspection equipment;
  - Place markers in silk screen to show proper device polarity / orientation;
  - Use connectors that only permit one-way orientation.

<u>System Design</u>

- Place electrical filters as close as possible to the device where the protection is needed;

- Select and place bypass capacitors to optimize the power supply performance and avoid unwanted resonance;
- Use well-regulated power supplies appropriate to the design;
- Use power supplies with overvoltage protection;
- Ensure voltage / current sources are capable of tolerating initial surge current;
- Ensure the design complies with all datasheet values, including power sequencing and ramp-rate requirements;
- If the system is designed for a hot-plugging application (e.g., USB), ensure the design tolerates side effects of hot plugging, such as inrush current and voltage sag;
- Minimize inductance in power supply connections in order to minimize radiated and conducted emissions;
- Design power circuits to prevent backwards current flow;
- Minimize overshoot and undershoot by using appropriate clamping devices;
- Avoid contention between output drivers;
- Avoid floating inputs, even for unused pins (e.g., by using pull-up / pull-down resistors);
- Select proper connectors between boards;
- Ensure proper heat dissipation;
- Distribute total board impedance as uniformly as possible;
- Ensure power routes are capable of sourcing adequate currents;
- Ensure impedance match between transmission line and load;
- Avoid ground loops;
- Use ground shields along signal paths to minimize crosstalk effects;
- Minimize impedance between separate ground planes;
- Review corner cases in software and eliminate undefined cases;
- Include error handling routines in software.

D8) CLOSURE:

TI Report Approver	Role
Cindy Wu	FQE

Appendix 1 (TI Notice and Disclaimer):

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Appendix 2 (TI Abbreviations):

Abbreviation	Definition
8D	Eight Disciplines (8Ds) Problem Solving is a method developed at Ford Motor Company used to approach and to resolve problems. Its purpose is to identify, correct, and eliminate recurring problems, and it is focused on product and process improvement. It establishes a permanent corrective action based on statistical analysis of the problem and on the origin of the problem by determining the root causes.
A/T	Assembly Test Site
A-B-A swap	The A-B-A swap method is used to investigate whether the observed issue is caused by non-TI part related aspects on the board.
ACO	Assembly County of Origin
AEO	Analog Engineering Operations
AFM	Atomic Force Microscope
AIZU	TI internal abbreviation for TI Aizu, Japan Wafer Fab
APC	Advanced Process Control
ASO	Assembly Site of Origin
ATE	Automated Test Equipment or Final Test
ATSS	Assembly Test Spec System
Batch #	Manufacturing Batch = SAP Batch number
BiCOM	Complementary Bi Polar
BCP	Business Continuity Program and Crisis Management
BOAC	Bond Over Active Circuit (BOAC)
C/T	Curve Tracer (C/T), a typical initial verification analysis measurement equipment for voltage vs. current curves
CA	Corrective action (CA): the action taken to help eliminate the root cause
CAPA	Corrective Action & Preventive Action
Carrier	Carrier is a pocket tape, tray, tube, or other fixture used to store and transport devices and components.
CCO	Chip County of Origin
CDA	Code for TI Chengdu, China Assembly Site
CDA	Compressed Dry Air
CDM	Charged Device Model (an ESD Test)
CFAB	TI internal abbreviation for TI Chengdu, China Wafer Fab
CIP	Continuous Improvement Process
CLARK	TI internal abbreviation for TI Pampanga (Clark), Philippines A/T Site
CMP	Chemical Mechanical Polishing
CMS	Change Management System
COO	County of Origin
COP	Crystal Originated Particle(s)
COP	Customer Oriented Process
Cover Tape	Cover Tape is a clear or transparent tape
cpk	Capability Index-Centering
CPW	Chips Per Wafer
CQE	Customer Quality Engineer
CRCT	Customer Return Cycle Time
CRU	Customer Returned Unit
CSO	Chip Site of Origin
CT	Cold Temperature
CT, C/T	Cycle Time
CU3	Code for TI Chengdu, China Wafer Fab
CU6	Code for TI Malacca (Melaka), Malaysia A/T Site
CUA	Code for TI Maine (Portland), USA Wafer Fab
CV	Capacitance-Voltage Measurement
CVD	Chemical Vapor Deposition
D/N	Delivery Note
DARC	Dielectric Anti-reflective Coating
DC	Datecode (D), typically shown on the TI box label in the format "YYWW" (year-year-week-week).
DDAO	TI Dallas Device Analysis Organization (Lab)
Desiccant	Desiccant is a moisture-adsorbing material placed inside sealed dry-pack bags to adsorb internal bag moisture.
DFAB	TI internal abbreviation for TI Dallas, USA Wafer Fab DFAB
Die	During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a Die.
DIP	Dual-In-Line Package
DIW	Deionized Water
DLN	Code for TI Dallas, USA Wafer Fab DFAB
DLS	Dynamic Laser Stimulation (DLS) can be used for failure isolation of functional failures dependent on voltage, temperature, frequency,….using TTL input of XIVA.
DM5	Code for TI Dallas, USA Wafer Fab DMOS5
DM6	Code for TI Dallas, USA Wafer Fab DMOS6
DMOS5	TI internal abbreviation for TI Dallas, USA Wafer Fab DMOS5
DMOS6	TI internal abbreviation for TI Dallas, USA Wafer Fab DMOS6
DOE	Design Of Experiment

Abbreviation	Definition
DPPM	Defects Parts per Million
DT	Deep Trench
DUF	Diffusion under film
DUT	Device Under Test
DUV	Deep UV - (Stabilization of Resist)
ECN	Engineering Change Note
ECU	Electrical Control Unit
EDX	Energy Dispersive X-ray Spectroscopy (EDX)
EE	Equipment Engineering
EELS	Electron Energy Loss Spectroscopy
EFA	Electrical Failure Analysis
EIPD	Electrically Induced Physical Damage
EM	Electromigration (void formation)
EM	External Manufacturing
EMEA	Europe Middle East and Africa (Sales Region)
EMMI (PEM)	Photon Emission Microscopy (EMMI / PEM) is a light sensing technique basically microscope with NIR objective lenses and a NIR detector
EOL	End of Life , same as Last Time Buy (LTB)
EOS	Electrical Overstress
EPI	Epitaxy
E-pin	Ejection Pin
ESD	Electrostatic Discharge
ESD	Estimated Shipping Date
ESDAQ	Enhanced Software Defect Analysis
ETA	Eagle Test Automatic Test system
EVM	Evaluation Module that allows users to evaluate the operation and performance of TI parts
FA	Failure Analysis
FCT	Functional Circuit Test
FDAO	TI Freising Device Analysis Organization (Lab)
FFAB	TI internal abbreviation for TI Freising, Germany Wafer Fab
FIB	Focused Ion Beam
FMEA	Failure Mode and Effects Analysis (FMEA)
FMX	TI internal abbreviation for TI Aguascalientes, Mexico A/T Site (FMX)
FQAE	Field Quality Application Engineer
FT	Final Test, usually the latest revision of the test program used in the A/T site.
FTIR	Fourier Transform Infrared Microscopy
FTY	Final Test Yield (after Packaging)
GEC	Good Electrical Chip
GF6	Code for TI Greenock, Scotland Wafer Fab (6" = 150mm)
GF8	Code for TI Greenock, Scotland Wafer Fab (8" = 200mm)
GFAB	TI internal abbreviation for TI Greenock, Scotland Wafer Fab
GOI	Gate Oxide Integrity
GRR	Gauge Reproducibility and Repeatability
GSP	Good Sample Probe
HBM	Human Body Model ESD Test
HCI	Hot Carrier Injection
HDP	High Density Plasma
HIC	Humidity Indicator Card
HT	High Temperature
HTO	High Temperature Oxide (oxidation)
HTOL	High Temperature Operating Life (an Reliability test)
HTSL	High Temp Storage Life (a Reliability test)
IC	Integrated Circuit
ICP	Inductively Coupled Plasma (Dry Etch)
ICPMS	Inductively Coupled Plasma Mass Spectroscopy
ICT	In-Circuit Test
ILD	Inter Level Dielectric
ILD-n	Inter Level Dielectric between Metal Levels n and n+1
ILO	Inter Level Oxide
IMD	Inter Metal Dielectric
IMDS	International Material Data System
IMPL	Implant
INQ	Inquiry
IPQC	In-Line Process control
IQC	Inline Quality Control
ITY	Integrated Test Yield
KGU	Known Good Unit
LBE	Local Business Entity
Lead-frame	Lead-frame insists as the interface area to the external terminals of the part.
LL	Lesson(s) Learned
LPCVD	Low Pressure Chemical-Vapor Deposition
LRR	Lot Reject Rate
LTB	Last Time Buy, same as End of Life (EOL)
LTC	Lot Trace Code; each TI part is marked with a unique LTC
LTO	Low Temperature Oxide (Oxidation)
MBB	Moisture Barrier Bag (MBB) or Dry Pack
MCLT	Minority Carrier Lifetime (TAU)
MCS	Metallurgic Cross-Section sample preparation is used to reveal the true component structure at a certain device location (e.g. solder joints, bond wire connection or die attach)
MDAO	TI Manchester Device Analysis Organization (Lab)
MEI	Manufacturing Equipment Installation
MES	Manufacturing Execution System
MEX	Code for TI Aguascalientes, Mexico A/T Site (FMX)
MFAB	TI internal abbreviation for TI Main (Portland), USA Wafer Fab

Abbreviation	Definition
MFC	Mass Flow Controller
MFF	Multi Factory Flow
MfG	Manufacturing
MH5	Code for TI Miho, Japan Wafer Fab (5")
MH6	Code for TI Miho, Japan Wafer Fab (6" = 150mm)
MH8	Code for TI Miho, Japan Wafer Fab (8" = 200mm)
MIF	TI internal abbreviation for TI Miho, Japan Assembly Site
MIHO	TI internal abbreviation for TI Miho, Japan Wafer Fab
MIM	Metal-Insulator-Metal
MLA	Code for TI Kuala Lumpur, Malaysia A/T Site
MLO	Multi-Level Oxide
MM	Manufacturing Maintenance
MOCVD	Metal-organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor Junction (Technology)
MOSFET	MOS Field Effect Transistor
MPY	Multiprobe Yield
MRB	Material Review Board
MSL	Moisture Sensitivity Level
NAC	TI will conduct a background check on the device to determine whether case monitoring is sufficient. A non-actionable case (NAC) is a direct result of this upfront background verification or physical analysis.
NMOS	N Channel Metal Oxide Semiconductor
NTF	No Trouble Found; TI could not verify the customer reported issue
NVA	Non-Value Added
O/S	Open / Shorts failures
OCAP	Out of Control Action Plan
OEE / OEU	Overall Equipment Efficiency / Overall Equipment Utilization
OFI	Opportunities For Improvement
OOC	Out of Control
OOS	Out of Spec
OPN	Operation
PA	Preventive action
Pb-free	a product that is rated RoHS & high temperature solderable (260°C) compatible.
PCD	Process Control Document
PCN	Process/Product Change Notification
PDC	Product Distribution Center (warehouse)
PDN	Product Discontinue Notification (EOL)
PE	Process Engineer(ing)
PECVD	Plasma Enhanced Chemical Vapor Deposition
PEM	Production Equipment Maintenance
PEM (EMMI)	Photon Emission Microscopy (EMMI / PEM) is a light sensing technique basically microscope with NIR objective lenses and a NIR detector
PFA	Physical Failure Analysis
PFMEA	Process Failure Mode and Effects Analysis
PHI	Code for TI Baguio, Philippines A/T Site
PI	Polyimide
Pitch	The distance from pin to pin or inter-lead spacing.
Pizza Box	Intermediate container for the fully loaded reel, carrier tape, and cover tape
PM	Preventive Maintenance
PMC	Process Monitoring Chip
PMD	Poly-Metal Dielectric(s)
PMOS	P Channel Metal Oxide Semiconductor
PO	Protective/Passivation Overcoating
PO	Purchase Order
POR	Process Of Record
PPAP	Production Part Approval Process (PPAP)
PPB	Parts Per Billion
PPM	Parts Per Million
PRM	Photo Resist Mask
PSD	P Implant Source/Drain
PSG	Phosphorous Silicate Glass
PSOG	Phosphorous Spin On Glass
PSW	Part Submission Warrant (PSW)
PTN	Product Termination Notification (PTN)
PVD	Physical Vapor Deposition
QA	Quality Assurance
QAB	Code for TI Pampanga (Clark), Philippines A/T Site
QBD	Charge to Breakdown
QBS	Qualification By Similarity
QC	Quality Control
QEM	Quality Event Manager system for 8D reports
QLT	Quality Leadership Team
QRA	Quality & Reliability Assurance
QSS	Quality System Standard
QST	Quality Steering Team
QTY	Quantity
RC	Root Cause
REB	Resist Etch Back
RFAB	TI internal abbreviation for TI Richardson, USA Wafer Fab
RFB	Code for TI Richardson, USA Wafer Fab
RoHS	Restriction of Hazardous Substances Directive 2002/95/EC
RPN	Risk Potential Number
RPPM	Returned Parts per Million
RT	Room Temperature
RTA	Rapid Thermal Anneal

Abbreviation	Definition
RTM	Release to market
RTO	Rapid Thermal Oxidation
RTP	Rapid Thermal Processing
RTV	Ramp to Volume
SACVD	Sub-Atmospheric Chemical - Vapor Deposition
SAM	Scanning Acoustic Microscopy; using ultrasonic waves to check for delamination.
SBE	Strategic Business Entity
SCI	Sub Collector Implant
SCM	Scanning Capacitance Microscopy
SCR	Standard Change Request
Scribe Line	Thin non-functional spacing is between neighboring Dies on a wafer where a saw can safely cut the wafer without damaging the circuits.
SD	Source-Drain (NSD,PSD)
SEM	Scanning Electron Microscope; imaging defects / damages beyond the resolution of an optical microscope
SFAB	TI internal abbreviation for TI Sherman, USA Wafer Fab
SFC	Statistical Factory Control
ShDAO	TI Shanghai Device Analysis Organization (Lab)
SHE	Code for TI Sherman, USA Wafer Fab
Shelf Life	Length of time that a TI part may be stored in controlled environment before mounted onto applications.
SIMS	Secondary Ion Mass Spectroscopy
SMC	Statistic Machine Control or Scribe line Monitoring Chip
SMD	Surface Mount Device
SMIF	Standard Mechanical Interface
sMPY	Standardized Multiprobe Yield
SMS	Semiconductor Manufacturing System
SO	Sales Order
SOF	State of Finish
SOG	Spin on Glass
SPC	Statistical Process Control
SRP	Spreading Resistance Probe
SS	Sample Size
STC	Unique tracking number on the TI label (1T) for each shipping container.
STI	Shallow Trench isolation
STM	Scanning Tunneling Microscope (Microscopy)
SVDAO	TI Santa Clara Device Analysis Organization (Lab)
SWR	Special Work Request
T&R	The tape-and-reel (T&R) configuration is used for transport and storage
TAI	Code for TI Taiwan A/T Site
tbd	To be done / defined
TCI	Test Coverage Issue/Improvement
TDAO	TI Tucson Device Analysis Organization (Lab)
TDBD	Time to Dielectric Breakdown
TEM	Transmission Electron Microscope
TFR	Thin Film Resistor
TICL	TI internal abbreviation for TI Pampanga (Clark), Philippines A/T Site
TID	TI Freising, Germany Wafer Fab
TID	Code for Texas Instruments Deutschland
TIEM	TI internal abbreviation for TI Malacca (Melaka), Malaysia A/T Site
TIM	TI internal abbreviation for TI Kuala Lumpur, Malaysia A/T Site
TIMS	Tool Interdiction and Monitoring System
TIPI	TI internal abbreviation for TI Baguio, Philippines A/T Site
TITL	TI internal abbreviation for TI Taiwan A/T Site
TIW	Code for Texas Instruments Warrenville
TMG	Technology and Manufacturing Group
TMX	TI internal abbreviation for TI Aguascalientes, Mexico A/T Site (FMX)
TNI	Trouble Not Identified; TI's investigation does not confirm the customer problem.
UPW	Ultra-Pure water
V/I	Voltage (V) vs. Current (I) verification
Via-n	Connection between Metal Levels n and n+1
VPD	Vapor Phase Decomposition
VPO	Versaport Pod Opener
VTN	Voltage Threshold N
VTP	Voltage Threshold P
W/F	Wafer Fab
WEE	Wafer Edge Exposure
WIC	Workplace Inventory Control
WIP	Work In Process
WLP	Wafer Level Package
WLR	Wafer Level Reliability
XIVA (LSIM)	Laser Signal Injection Microscopy (LSIM) is a current sensing technique Externally Induced Voltage Alterations
X-RAY	Electromagnetic radiation that differentially penetrates structures and creates images of these structures on photographic film or a fluorescent screen. These images are called diagnostic x rays.
YE	Yield Enhancement