I want to get ADC at this timing to reduce motor driver's switching noise.

Conditions
 - I am using EPWM1A for Interrupt handler of ADC conversion.(made from up-down count mode)
 - Motor driver's U , V, W signal are made for EPWM2A,4A & 7A.
   PWM is made from up-down count mode.
   (Motor driver IC is DRV8312)

Question
 1, According to the sample code, this is using up count mode. Is there sample code using up-down count mode.
 2, I think that EPWM1A (interrupt handler) and other EPWM2,4,7(U,V,W signals) are needs to be synchronized.
    To synchronize each EPWM, we are setting following resgister for EPWM 2,4,7. is this setting correct?

Figure 15-93. TBCTL Register

15	14	13	12	11	10	9	8
FREE_SOFT		PHSDIR		CLKDIV		HSPCLKDIV	
R/W-0h		R/W-0h		R/W-0h		R/W-1h	

7	6	5	4	3	2	1	0
HSPCLKDIV	SWFSYNC	SYNCOSEL		PRDLD	PHSEN	CTRMODE	
R/W-1h	R-0/W1S-0h	R/W-0h		R/W-0h	R/W-0h	R/W-3h	

5-4	SYNCOSEL	R/W	0h	Sync Output Select
				00: EPWMxSYNCI / SWFSYNC
				01: CTR = zero: Time-base counter equal to zero (TBCTR = 0x00)
				10: CTR = CMPB : Time-base counter equal to counter-compare B (TBCTR = CMPB)
				11: EPWMXSYNCO is defined by TBCTL2[SYNCOSELX] Reset type: SYSRSn

Bit	Field	Type	Reset	Description
2	PHSEN	R/W	0h	Counter Reg Load from Phase Reg Enable
				0: Do not load the time-base counter (TBCTR) from the time-base phase register (TBPHS)
				1: Allow Counter to be loaded from the Phase register (TBPHS) and shadow to active load events when an EPWMxSYNCI input signal occurs or a software-forced sync signal, see bit 6. Reset type: SYSRSn

3, Are there any constraint about count mode? For example, do synchronized EPWMs need to be in the same count mode?