Hi,

I am using TMS320F28379s C2000 series micro controller (Master) to interface SRAM 23LCV1024 (Slave) via SPI. I have configured the SPI in the FIFO mode as per the example code provided in the control suite, SPI Configuration are as follows controller is in master mode, Clock polarity to rising, clock phase is normal (0), data character length is 8 bit and bit rate is 500KHz have been configured.

I’m trying to write the 1 byte data - 111 (0x6F) to the NVRAM and to read the same from the NVRAM IC. But I’m not getting the data as expected 111 (0x6F) instead I’m getting as 255 (0xFF) always…! while checking the pulses of the SPI pins I’m getting the data from the Slave device(in MISO pin)

But the responded data is not fetched by MCU.. while checking in oscilloscope the below results were observed in below case 1 the pulse pattern found correct but in MCU read SPI memory 0xff is found always.

Whereas in case 2 the pulse pattern has breaks in clock pulses.

1. Is there any thing I’ve missed out in my code ?
2. And I’ve a doubt that do we need to check the RX Fifo status reg before receiving the data ?

Please find the attached code and the SPI pulse images & debug screen screen shots.

Write Query :

SPI\_write\_byte 1 = 0x02 //write command

SPI\_write\_byte 2 = 0x00 //Address\_1 (bit 27 - 16)

SPI\_write\_byte 3 = 0x13 //Address\_2 (bit 15 to 8)

SPI\_write\_byte 4 = 0x88 //Address\_3 (bit 7 to 0)

SPI\_write\_byte 5 = 0x6F //Write data

Read Query :

SPI\_write\_byte 1 = 0x03 //Read command

SPI\_write\_byte 2 = 0x00 //Address\_1 (bit 27 - 16)

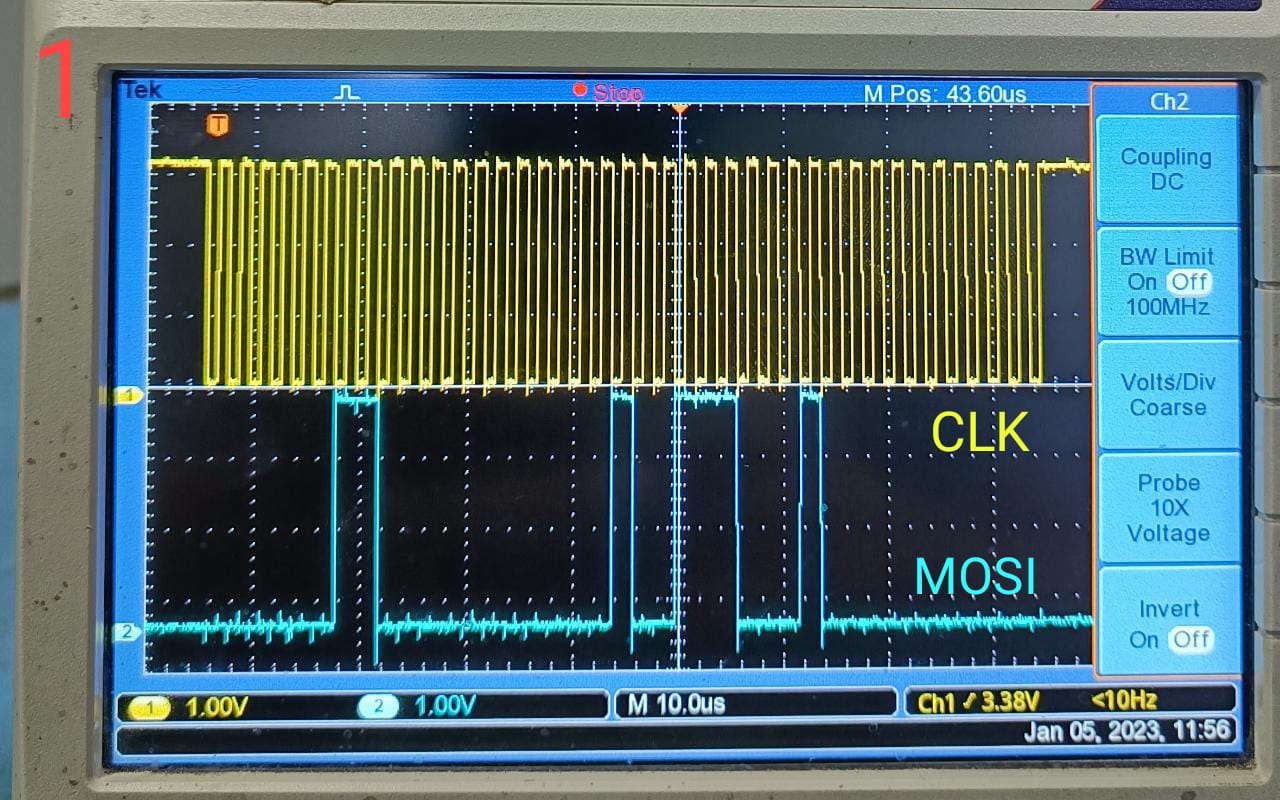
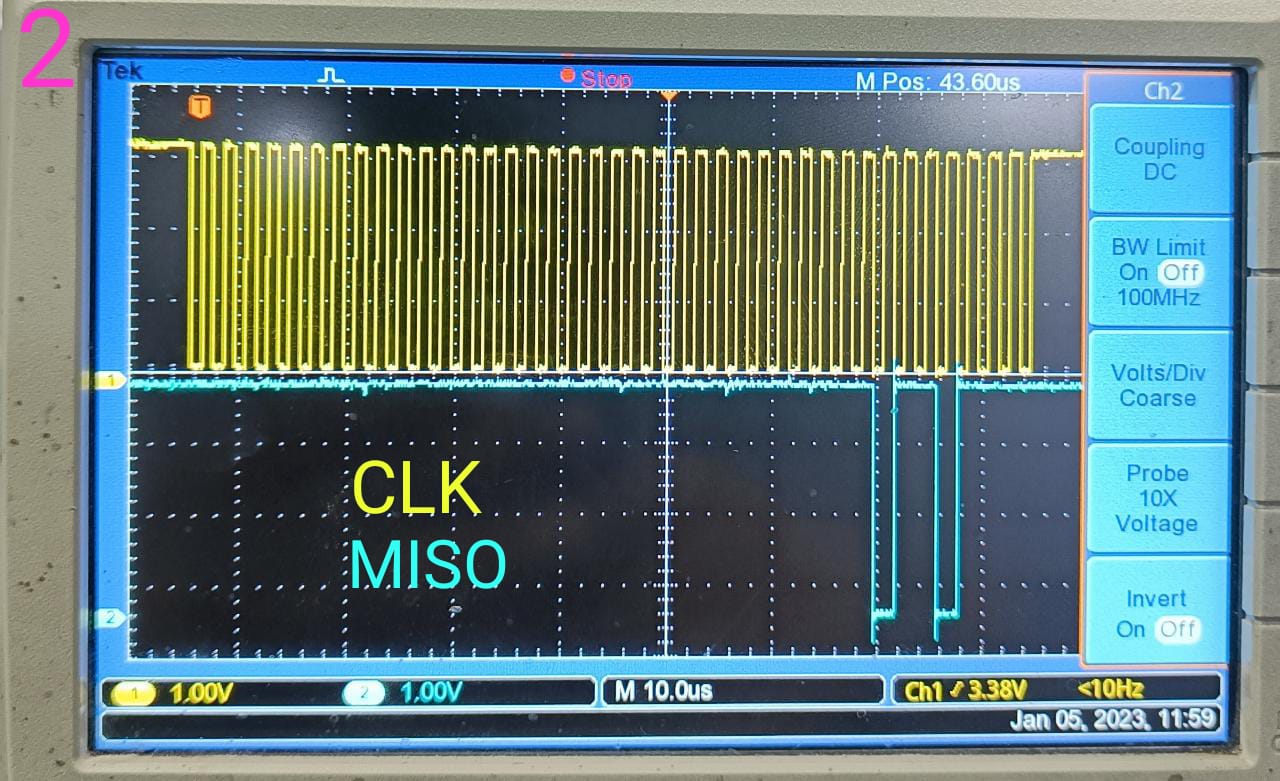
SPI\_write\_byte 3 = 0x13 //Address\_2 (bit 15 to 8)

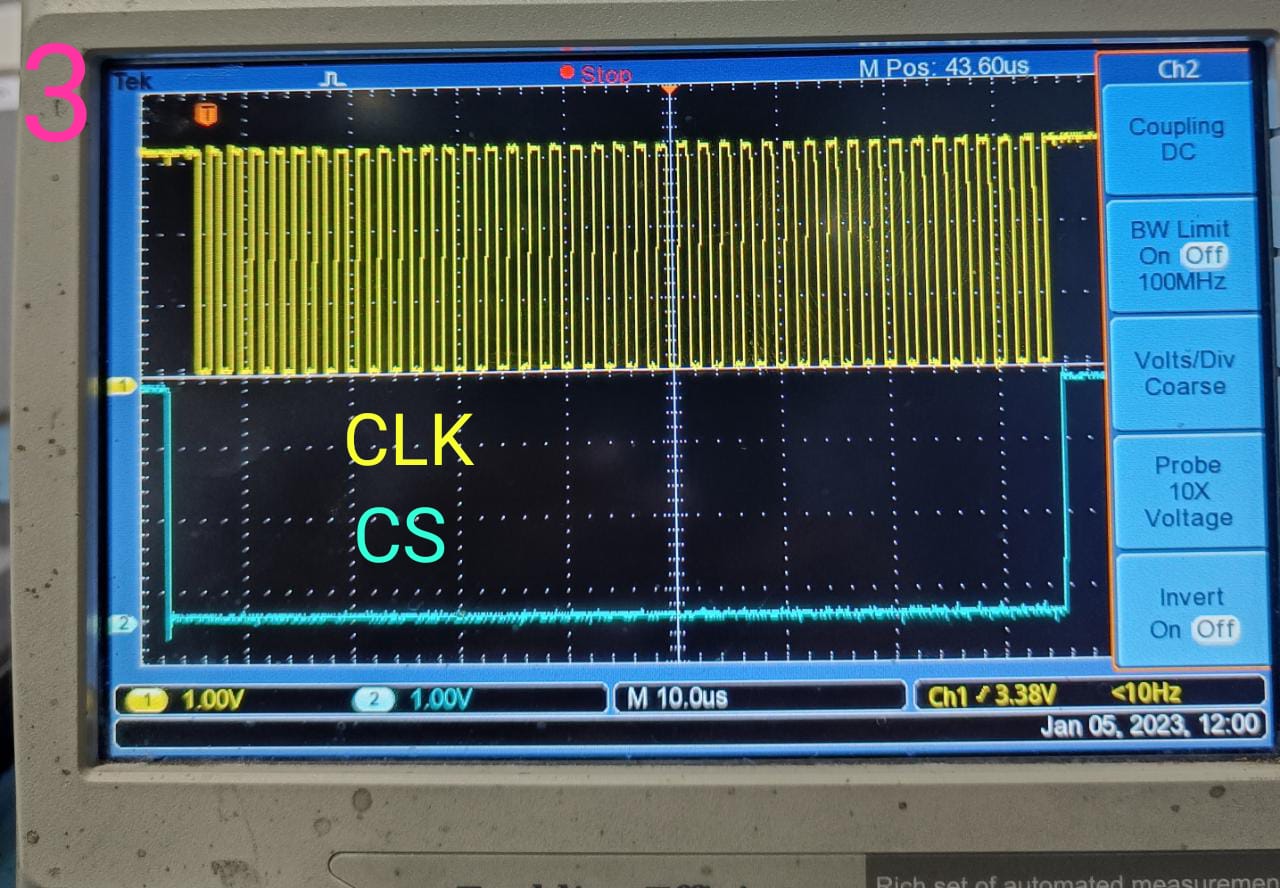
SPI\_write\_byte 4 = 0x88 //Address\_3 (bit 7 to 0)

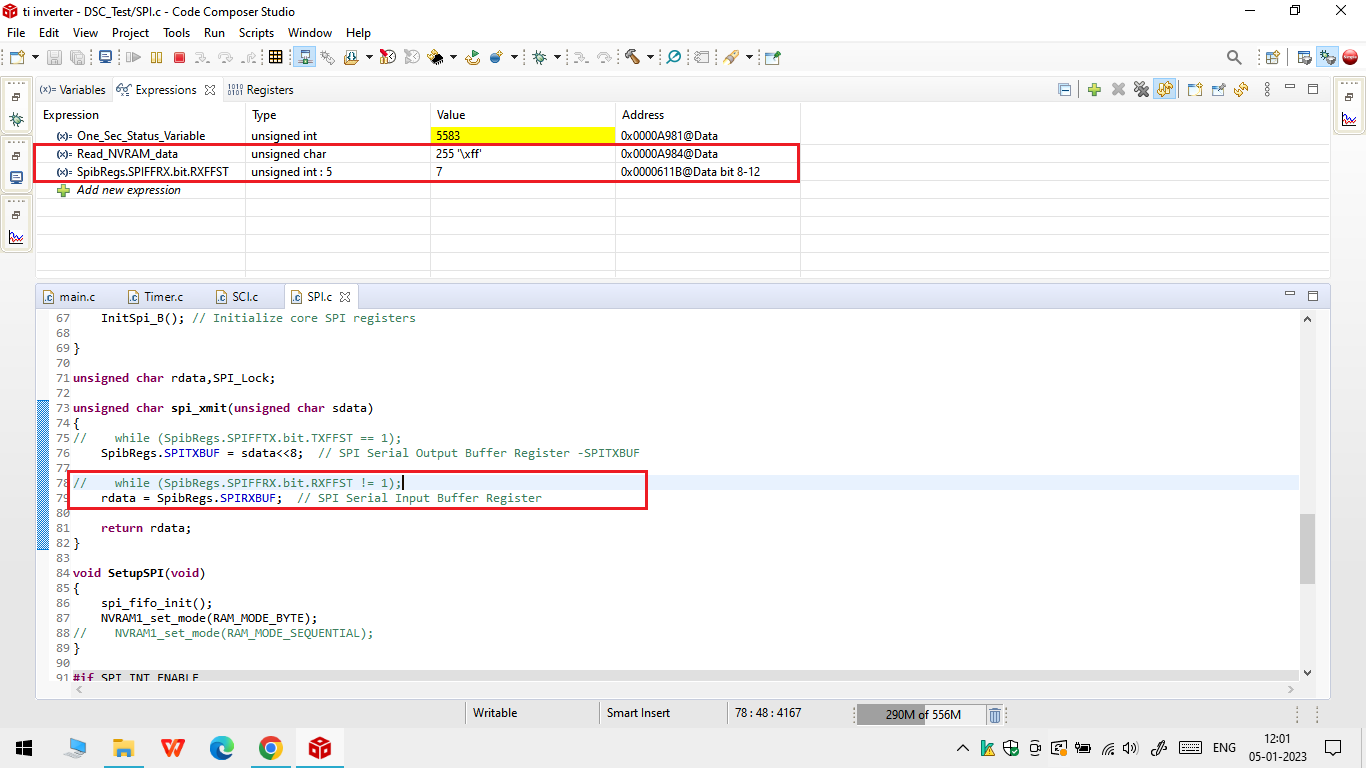
SPI\_write\_byte 5 = 0x00 //Dummy Write to read data

Case 1 :

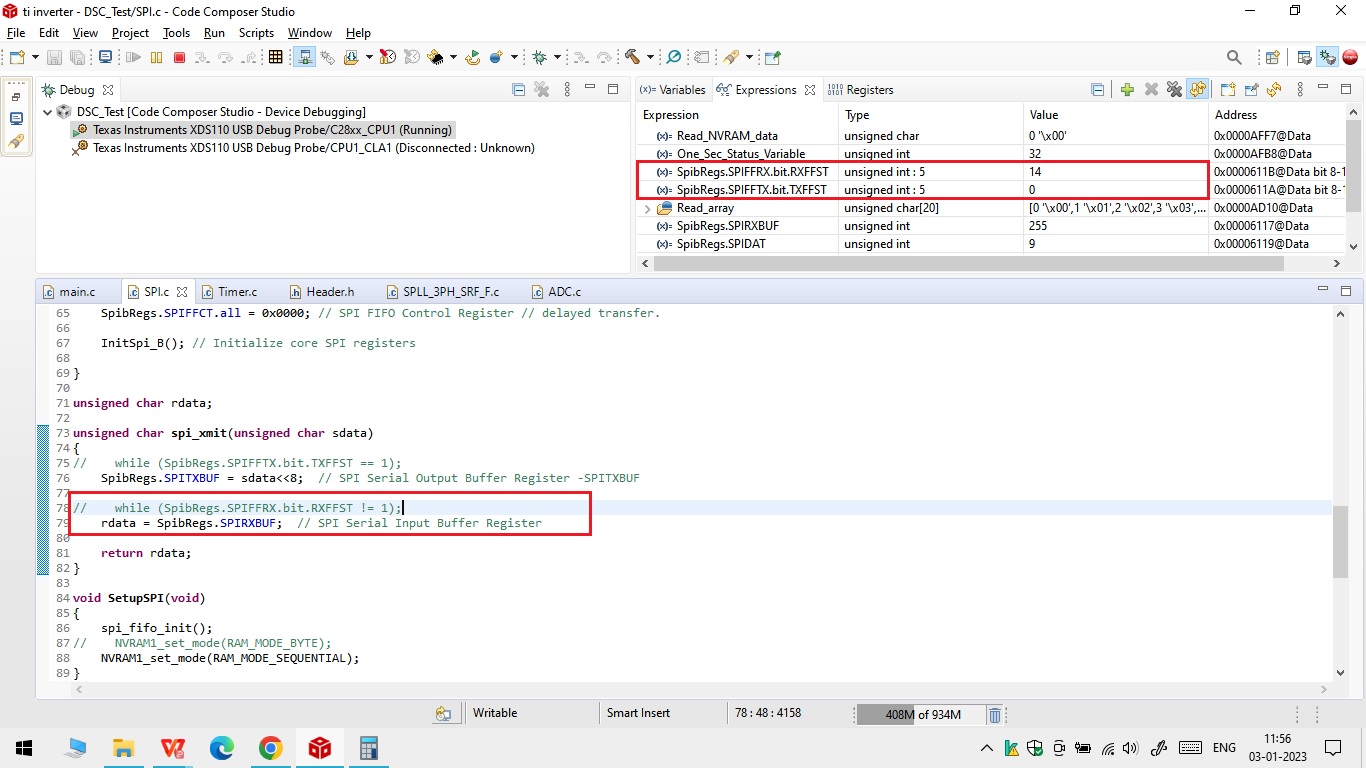
SPI Pulses When RX FIFO status **(SpibRegs.SPIFFRX.bit.RXFFST)** is Not checked



When receiving the data without checking the RX Fifo status buffer (SpibRegs.SPIFFRX.bit.RXFFST) it shows the values as 7 , 14 …etc & sometimes the Overrun flag bit (SpibRegs.SPISTS.bit.OVERRUN\_FLAG) is also getting High(1).



Case 2 :

SPI Pulses When RX FIFO status **(SpibRegs.SPIFFRX.bit.RXFFST)** is Checked

Receive data when 1 or more word is available.

1. As per the above configuration the clock is not continuous ?
2. Master is sending the data when there is no Clock (CLK) pulse available ?
3. I’m not getting any data on the MISO pin (from the slave device)