

ADC acquisition time is 1970ns

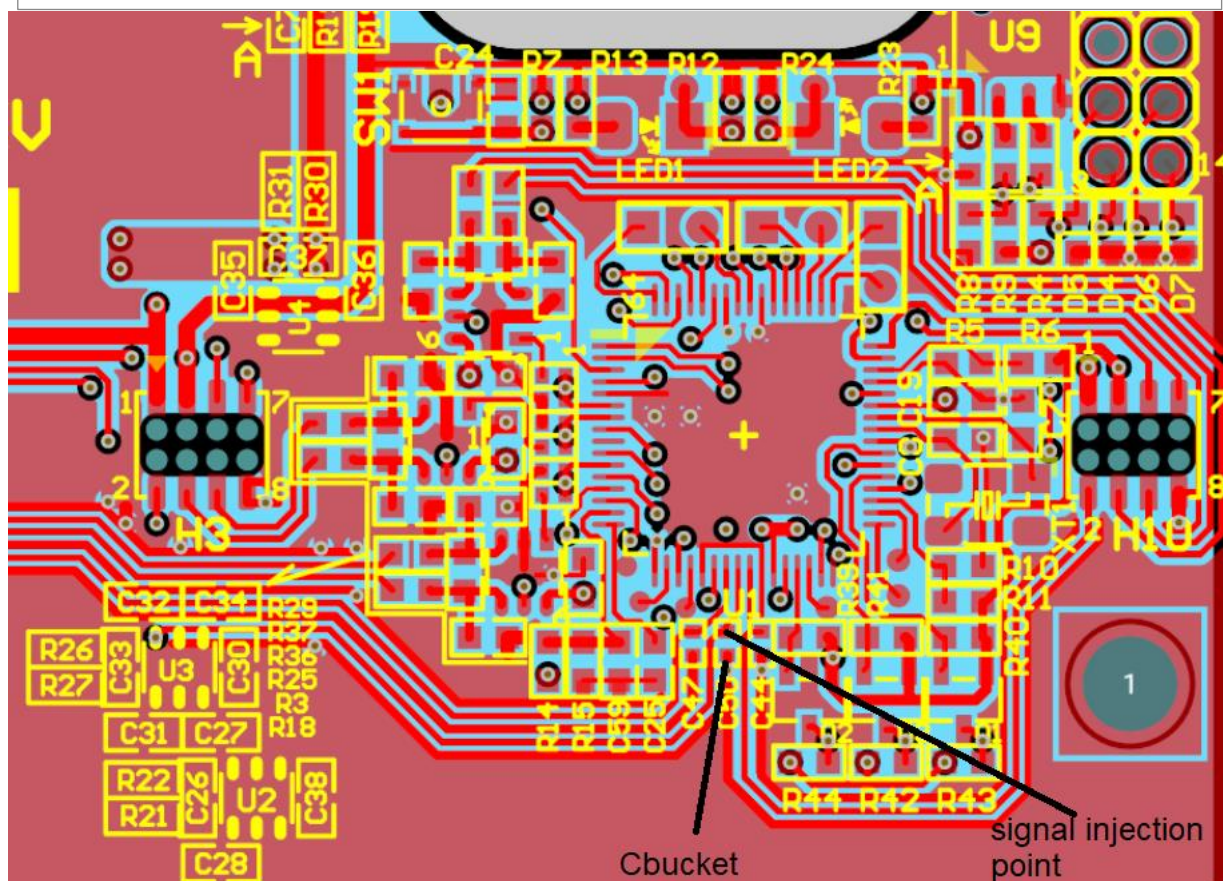
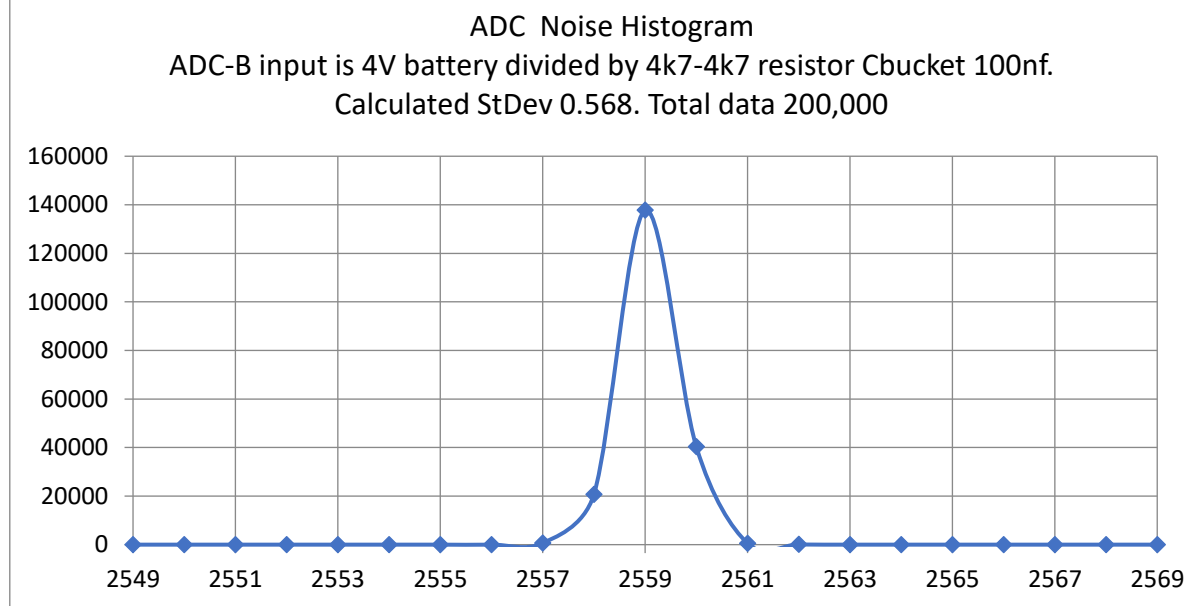


Figure 1

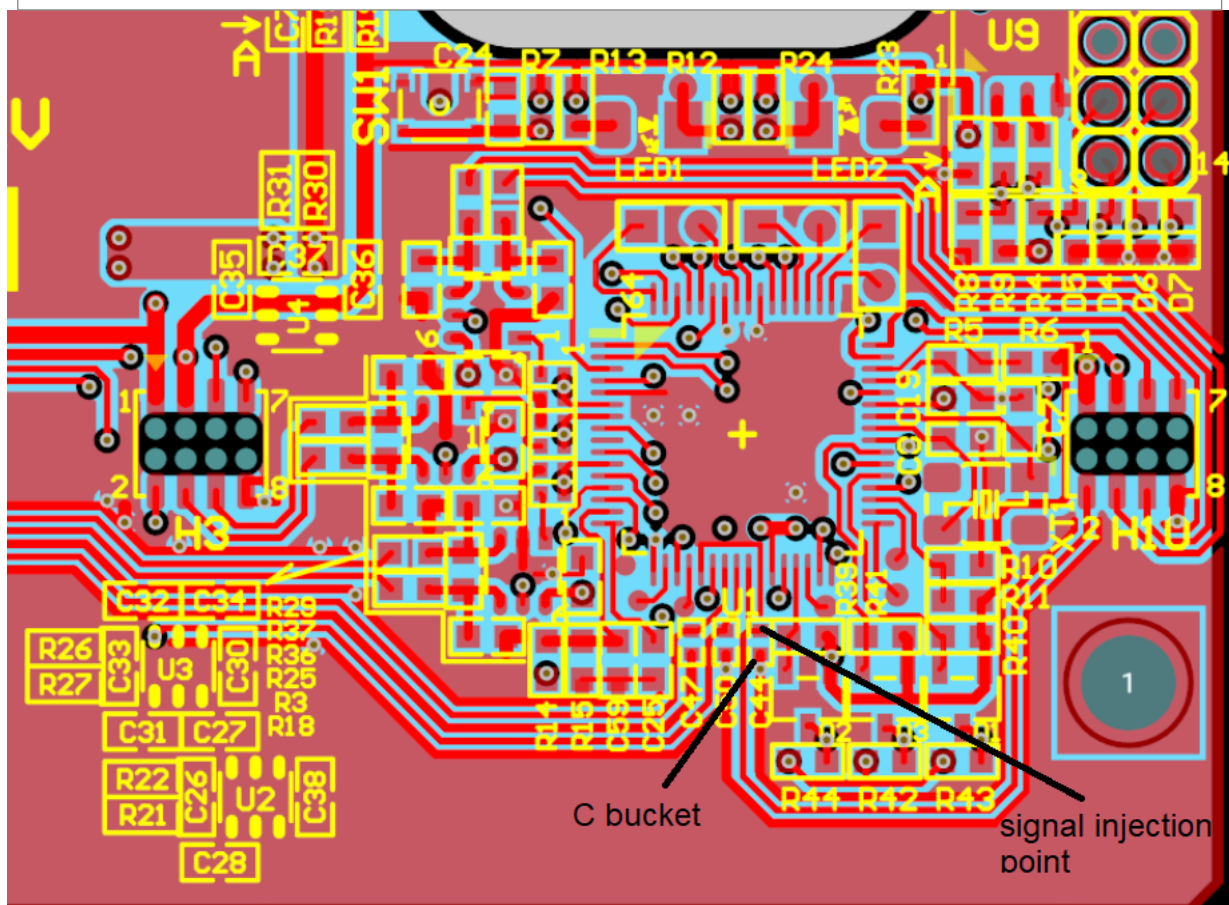
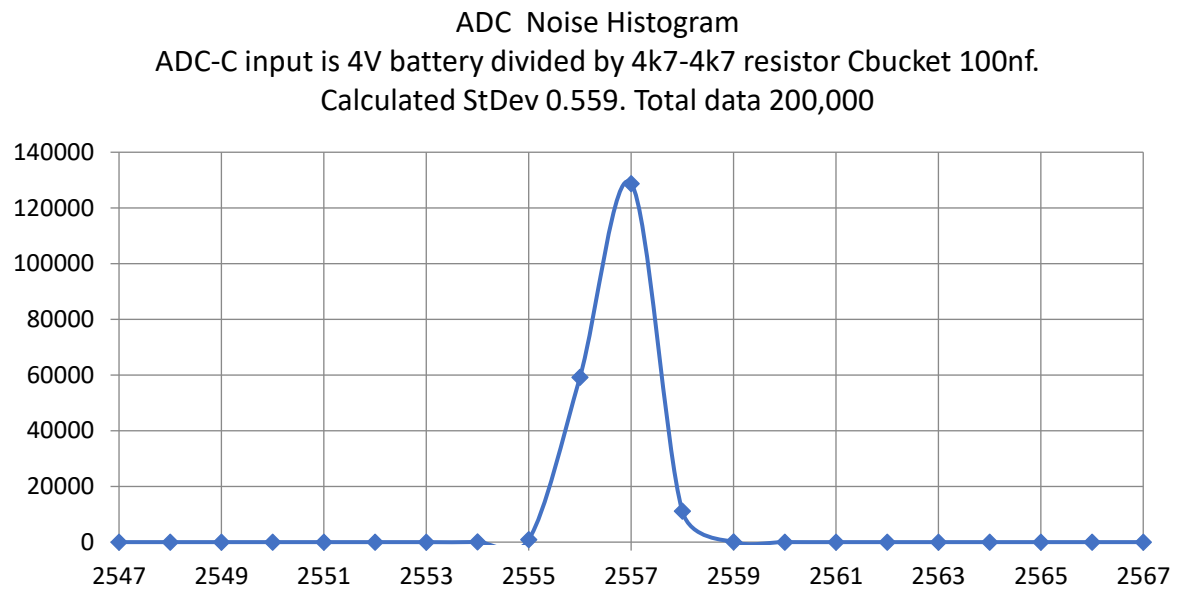


Figure 2

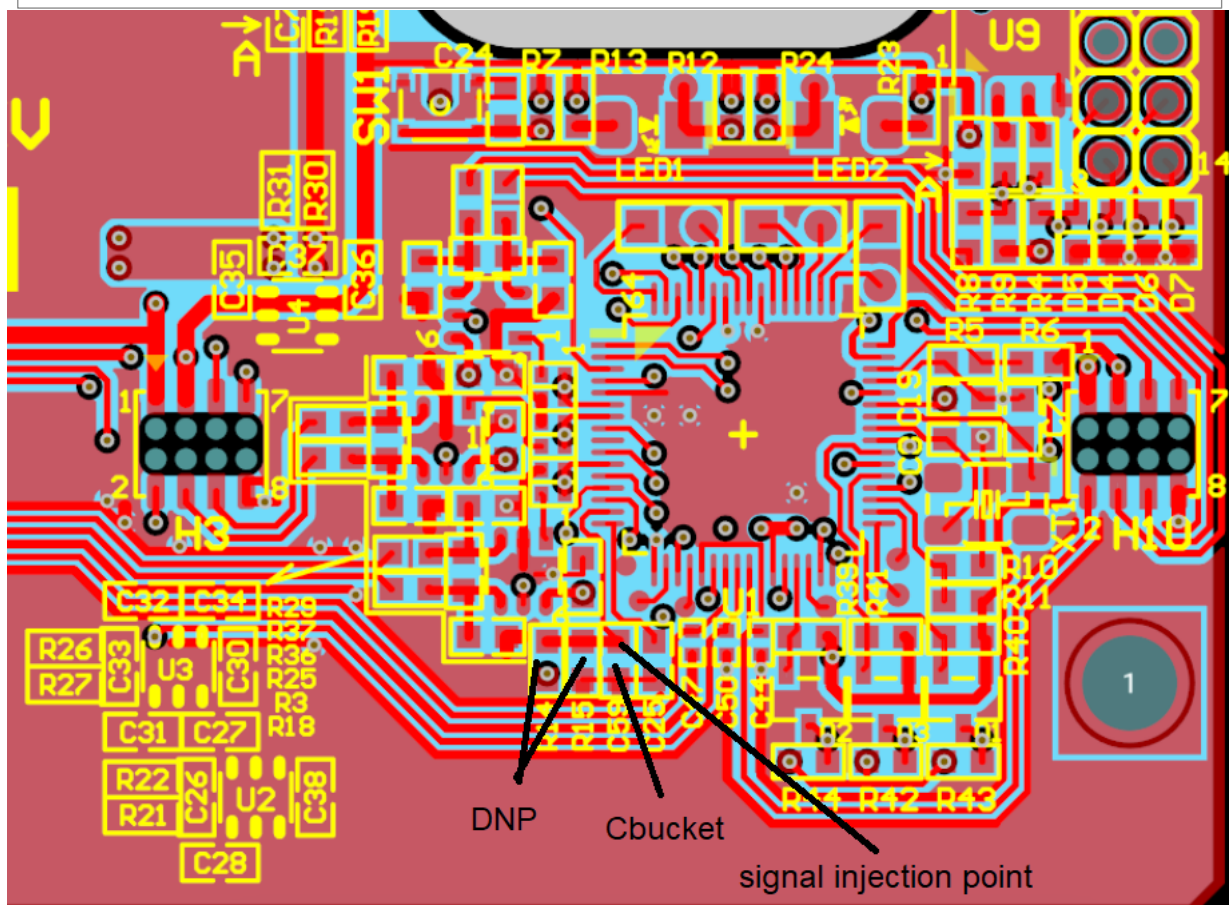
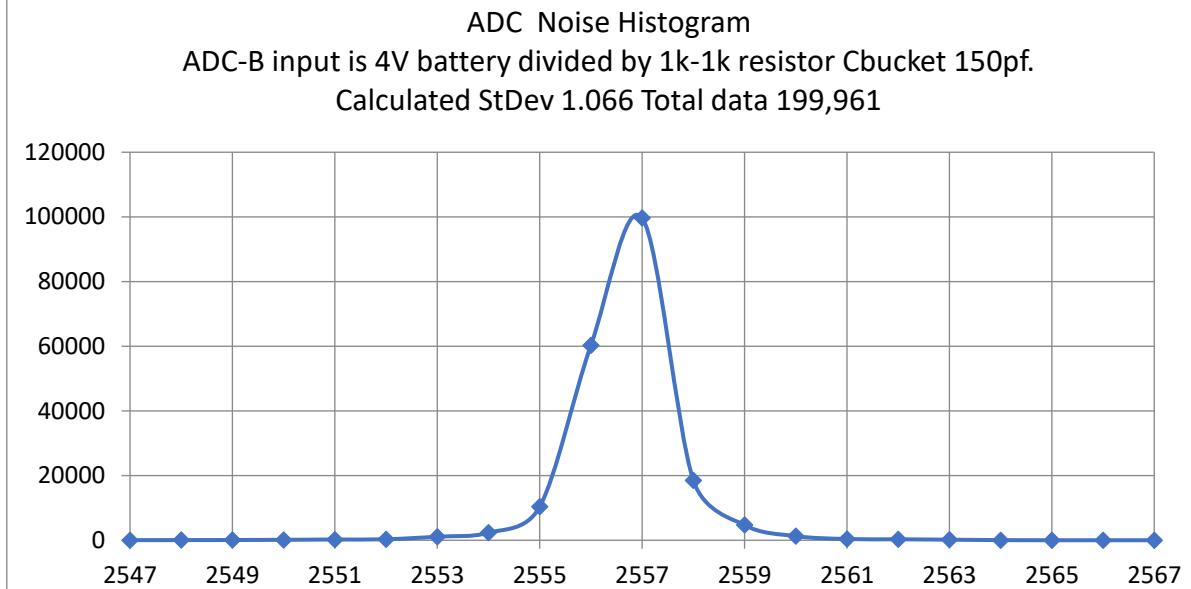


Figure 3

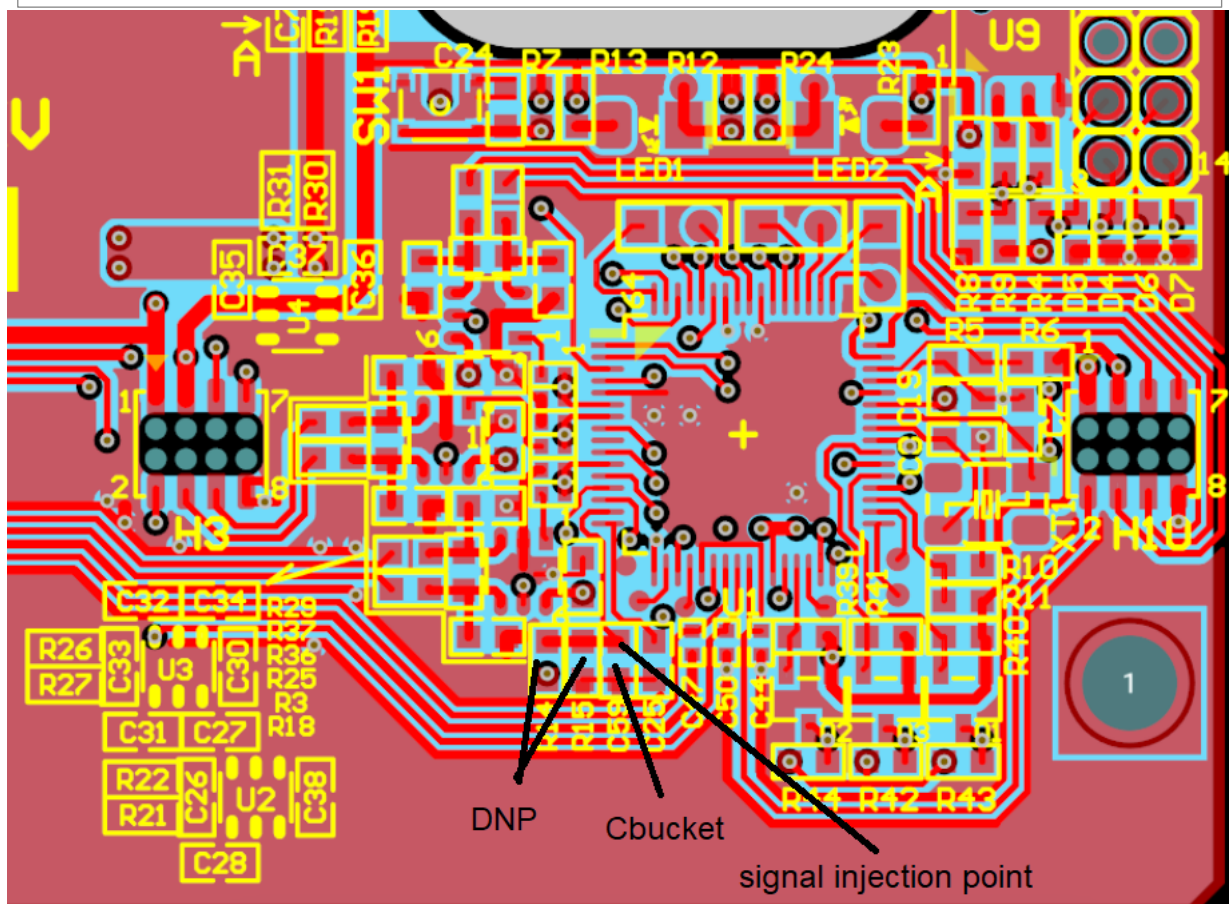
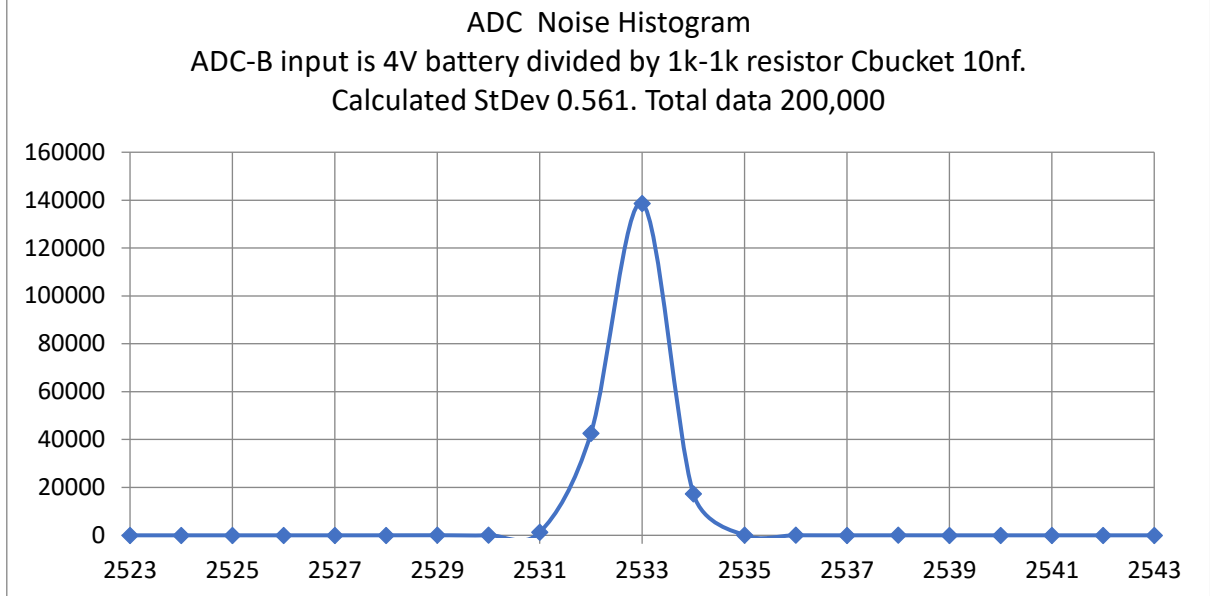


Figure 4

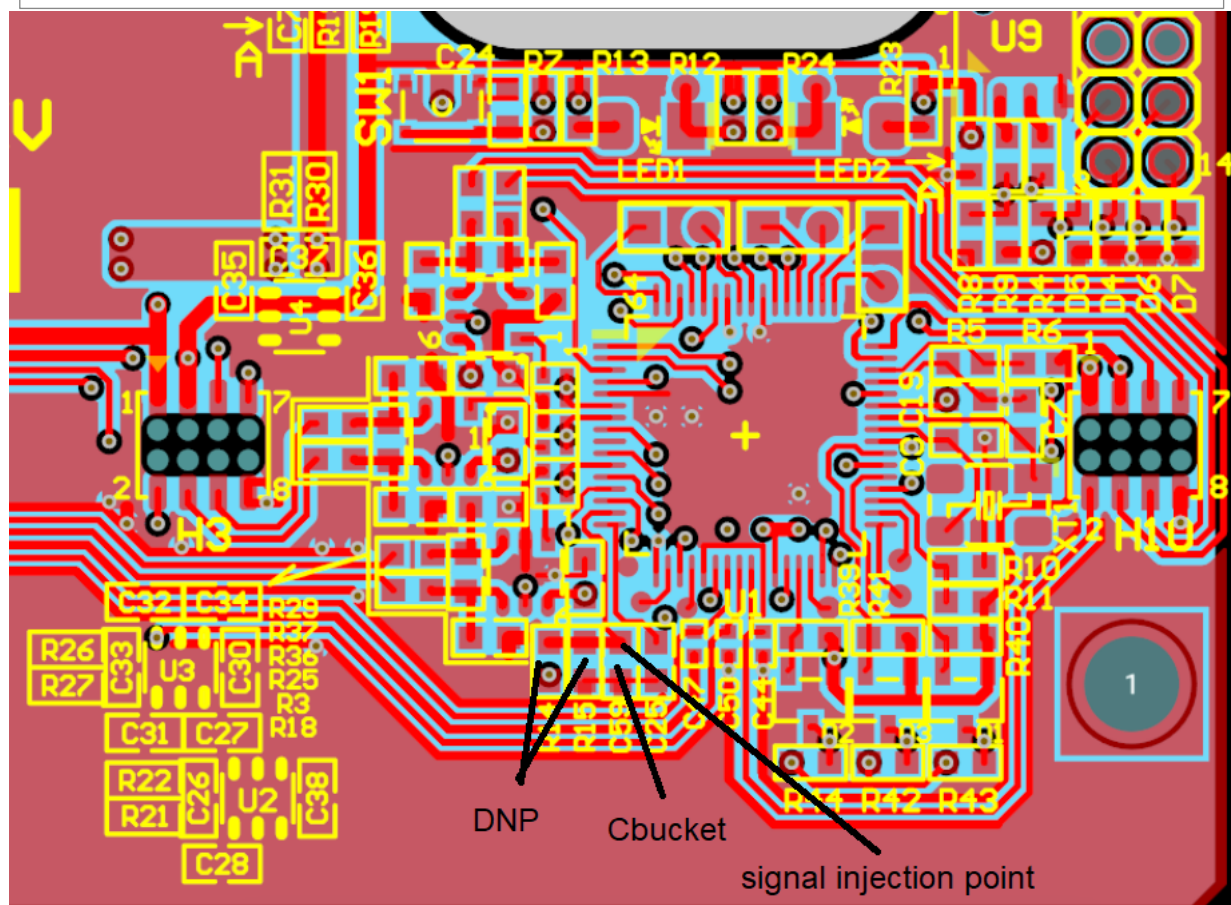
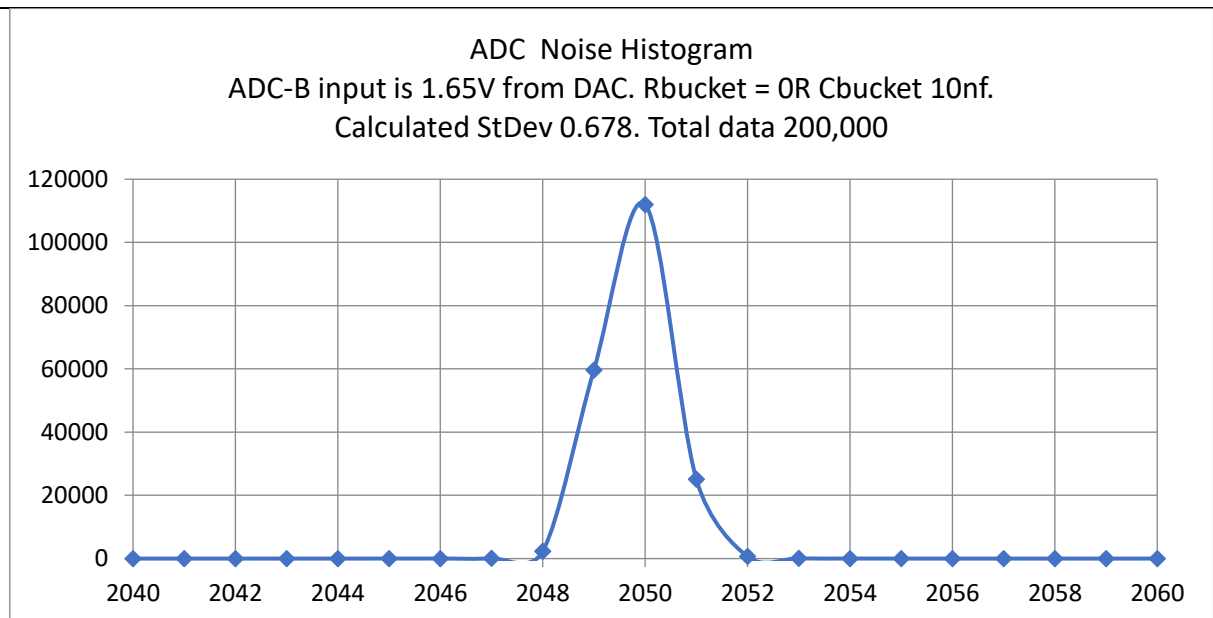


Figure 5

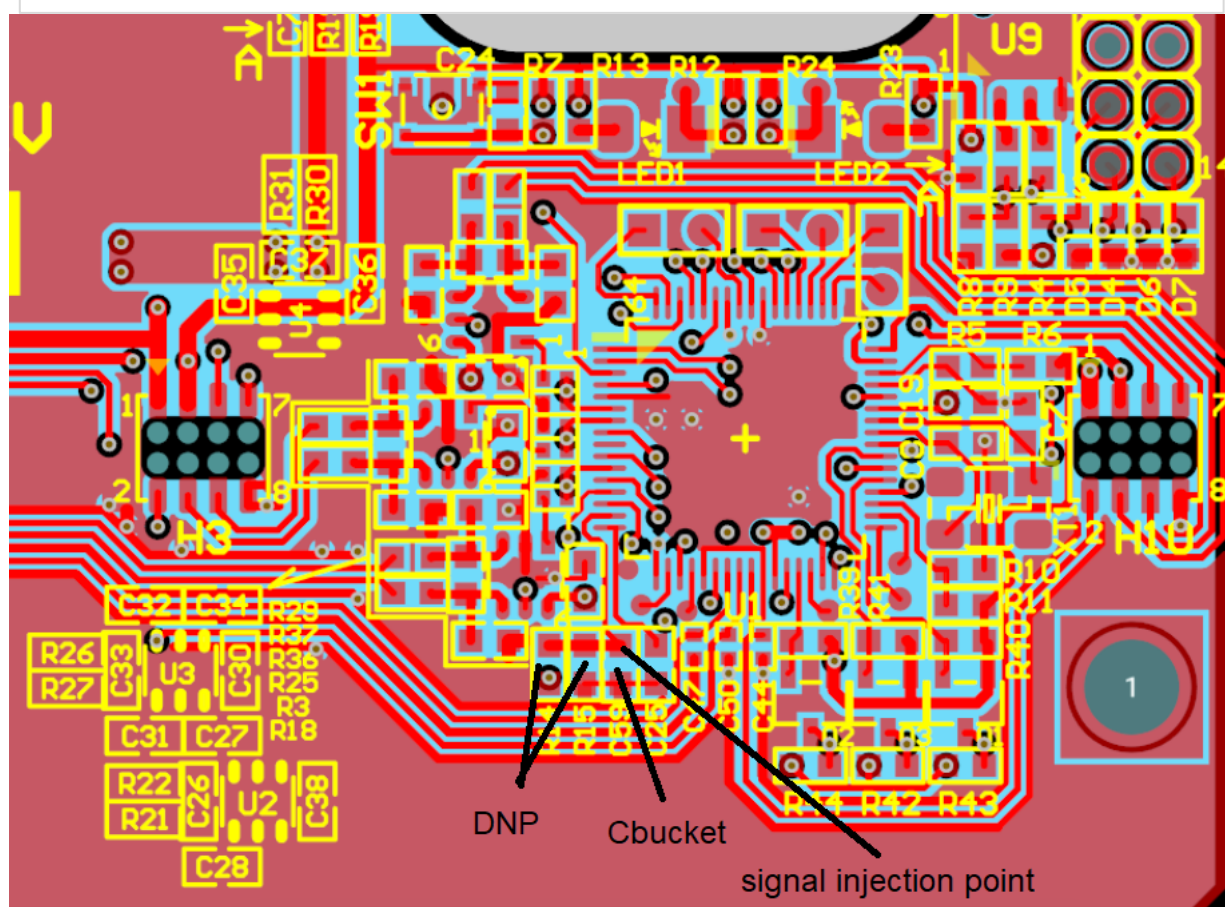
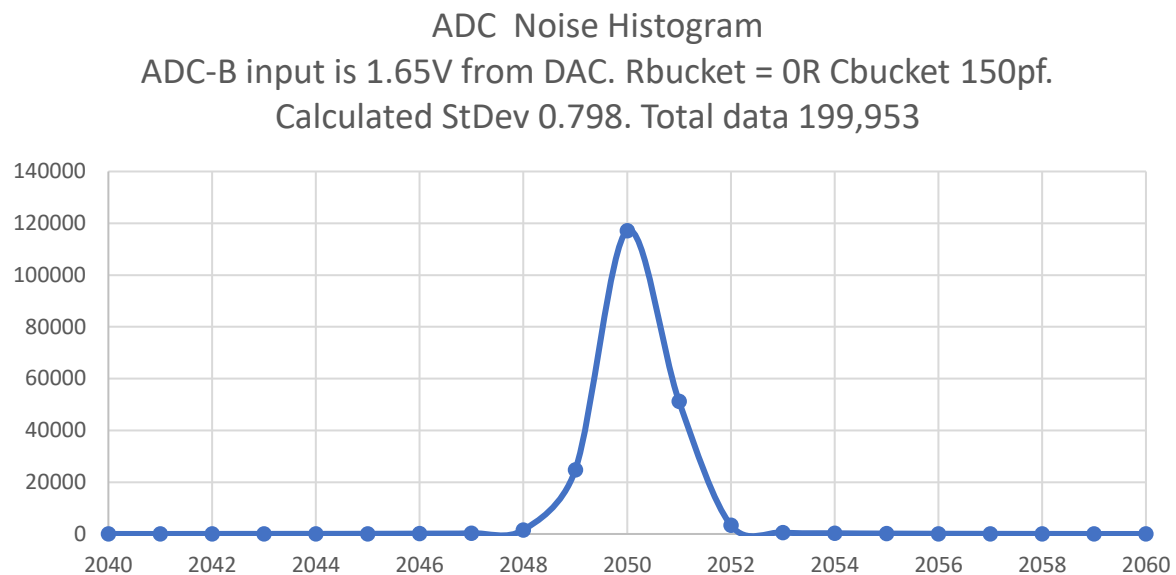


Figure 6

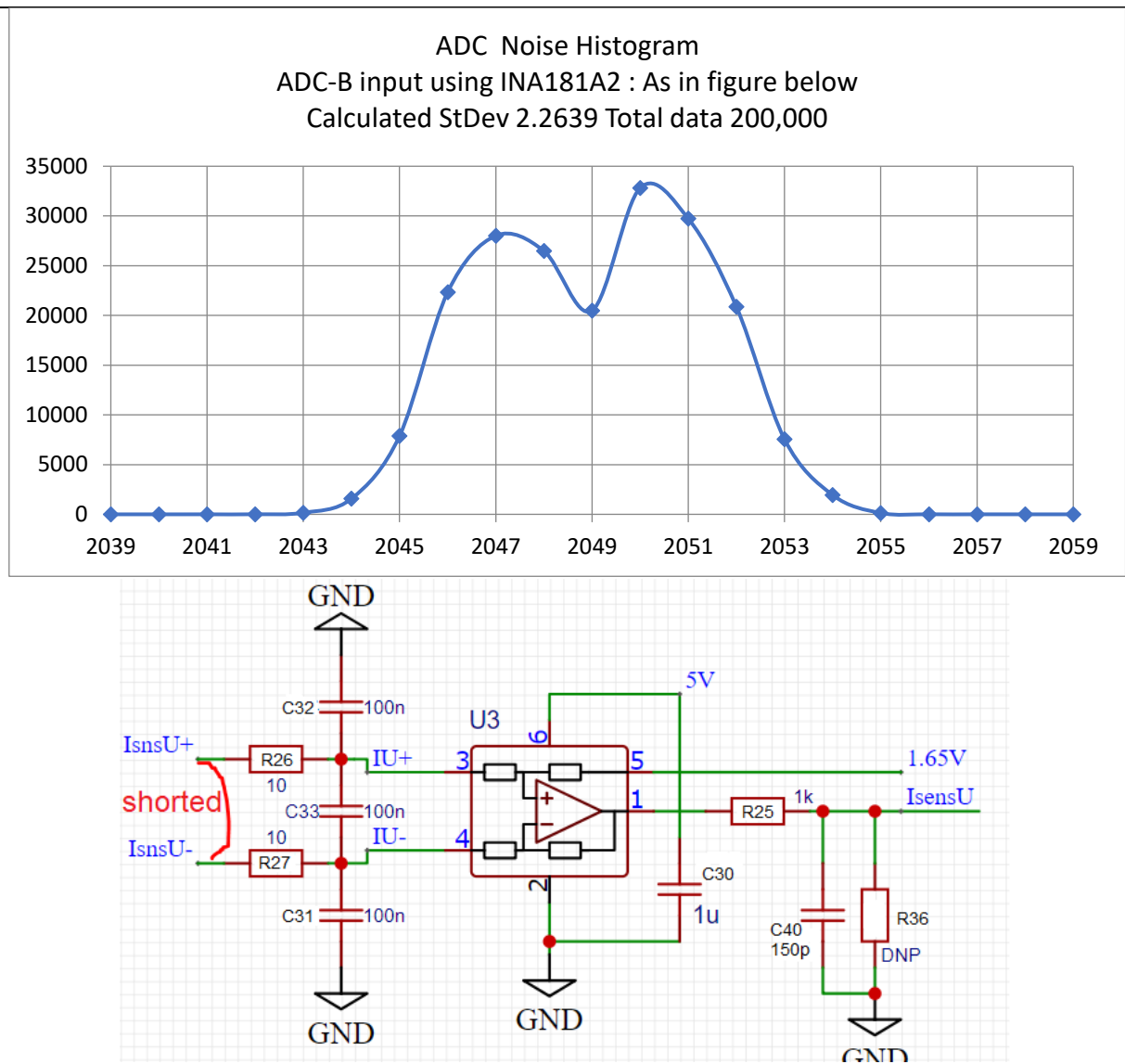


Figure 7

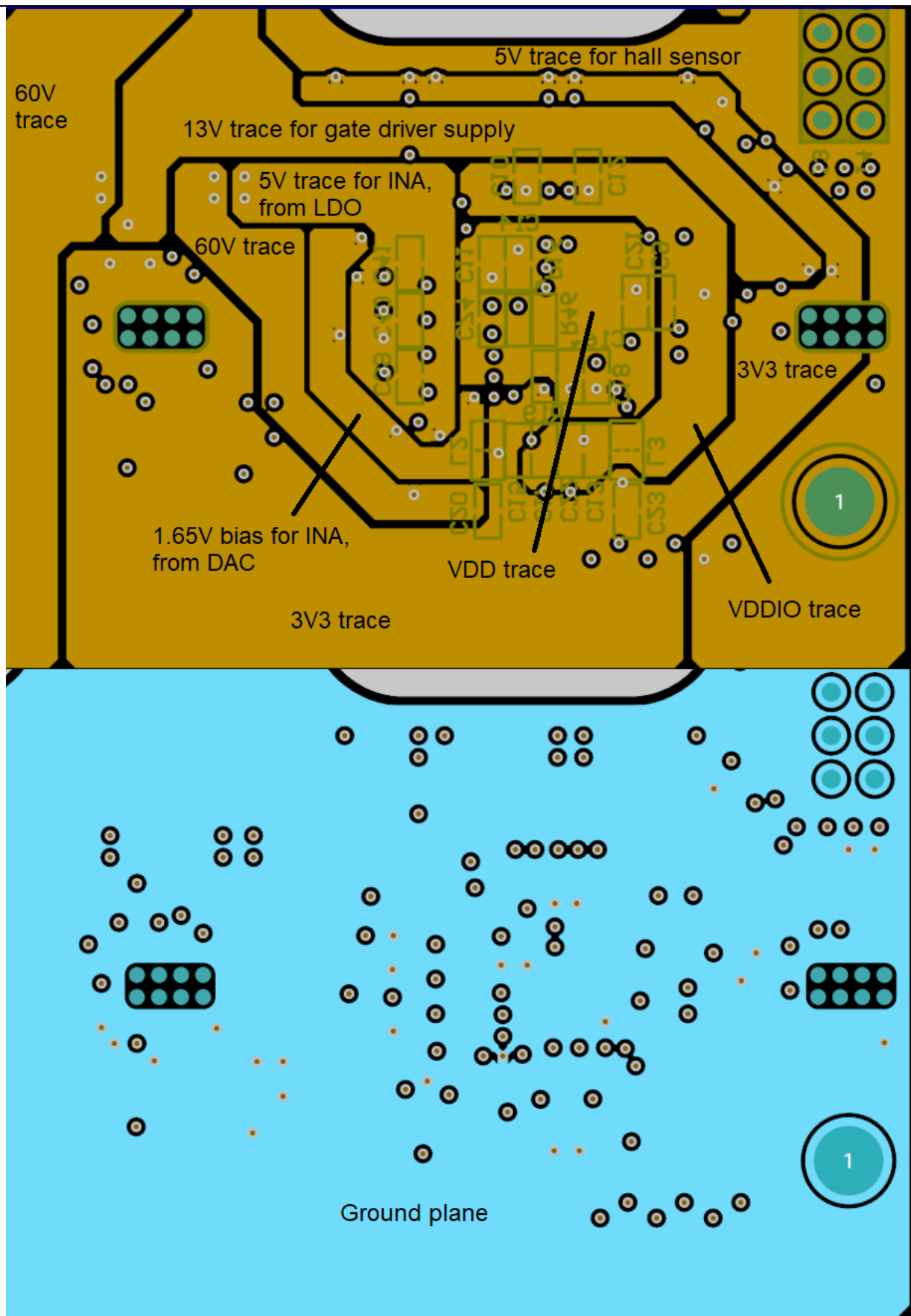


Figure 8. Layer stacking : Top(red) – Ground plane(cyan) – Power plane(brown) – Bottom (blue)

60V trace and 13V trace are floating, so the buck regulator do not work.

5V supply come from battery through LDO.

3V3 supply come from 5V through LDO.

VDD core use internal LDO

ADC Noise Histogram

ADC-B input come from PGA3OF. Rfilt (internal) 200ohm, Cfilt(ext) 150pf
 PGA3IN is from 4V battery, divided by 1K - 3K3 resistor. PGA3 gain is 3x
 Calculated StDev 4.943. Total data 190,220

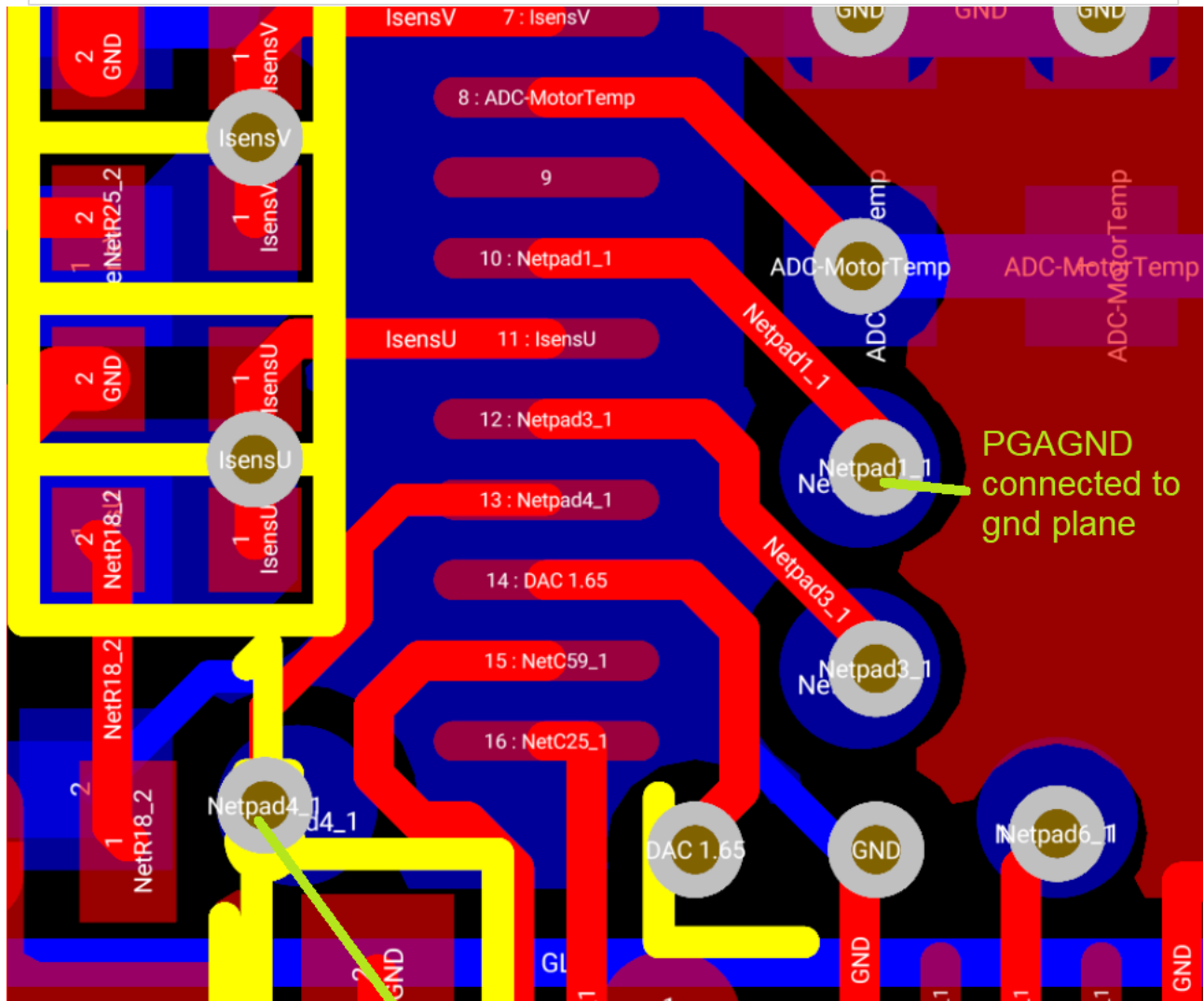
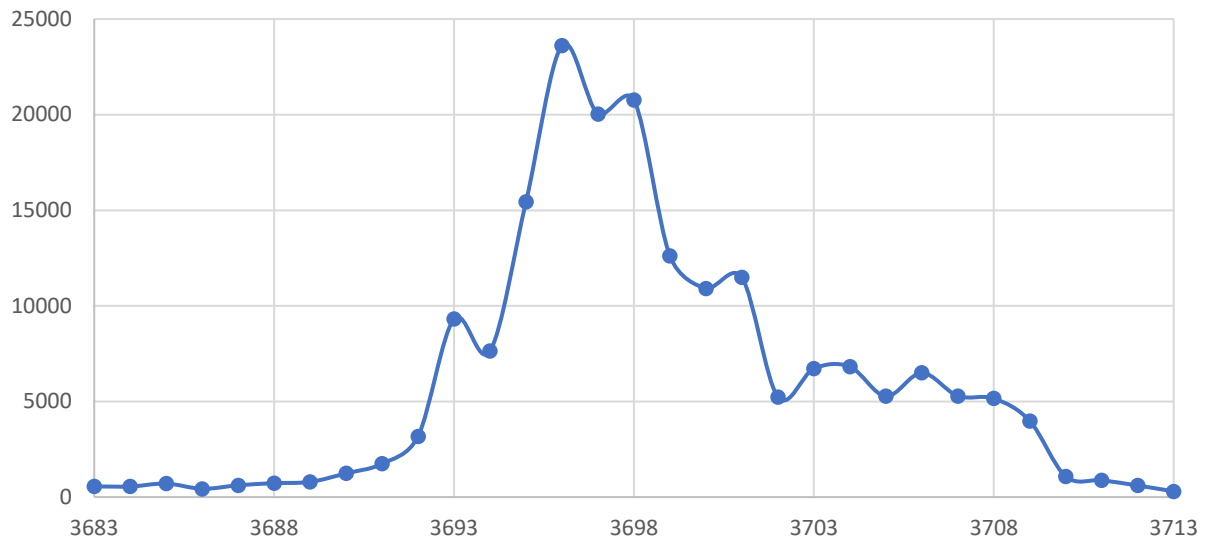


Figure 9

