

Setup:

TI F28335 communicates via parallel bus (XINTF) with the following nodes:

- TI C6747
 - o XINTF zone 7
 - o over HPI
 - o address + data multiplexed
- EtherCAT module
 - o XINTF zone 6
 - o separate address and data lines
- external ADC
 - o XINTF zone 0

Problems:

1. First High-Word read = 0x0000

The first High-Word is read out with 0x0000 each time a new address is set.

This happens:

- in auto-increment-mode:
 - o the first read access after setting a new start address
- in NON-auto-increment-mode (i.e. when reading a single value):
 - o every time

→ Reason for this behavior is probably a wrong reaction/function of the xReady signal. The F28335 finishes its read request although it receives a BUSY signal from the C6747.

This behavior can be influenced by changing the XRDACTIVE setting.

- a) With setting XRDACTIVE = 4, the xReady signal is ignored. (see Figure 1)
- b) With setting XRDACTIVE = 5, the F28335 reacts correctly on the xReady signal. (see Figure 2)

a) Ignored xReady signal when XRDACTIVE = 4 (and X2TIMING = 0).

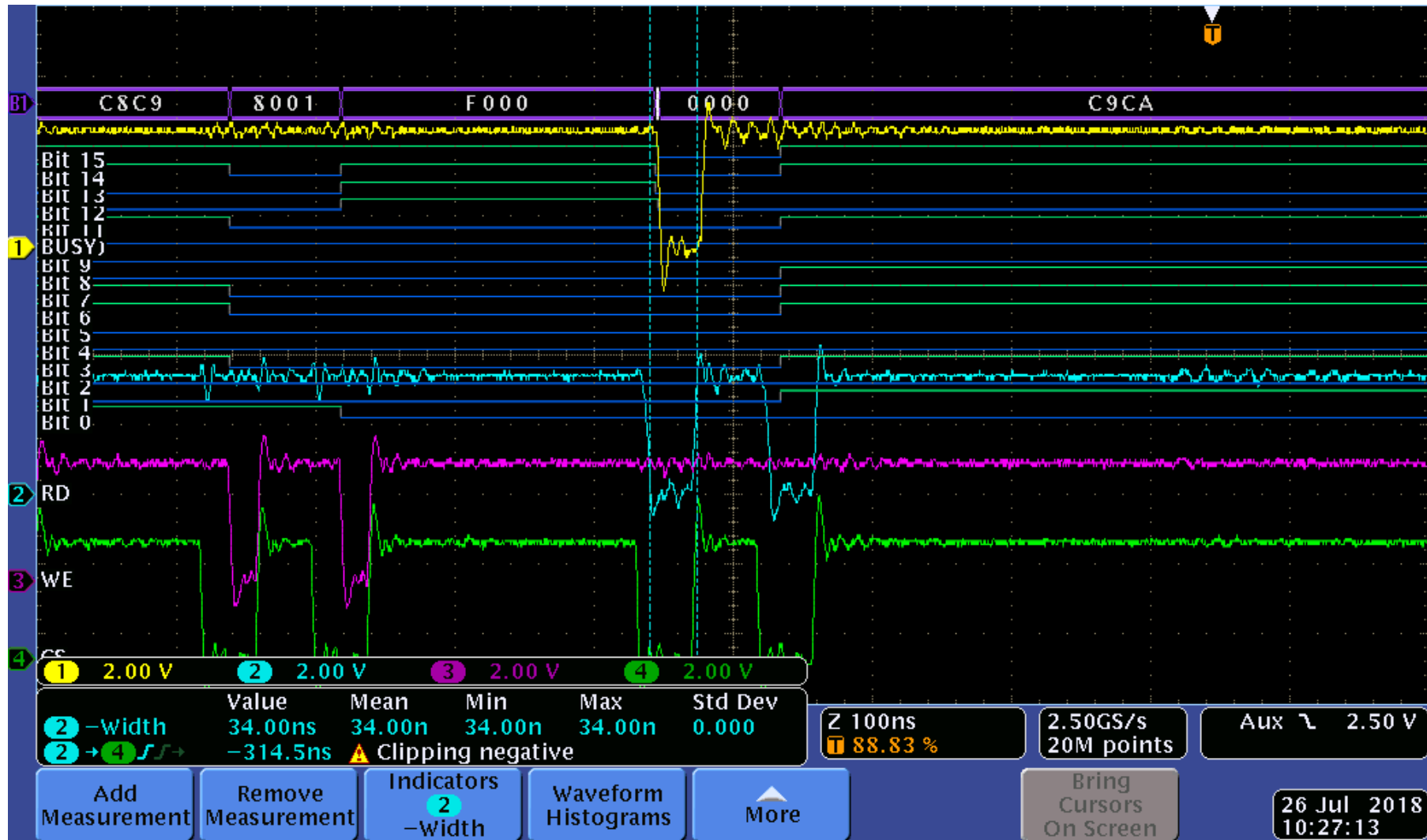


Figure 1: Reading data from 0x8001 F000. Expected value: 0xC7C8 C9CA. Read value: 0x0000 C9CA.
The first read pulse toggles to HIGH again before xReady is HIGH. → XINTF settings: XRDACTIVE = 4 (X2TIMING = 0)
xReady (yellow), nRead (cyan), nWrite (magenta), nCS (green), parallel bus (violet)

b) Anticipated xReady signal when XRDACTIVE = 5 (and X2TIMING = 0).

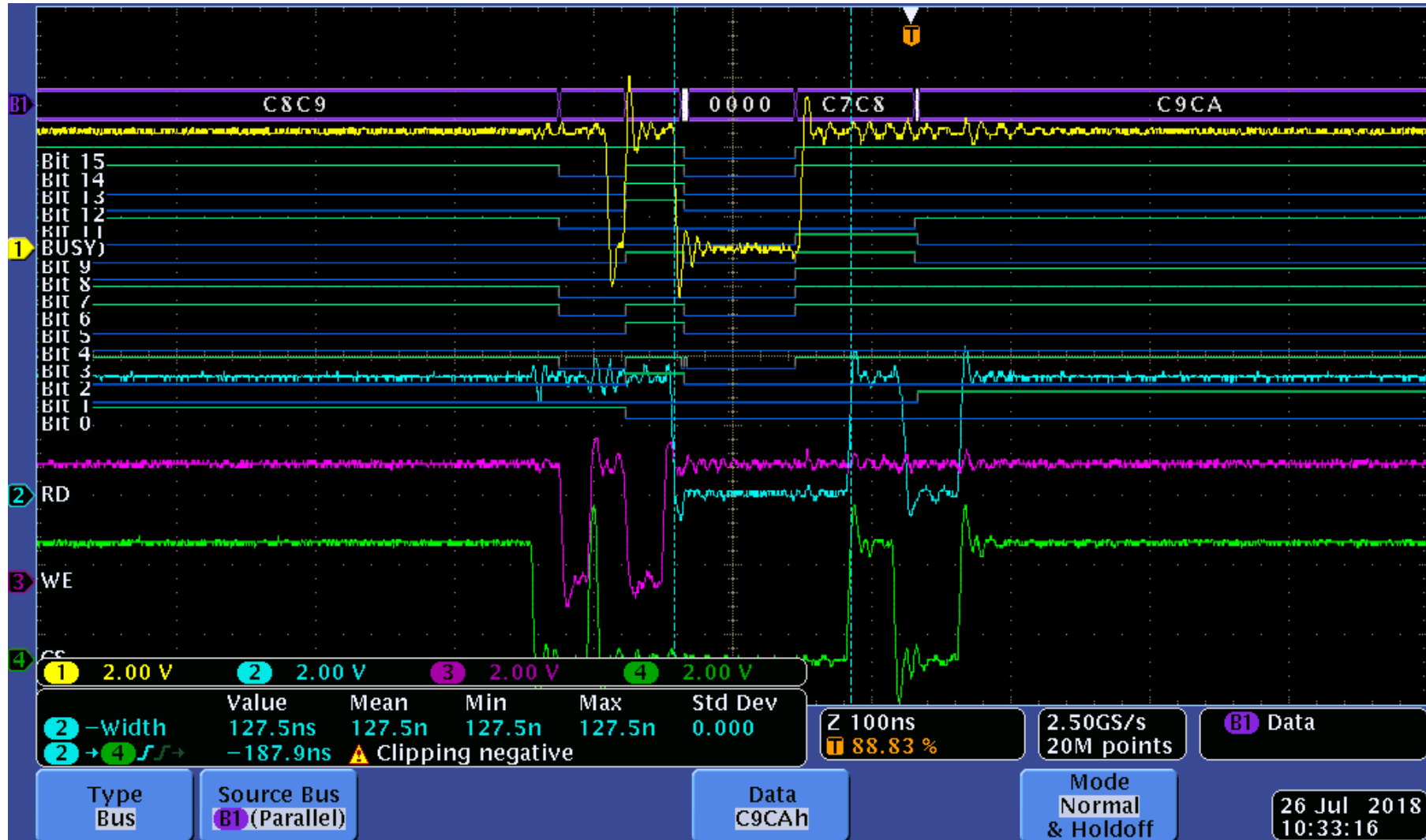


Figure 2: Reading data from 0x8001 F000. Value 0xC7C8 C9CA read correctly.
The first read pulse is prolonged because of the xReady signal. → XINTF settings: XRDACTIVE = 5 (X2TIMING = 0)
xReady (yellow), nRead (cyan), nWrite (magenta), nCS (green), parallel bus (violet)

Question 1	Why does the slight change of XRDACTIVE from “4” to “5” ticks change the reaction on the xReady signal? - Why is the behavior related to the active tick setting? - Why does the F28335 not wait for the C6747 in case the active ticks are set to 4? It seems to ignore the xReady signal completely in this case.
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Question 2	So far, we always use asynchronous mode for this XINTF (READYMODE = 1). Can you explain the difference between asynchronous and synchronous mode in more detail? In the datasheet this topic is scarcely covered.
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2. Timing restrictions for XINTF

Before getting to the results above, the following settings for the XINTF (Zone 7) have been used:

Parameter	Description	Value
XWRLEAD	Write LeadTicks	1
XWRACTIVE	Write ActiveTicks	2
XWRTRAIL	Write TrailTicks	2
XRDLEAD	Read LeadTicks	3
XRDACTIVE	Read ActiveTicks	4
XRDTRAIL	Read TrailTicks	3
USEREADY	Use XREADY Pin	1
READYMODE	Enable the XREADY sampling	1
X2TIMING	Double the TimingSettings	0

After checking in the datasheet, it seems this is an invalid configuration (see Figure 3):

4.3 Asynchronous Mode (USEREADY = 1, READYMODE = 1)						
XRDLEAD ≥ 1	XRDACTIVE ≥ 2	XRDTRAIL 0	XWRLEAD ≥ 1	XWRACTIVE ≥ 2	XWRTRAIL 0	X2TIMING 0, 1
or						
XRDLEAD ≥ 2	XRDACTIVE ≥ 1	XRDTRAIL 0	XWRLEAD ≥ 2	XWRACTIVE ≥ 1	XWRTRAIL 0	X2TIMING 0, 1

Figure 3: Timing settings for asynchronous mode.

Although the criteria **XRDTRAIL == 0** AND **XWDTRAIL == 0** was not met, the communication behavior stayed the same.
i.e. HIGH-word errors when XRDACTIVE = 4 and no HIGH-word errors with XRDACTIVE = 5.

Question 3	Can you explain how this wrong setting influences the communication? The reason I ask this is, that for another XINTF zone we must violate the above rules to get a working communication.
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The XINTF settings for communication with the attached EtherCAT Board (Zone 6) are as follows:

Parameter	Description	Value
XWRLEAD	Write LeadTicks	3
XWRACTIVE	Write ActiveTicks	7
XWRTRAIL	Write TrailTicks	3
XRDLEAD	Read LeadTicks	2
XRDACTIVE	Read ActiveTicks	7
XRDTRAIL	Read TrailTicks	2
USEREADY	Use XREADY Pin	1
READYMODE	Enable the XREADY sampling	1
X2TIMING	Double the TimingSettings	0

When changing XWRTRAIL to “0” as implicated, the communication **does not work** anymore. Data is then written incorrectly to the EtherCAT module.

Question 4	Can you please explain in more detail the timing requirements for XINTF of C2000 (trail, active, lead ticks, ...)?
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4.1 USEREADY = 0 (READYMODE = 0 or READYMODE = 1)							
Valid	XRDLEAD ≥ 1	XRDACTIVE ≥ 0	XRDTRAIL ≥ 0	XWRLEAD ≥ 1	XWRACTIVE ≥ 0	XWRTRAIL ≥ 0	X2TIMING 0, 1
4.2 Synchronous Mode (USEREADY = 1, READYMODE = 0)							
	XRDLEAD ≥ 1	XRDACTIVE ≥ 1	XRDTRAIL ≥ 0	XWRLEAD ≥ 1	XWRACTIVE ≥ 1	XWRTRAIL ≥ 0	X2TIMING 0, 1 ⁽¹⁾
4.3 Asynchronous Mode (USEREADY = 1, READYMODE = 1)							
	XRDLEAD ≥ 1	XRDACTIVE ≥ 2	XRDTRAIL 0	XWRLEAD ≥ 1	XWRACTIVE ≥ 2	XWRTRAIL 0	X2TIMING 0, 1
or							
	XRDLEAD ≥ 2	XRDACTIVE ≥ 1	XRDTRAIL 0	XWRLEAD ≥ 2	XWRACTIVE ≥ 1	XWRTRAIL 0	X2TIMING 0, 1

Figure 4: XINTF setting restrictions (from F28335 datasheet)

3. Read request from wrong address

Another issue we came across is that the address where the data is read from the C6747 is corrupted because of wrong XINTF settings. We cannot see the issue on the scope, but when checking the F28335 registers, it is clear, that the wrong address is set.

Error example:

On C6747 @address 0x8001 F37C the value 0x3B3C 3D3E is stored. When reading from this address, the data 0x6C6D 6E6F is read instead (incorrectly).

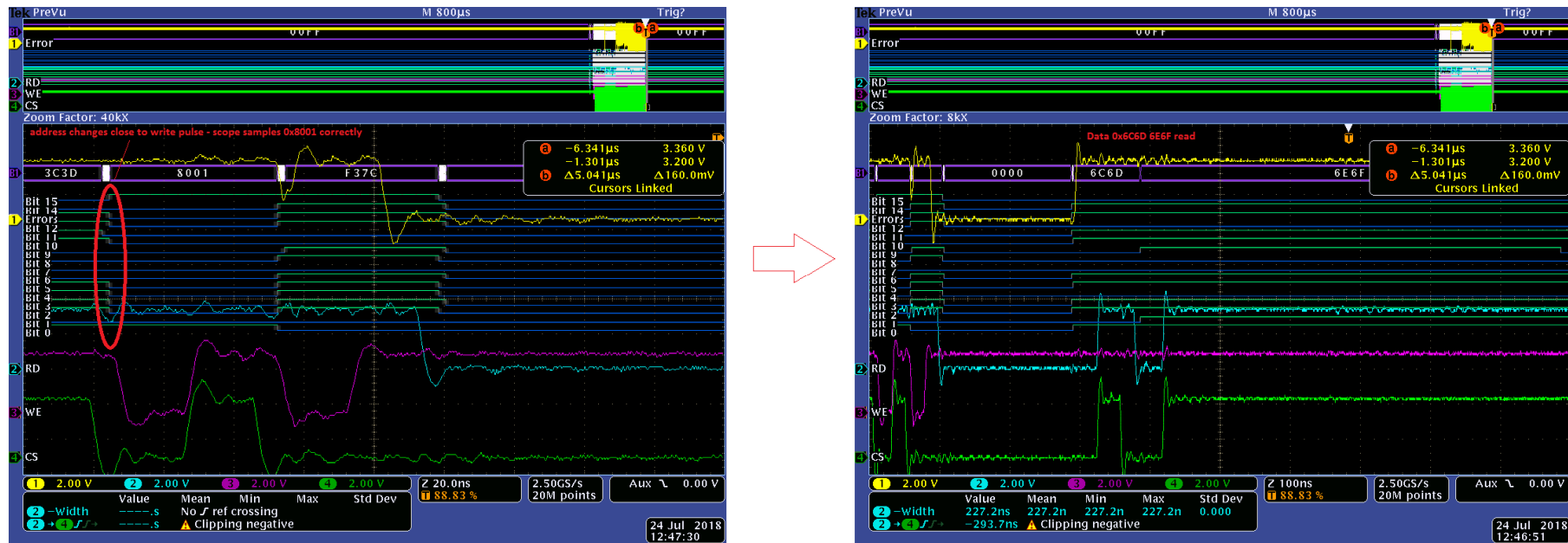


Figure 5: Scope recordings of incident. (0x6C6D 6E6F read instead of 0x3B3C 3D3E)
xReady (yellow), nRead (cyan), nWrite (magenta), nCS (green), parallel bus (violet)

F28335 debug output		
(x)= currAdr	unsigned long	223
(x)= testPattern[currAdr]	unsigned long	0x3B3C3D3E (Hex)
(x)= readBack2[currAdr]	unsigned long	0x6C6D6E6F (Hex)
(x)= *(Uint16*)0x200004	unsigned int	0xE009 (Hex)
(x)= *(Uint16*)0x200005	unsigned int	0xF380 (Hex)

← expected data
 ← actually read data
 } Address to read from => 0xE009 F380
 (already incremented automatically by 4)

↑

Expected address would be 8001F380

Figure 6: Watch output of F28335 at the same time instant as the scope recording

C6747 Memory

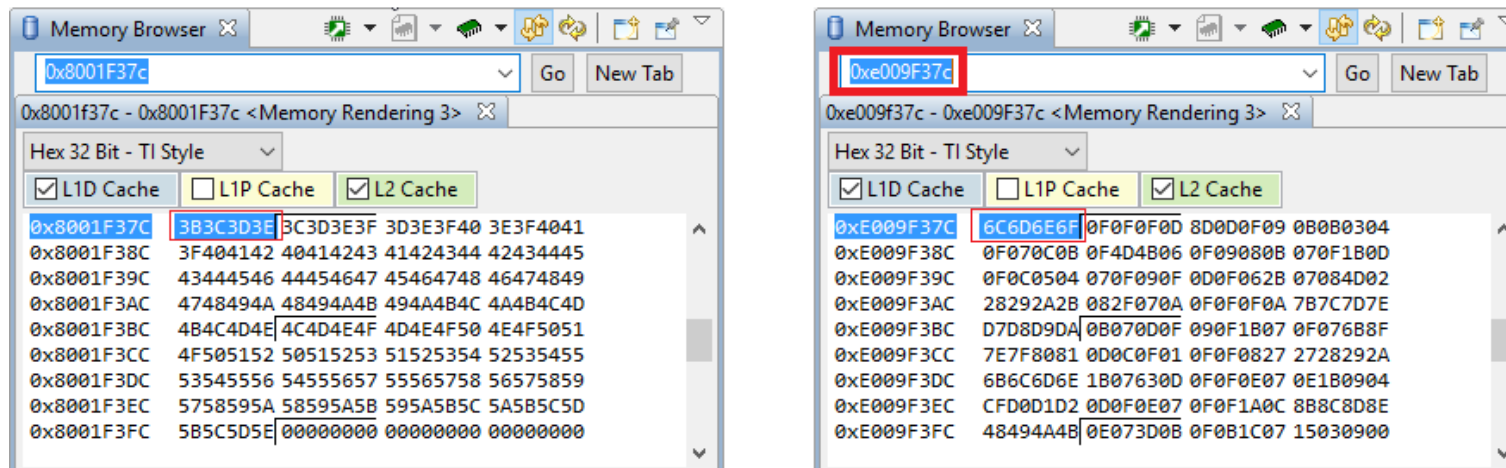


Figure 7: C6747 memory (@address 0x8001F37C and @address 0xE009F37C) at the same time instant as the scope recording

The described problem could be solved by increasing the XWRLEAD from "1" to "3". On the scope, however, the timing when the address bits toggle does not really change in relation to the write pulse start. But in the test firmware no communication errors occur. The increased time between CS start (green) and Write start (magenta) can be seen in Figure 8.

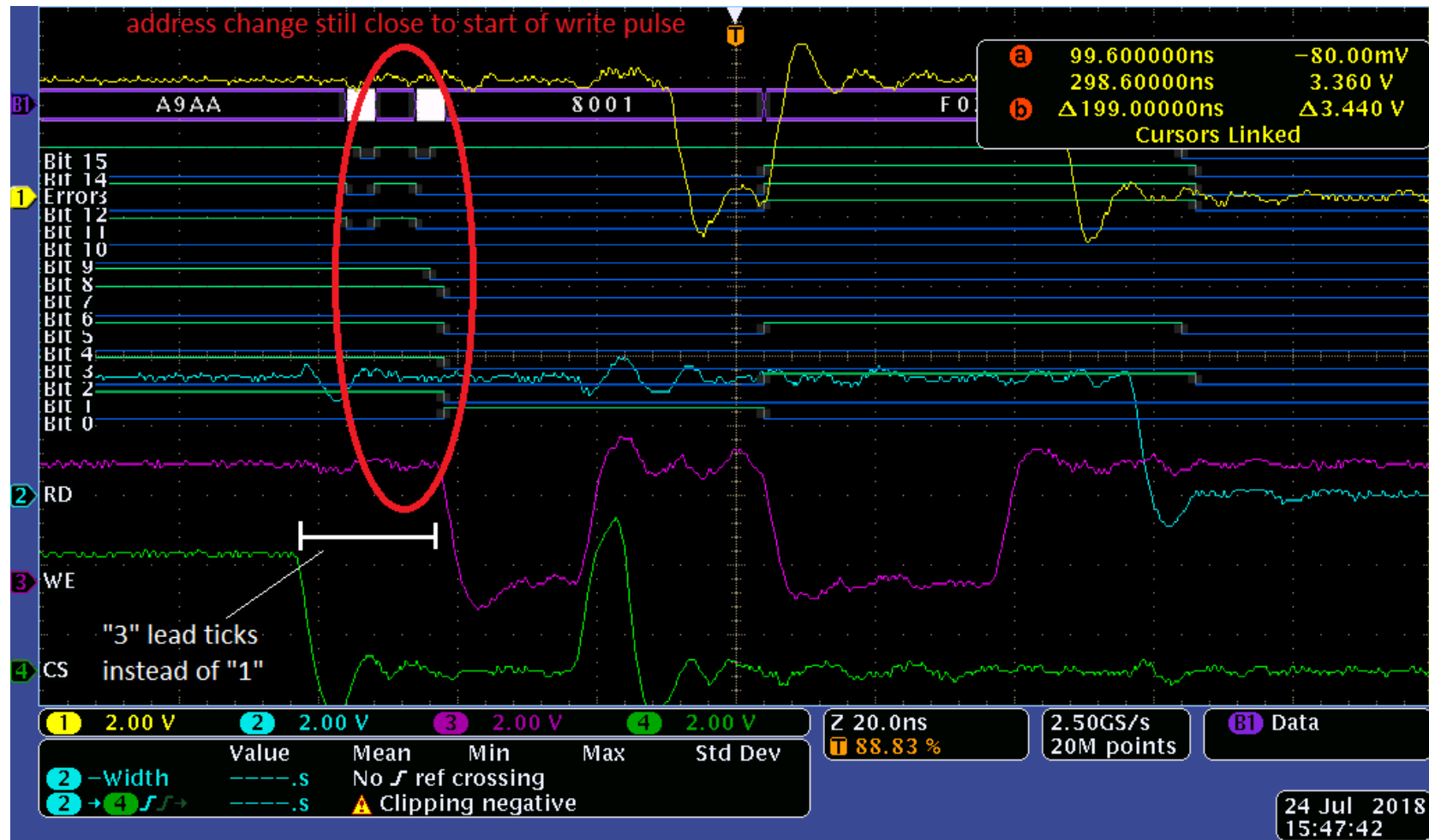


Figure 8: Scope measurement of correct data read after XWRLEAD tick change from "1" to "3"
 xReady (yellow), nRead (cyan), nWrite (magenta), nCS (green), parallel bus (violet)

Question 5	Can you explain, why the change of XWRLEAD solves the issue, although timing of data/address lines seems to be unchanged in relation to Write pulse.
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