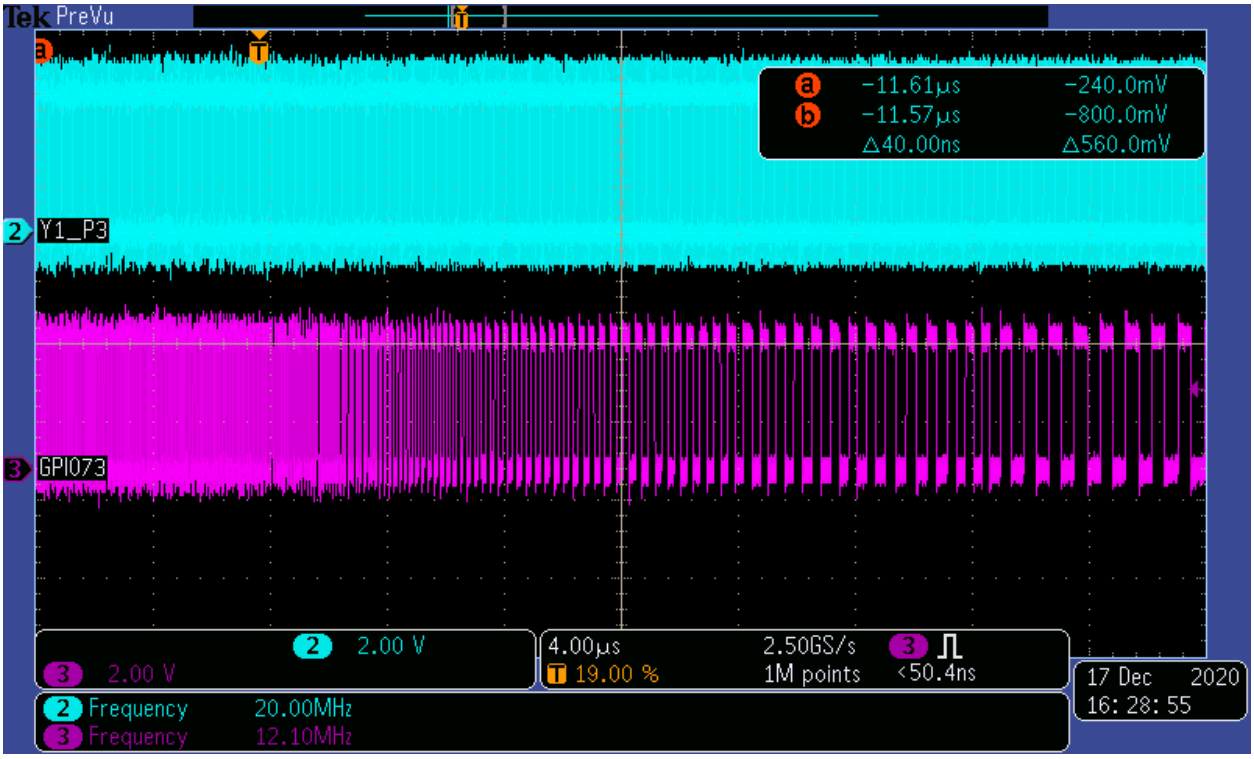
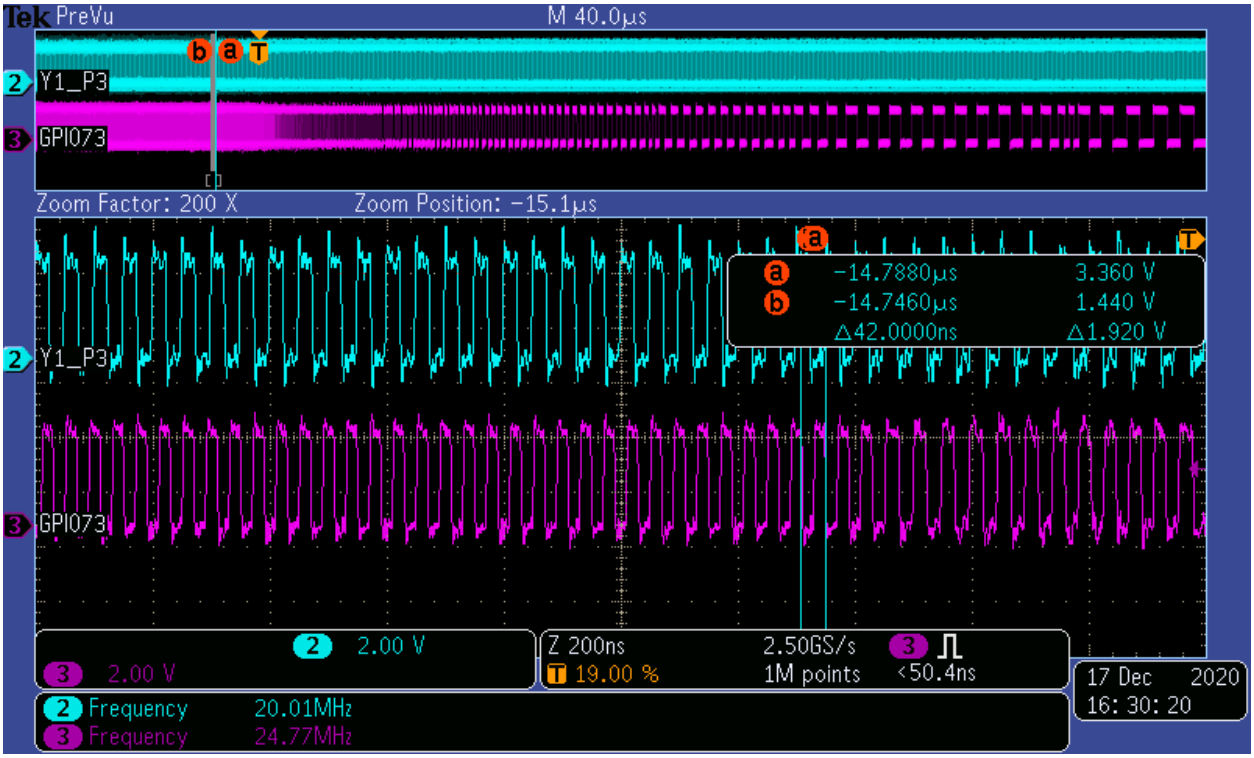
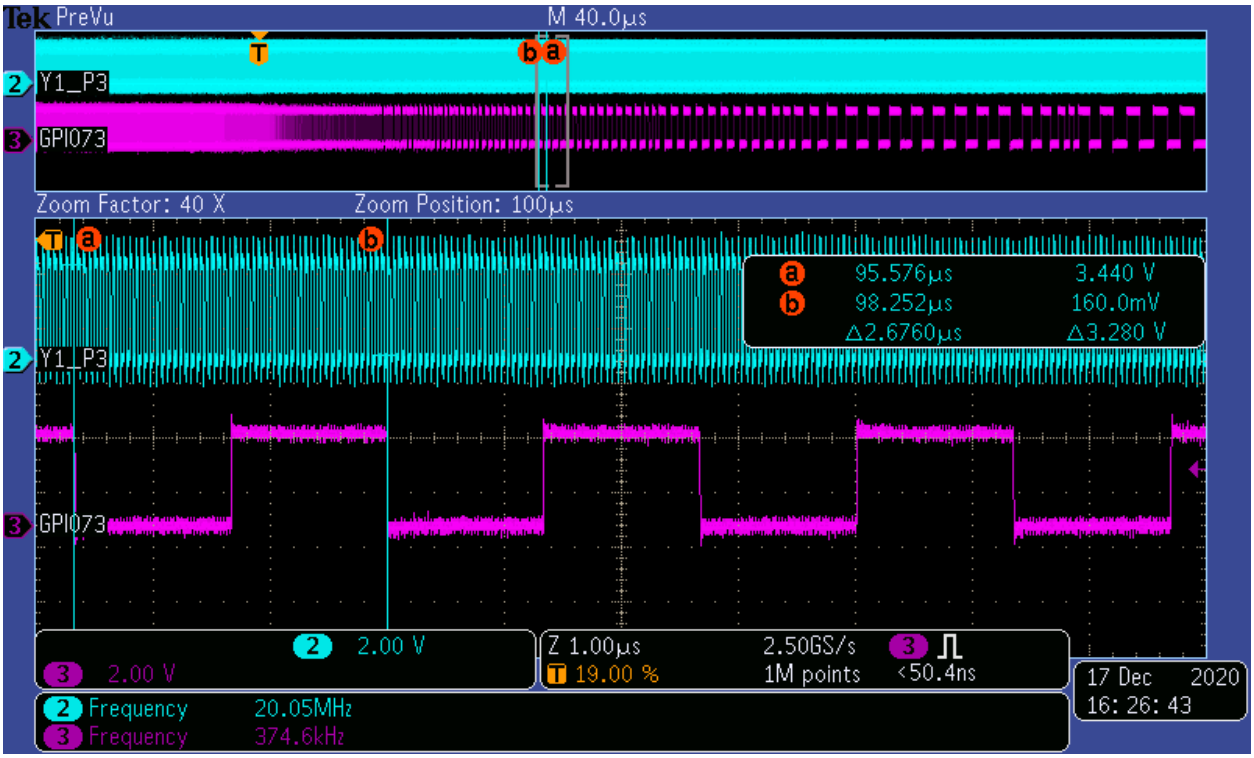
TEST 1

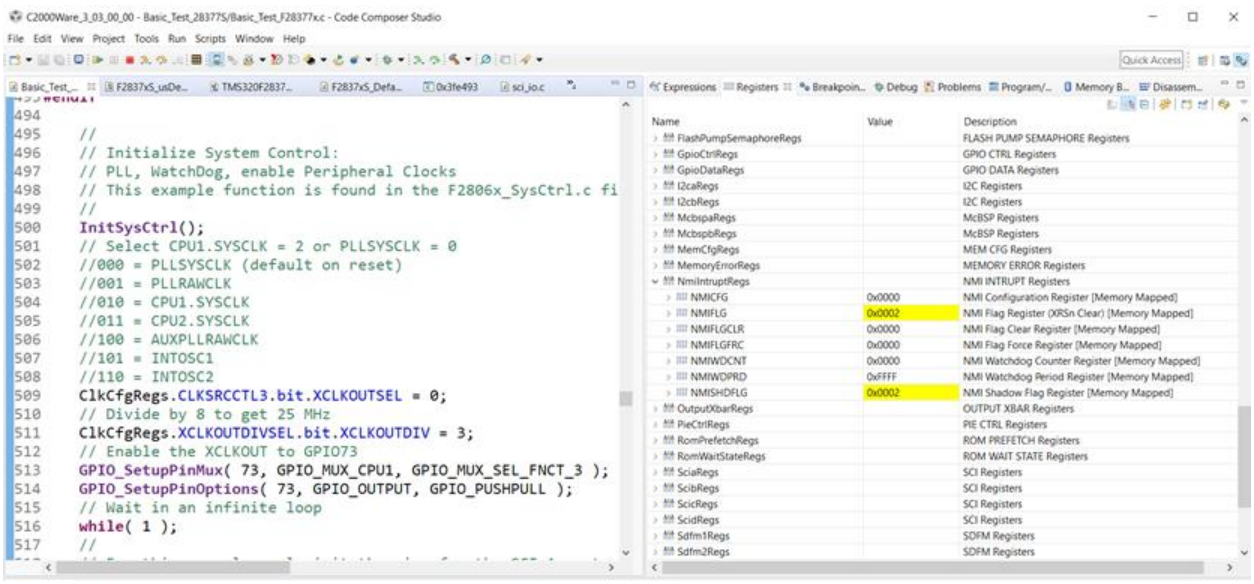
- Run the application with our standard configuration where external 20MHz oscillator clock is used at X1 pin to generate 200MHz PLLSYSCLK.
- PLLSYSCLK was divided by 8 and routed as 25MHz signal to XCLKOUT (GPIO73)
- We had oscilloscope probes on both X1 and XCLKOUT (GPIO73)
- As the chamber temperature was being reduced we observed that at around -18°C the XCLKOUT (GPIO73) signal frequency changed from 25MHz down to 374kHz within 4ms. Blue trace below is external clock signal, while pink trace is XCLKOUT (GPIO73).







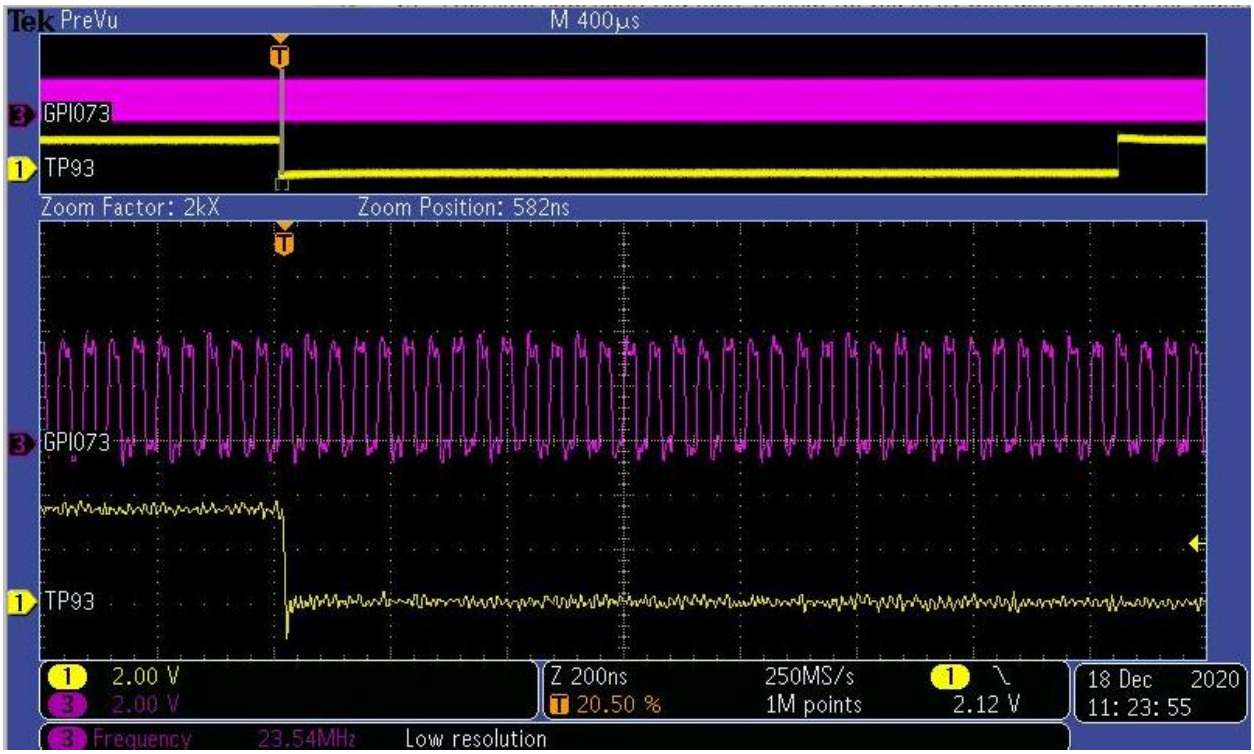
- CLOCKFAIL flag was set in NMIFLG register



TEST 2

If INTOSC1 or INTOSC2 is used as the clock source, then the maximum frequency is 194 MHz

- Run the application with internal clock used to generate 190MHz PLLSYSCLK.
- PLLSYSCLK was divided by 8 and routed as 23.75MHz signal to XCLKOUT (GPIO73)
- We had oscilloscope probe on XCLKOUT (GPIO73) and GPIO109 (TP93) which is a "hart beat" 2.5Hz signal that our application generates.



- We were able to run down to below -30°C without any change to the XCLKOUT (GPIO73) signal frequency.