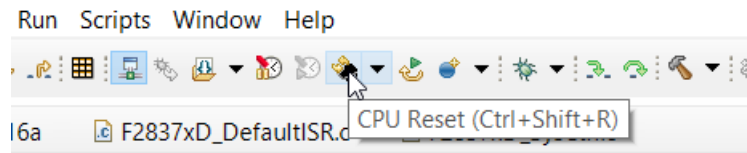


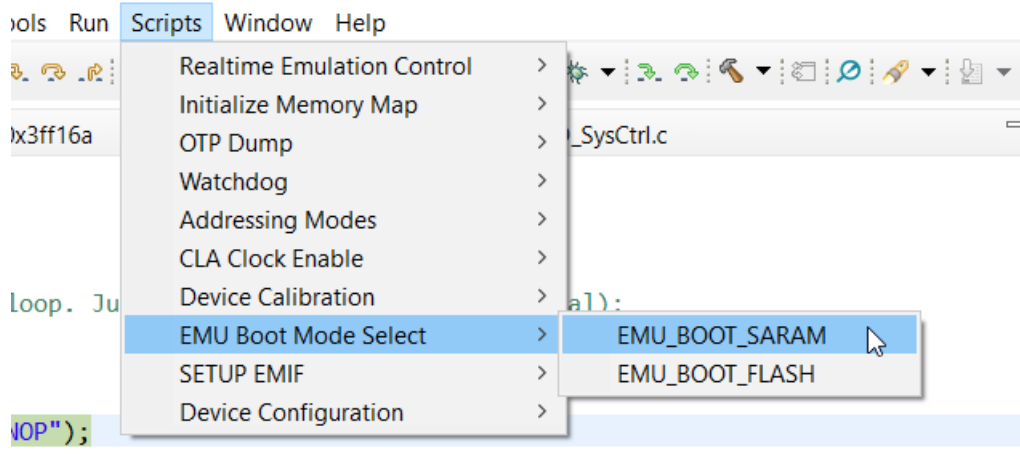
The reset is issued from the debugger.

ger\_dc/timer\_ext\_trigger.c - Code Composer Studio

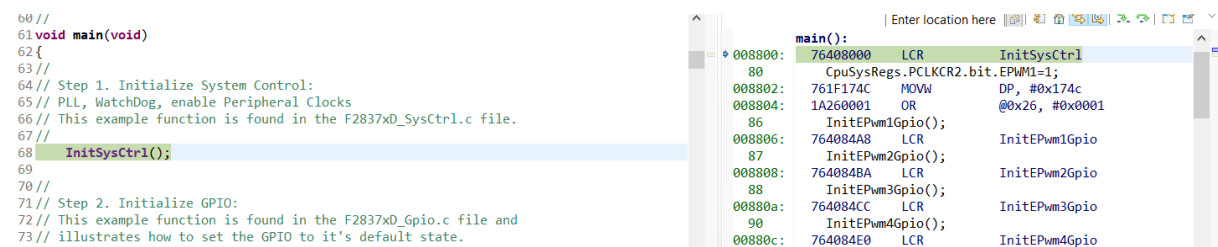


After that the EMU\_BOOT MODE is switched to SARAM

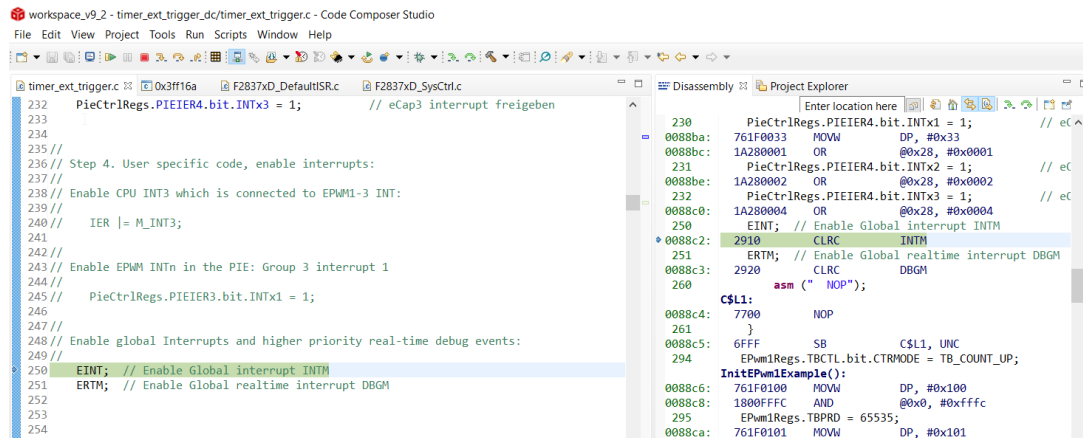
t\_trigger\_dc/timer\_ext\_trigger.c - Code Composer Studio



I have insert a breakpoint at main(). The DSP runs to this point.

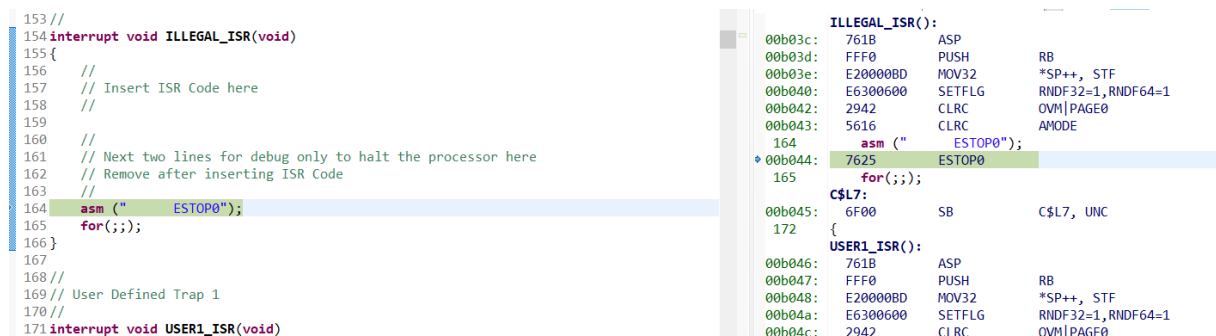


After that it is possible to step through the code until EINT is reached. Until this point everything is OK



The screenshot shows the Code Composer Studio interface. On the left, the C source file `timer_ext_trigger.c` is open, showing lines 232 to 254. Line 250, `EINT; // Enable Global interrupt INTM`, is highlighted. On the right, the disassembly view shows the corresponding assembly instructions. Line 250 corresponds to `2910 CLRC INTM`, which is also highlighted. Other visible assembly instructions include `761F0033 MOVW DP, #0x33`, `1A280001 OR @0x28, #0x0001`, `1A280002 OR @0x28, #0x0002`, `1A280004 OR @0x28, #0x0004`, `2910 CLRC INTM`, `2920 CLRC DBGM`, `7700 NOP`, `6FFF SB C$L1, UNC`, `EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;`, `761F0100 MOVW DP, #0x100`, `1800FFC AND @0x0, #0xfffc`, and `761F0101 MOVW DP, #0x101`.

After pressing the “Resume (F8)” button the DSP runs to the Illegal ISR.



The screenshot shows the Code Composer Studio interface. On the left, the C source file `timer_ext_trigger.c` is open, showing lines 153 to 171. Line 154, `void ILLEGAL_ISR(void)`, is highlighted. On the right, the disassembly view shows the assembly instructions for the `ILLEGAL_ISR()` function. Line 154 corresponds to `7625 ESTOP0`, which is also highlighted. Other visible assembly instructions include `7618 ASP`, `FFF0 PUSH RB`, `E2000BD MOV32 *SP++, STF`, `E6300600 SETFLG RNDf32=1, RNDf64=1`, `2942 CLRC OVM|PAGE0`, `5616 CLRC AMODE`, `asm ("ESTOP0");`, `7625 ESTOP0`, `for(;;);`, `6F00 SB C$L7, UNC`, `7618 ASP`, `FFF0 PUSH RB`, `E2000BD MOV32 *SP++, STF`, `E6300600 SETFLG RNDf32=1, RNDf64=1`, and `2942 CLRC OVM|PAGE0`.

Single Step is possible! In this case the Illegal ISR is not reached.