USB 2.0 Board Design and Layout Guidelines

DSPS Applications

ABSTRACT

This application report discusses schematic guidelines when designing a universal serial bus (USB) system.

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1   Background

Clock frequencies generate the main source of energy in a USB design. The USB differential DP/DM pairs operate in high-speed mode at 480 Mbps. System clocks can operate at 12 MHz, 48 MHz, and 60 MHz. The USB cable can behave as a monopole antenna; take care to prevent RF currents from coupling onto the cable.

When designing a USB board, the signals of most interest are:

- Device interface signals: Clocks and other signal/data lines that run between devices on the PCB.
- Power going into and out of the cable: The USB connector socket pin 1 (VBUS) may be heavily filtered and need only pass low frequency signals of less than ~100 KHz. The USB socket pin 4 (analog ground) must be able to return the current during data transmission, and must be filtered sparingly.
- Differential twisted pair signals going out on cable, DP and DM: Depending upon the data transfer rate, these device terminals can have signals with fundamental frequencies of 240 MHz (high speed), 6 MHz (full speed), and 750 kHz (low speed).
- External crystal circuit (device terminals XI and X0): 12 MHz, 19.2 MHz, 24 MHz, and 48 MHz fundamental. When using an external crystal as a reference clock, a 24 MHz and higher crystal is highly recommended.

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2 USB PHY Layout Guide

The following sections describe in detail the specific guidelines for USB PHY Layout.

2.1 General Routing and Placement

Use the following routing and placement guidelines when laying out a new design for the USB physical layer (PHY). These guidelines help minimize signal quality and electromagnetic interference (EMI) problems on a four-or-more layer evaluation module (EVM).

- Place the USB PHY and major components on the un-routed board first. For more details, see Section 2.2.3.
- Route the high-speed clock and high-speed USB differential signals with minimum trace lengths.
- Route the high-speed USB signals on the plane closest to the ground plane, whenever possible.
- Route the high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.
- Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mils.
- Route all high-speed USB signal traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch, commonly found with plane splits.

2.2 Specific Guidelines for USB PHY Layout

The following sections describe in detail the specific guidelines for USB PHY Layout.

2.2.1 Analog, PLL, and Digital Power Supply Filtering

To minimize EMI emissions, add decoupling capacitors with a ferrite bead at power supply terminals for the analog, phase-locked loop (PLL), and digital portions of the chip. Place this array as close to the chip as possible to minimize the inductance of the line and noise contributions to the system. An analog and digital supply example is shown in Figure 1. In case of multiple power supply pins with the same function, tie them up to a single low-impedance point in the board and then add the decoupling capacitors, in addition to the ferrite bead. This array of caps and ferrite bead improve EMI and jitter performance. Take both EMI and jitter into account before altering the configuration.
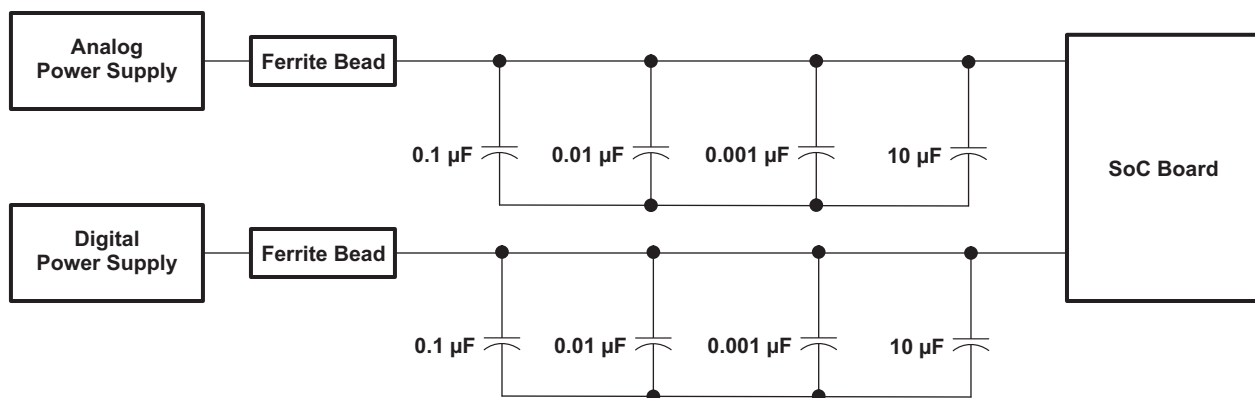

Figure 1. Suggested Array Capacitors and a Ferrite Bead to Minimize EMI

Consider the recommendations listed below to achieve proper ESD/EMI performance:

- Use a 0.01 µF cap on each cable power VBUS line to chassis GND close to the USB connector pin.
- Use a 0.01 µF cap on each cable ground line to chassis GND next to the USB connector pin.
- If voltage regulators are used, place a 0.01 µF cap on both input and output. This is to increase the immunity to ESD and reduce EMI. For other requirements, see the device-specific datasheet.

2.2.2 Analog, Digital, and PLL Partitioning

If separate power planes are used, they must be tied together at one point through a low-impedance bridge or preferably through a ferrite bead. Care must be taken to capacitively decouple each power rail close to the device. The analog ground, digital ground, and PLL ground must be tied together to the low-impedance circuit board ground plane.

2.2.3 Board Stackup

Because of the high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 2.
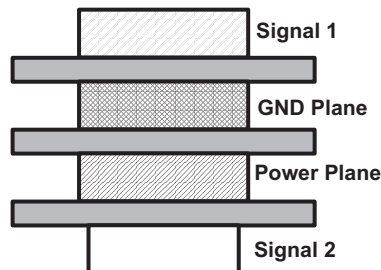

Figure 2. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

2.2.4 Cable Connector Socket

Short the cable connector sockets directly to a small chassis ground plane (GND *strap*) that exists immediately underneath the connector sockets. This shorts EMI (and ESD) directly to the chassis ground before it gets onto the USB cable. This etch plane should be as large as possible, but all the conductors coming off connector pins 1 through 6 must have the board signal GND plane run under. If needed, scoop out the chassis GND strap etch to allow for the signal ground to extend under the connector pins. Note that the etches coming from pins 1 and 4 (VBUS power and GND) should be wide and via-ed to their respective planes as soon as possible, respecting the filtering that may be in place between the connector pin and the plane. See Figure 3 for a schematic example.

Place a ferrite in series with the cable shield pins near the USB connector socket to keep EMI from getting onto the cable shield. The ferrite bead between the cable shield and ground may be valued between 10 Ω and 50 Ω at 100 MHz; it should be resistive to approximately 1 GHz. To keep EMI from getting onto the cable bus power wire (a very large antenna) a ferrite may be placed in series with cable bus power, VBUS, near the USB connector pin 1. The ferrite bead between connector pin 1 and bus power may be valued between 47 Ω and approximately 1000 Ω at 100 MHz. It should continue being resistive out to approximately 1 GHz, as shown in Figure 3.
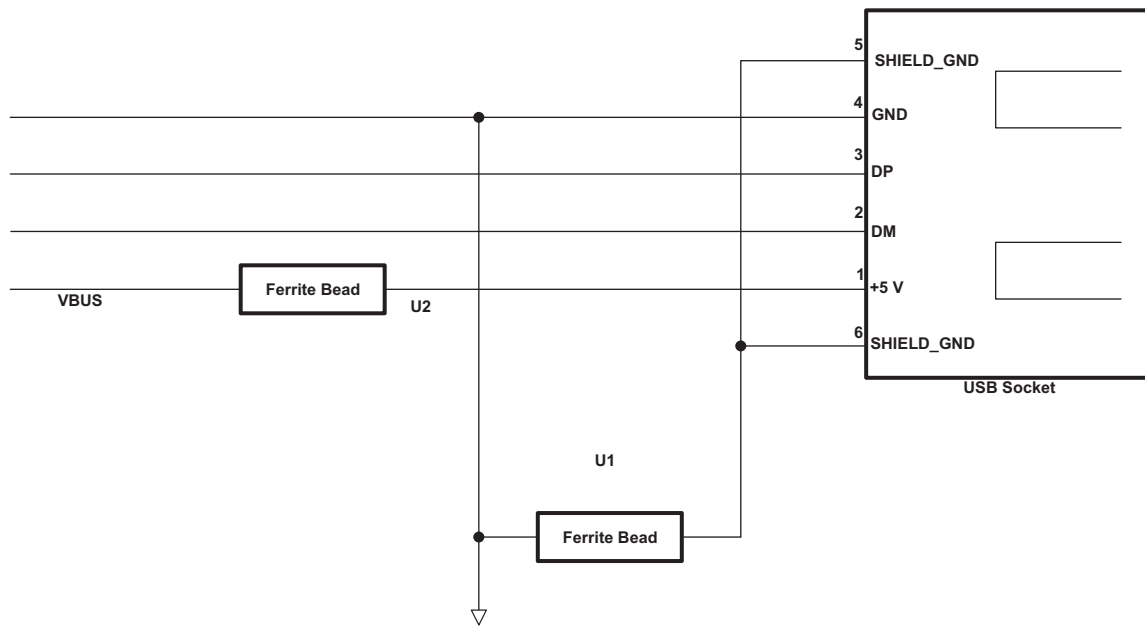
Figure 3. USB Connector

2.2.5 Clock Routings

To address the system clock emissions between devices, place a ~10 to 130 Ω resistor in series with the clock signal. Use a trial and error method of looking at the shape of the clock waveform on a high-speed oscilloscope and of tuning the value of the resistance to minimize waveform distortion. The value on this resistor should be as small as possible to get the desired effect. Place the resistor close to the device generating the clock signal. If an external crystal is used, follow the guidelines detailed in the *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122).

When routing the clock traces from one device to another, try to use the 3W spacing rule. The distance from the center of the clock trace to the center of any adjacent signal trace should be at least three times the width of the clock trace. Many clocks, including slow frequency clocks, can have fast rise and fall times. Using the 3W rule cuts down on crosstalk between traces. In general, leave space between each of the traces running parallel between the devices. Avoid using right angles when routing traces to minimize the routing distance and impedance discontinuities. For further protection from crosstalk, run guard traces beside the clock signals (GND pin to GND pin), if possible. This lessens clock signal coupling, as shown in Figure 4.
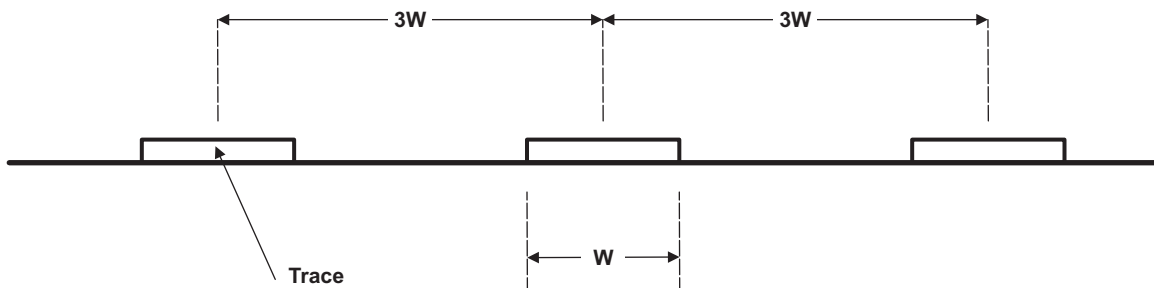
Figure 4. 3W Spacing Rule

2.2.6 Crystals/Oscillator

Keep the crystal and its load capacitors close to the USB PHY pins, XI and XO (see Figure 5). Note that frequencies from power sources or large capacitors can cause modulations within the clock and should not be placed near the crystal. In these instances, errors such as dropped packets occur. A placeholder for a resistor, in parallel with the crystal, can be incorporated in the design to assist oscillator startup.

Power is proportional to the current squared. The current is $I = C*dv/dt$, since dv/dt is a function of the PHY, current is proportional to the capacitive load. Cutting the load to 1/2 decreases the current by 1/2 and the power to 1/4 of the original value. For more details on crystal selection, see the *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122).
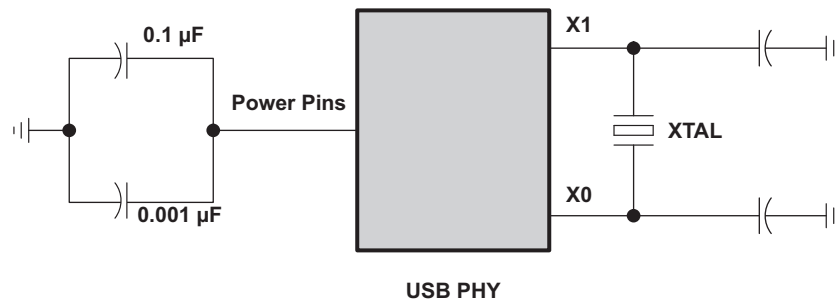
Figure 5. Power Supply and Clock Connection to the USB PHY

2.2.7 DP/DM Trace

Place the USB PHY as close as possible to the USB 2.0 connector. The signal swing during high-speed operation on the DP/DM lines is relatively small (400 mV ± 10%), so any differential noise picked up on the twisted pair can affect the received signal. When the DP/DM traces do not have any shielding, the traces tend to behave like an antenna and picks up noise generated by the surrounding components in the environment. To minimize the effect of this behavior:

- DP/DM traces should always be matched lengths and must be no more than 4 inches in length; otherwise, the eye opening may be degraded (see Figure 6).
- Route DP/DM traces close together for noise rejection on differential signals, parallel to each other and within two mils in length of each other (start the measurement at the chip package boundary, not to the balls or pins).
- A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance of 90 Ω ±15%. In layout, the impedance of DP and DM should each be 45 Ω ± 10%.
- DP/DM traces should not have any extra components to maintain signal integrity. For example, traces cannot be routed to two USB connectors.
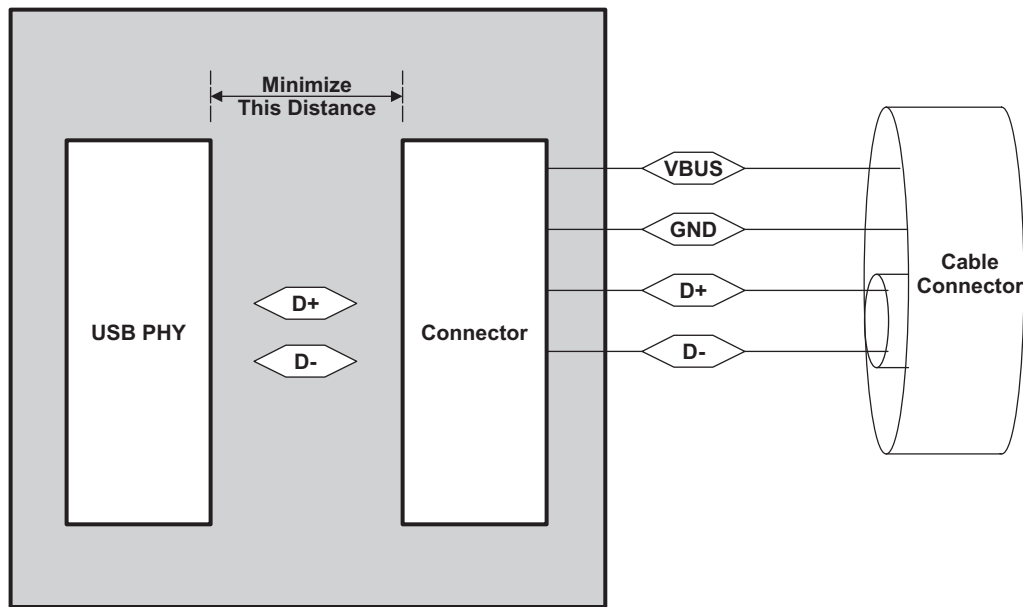
Figure 6. USB PHY Connector and Cable Connector

2.2.8   DP/DM Vias

When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

2.2.9   Image Planes

An image plane is a layer of copper (voltage plane or ground plane), physically adjacent to a signal routing plane. Use of image planes provides a low impedance, shortest possible return path for RF currents. For a USB board, the best image plane is the ground plane because it can be used for both analog and digital circuits.

- Do not route traces so they cross from one plane to the other. This can cause a broken RF return path resulting in an EMI radiating loop as shown in Figure 7. This is important for higher frequency or repetitive signals. Therefore, on a multi-layer board, it is best to run all clock signals on the signal plane above a solid ground plane.
- Avoid crossing the image power or ground plane boundaries with high-speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals (DP, DM). Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through vias.
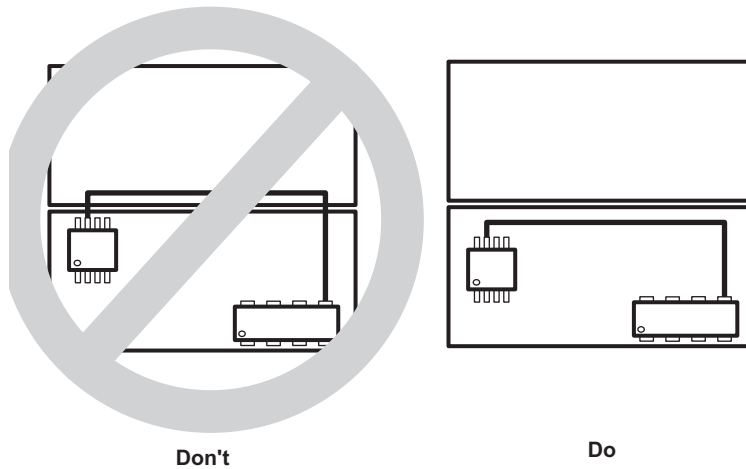
Figure 7. Do Not Cross Plane Boundaries

- Do not overlap planes that do not reference each other. For example, do not overlap a digital power plane with an analog power plane as this produces a capacitance between the overlapping areas that could pass RF emissions from one plane to the other, as shown in Figure 8.
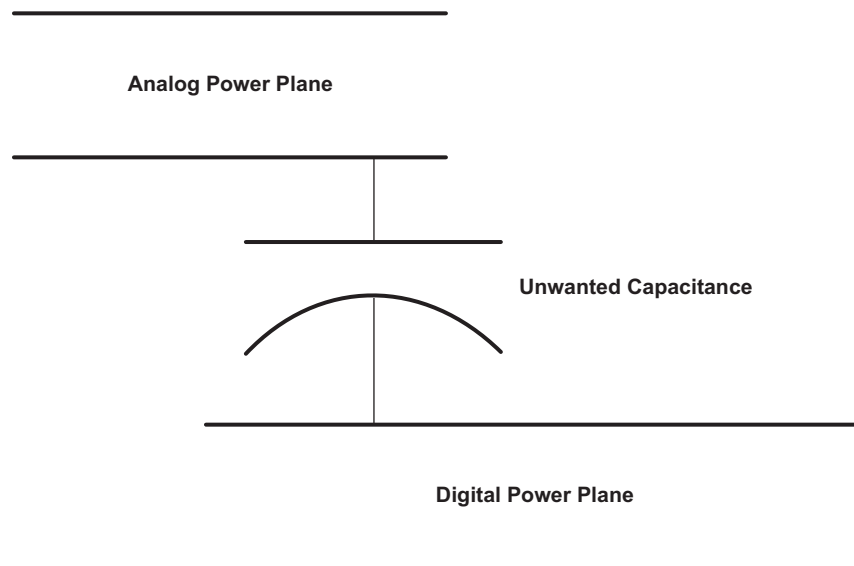
Figure 8. Do Not Overlap Planes

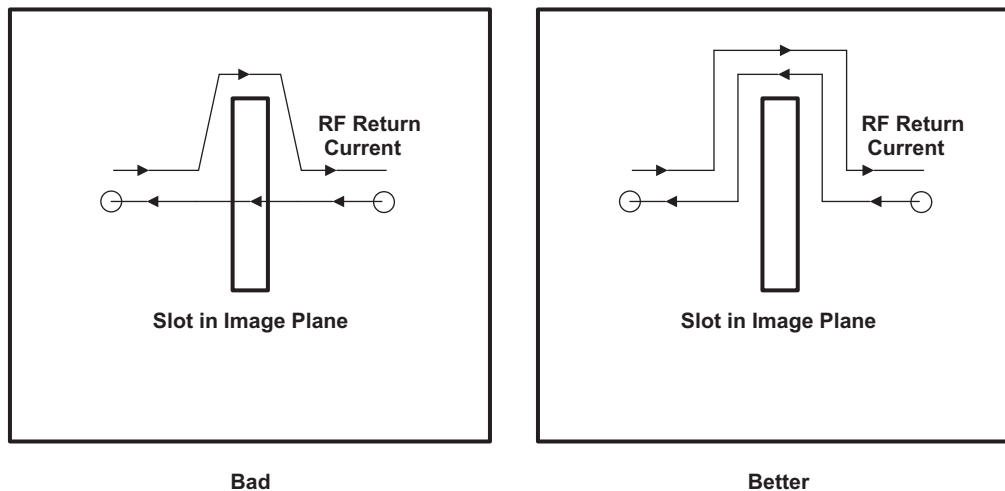- Avoid image plane violations. Traces that route over a slot in an image plane results in a possible RF return loop, as shown in Figure 9.

Figure 9. Do Not Violate Image Planes

2.2.10 JTAG Interface

For test and debug of the USB PHY only, an IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) and Serial Test and Configuration Interface (STCI) may be available on the System-on-Chip (SoC). If available, keep the USB PHY JTAG interface less than six inches; keeping this distance short reduces noise coupling from other devices and signal loss due to resistance.

2.2.11 Power Regulators

Switching power regulators are a source of noise and can cause noise coupling if placed close to sensitive areas on a circuit board. Therefore, the switching power regulator should be kept away from the DP/DM signals, the external clock crystal (or clock oscillator), and the USB PHY.

3 Electrostatic Discharge (ESD)

International Electronic Commission (IEC) 61000-4-xx is a set of about 25 testing specifications from the IEC. IEC ESD Stressing is done both un-powered and with power applied, and with the device functioning. There must be no physical damage, and the device must keep working normally after the conclusion of the stressing. Typically, equipment has to pass IEC stressing at 8 kV contact and 15 kV air discharge, or higher. To market products/systems in the European community, all products/systems must be CE compliant and have the CE Mark. To obtain the CE Mark, all products/systems need to go through and pass IEC standard requirements; for ESD, it is 61000-4-2. 61000-4-2 requires that the products/systems pass contact discharge at 8 kV and air discharge at 15 kV. When performing an IEC ESD Stressing, only pins accessible to the *outside world* need to pass the test. The system into which the integrated circuit (IC) is placed makes a difference in how well the IC does. For example:

- Cable between the zap point and the IC attenuate the high frequencies in the waveform.
- Series inductance on the PCB board attenuates the high frequencies.
- Unless the capacitor's ground connection is inductive, capacitance to ground shunts away high frequencies.

3.1 IEC ESD Stressing Test

The following sections describe in detail the IEC ESD Stressing Test modes and test types.

3.1.1 Test Mode

The IEC ESD Stressing test is done through two modes: contact discharge mode and air discharge mode.

For the contact discharge test mode, the preferred way is direct contact applied to the conductive surfaces of the equipment under test (EUT). In the case of the USB system, the conductive surface is the outer casing of the USB connector. The electrode of the ESD generator is held in contact with the EUT or a coupling plane prior to discharge. The arc formation is created under controlled conditions, inside a relay, resulting in repeatable waveforms; however, this arc does not accurately recreate the characteristic unique to the arc of an actual ESD event.

3.1.2 Air Discharge Mode

The air discharge usually applies to a non-conductive surface of the EUT. Instead of a direct contact with the EUT, the charged electrode of the ESD generator is brought close to the EUT, and a spark in the air to the EUT actuates the discharge. Compared to the contact discharge mode, the air discharge is more realistic to the actual ESD occurrence. However, due to the variations of the arc length, it may not be able to produce repeatable waveform.

3.1.3 Test Type

The IEC ESD Stressing test has two test types: direct discharge and indirect discharge. Direct discharge is applies directly to the surface or the structure of the EUT. It includes both contact discharge and air discharge modes. Indirect discharge applies to a coupling plane in the vicinity of the EUT. The indirect discharge is used to simulate personal discharge to objects which are adjacent to the EUT. It includes contact discharge mode only.

3.2 TI Component Level IEC ESD Test

TI Component Level IEC ESD Test tests only the IC terminals that are exposed in system level applications. It can be used to determine the robustness of on-chip protection and the latch-up immunity. The IC can only pass the TI Component Level IEC ESD test when there is no latch-up and IC is fully functional after the test.

3.3 Construction of a Custom USB Connector

A standard USB connector, either type A or type B, provides good ESD protection. However, if a custom USB connector is desired, the following guidelines should be observed to ensure good ESD protection.

- There should be an easily accessible shield plate next to the connector for air-discharge mode purpose.
- Tie the outer shield of the connector to GND. When a cable is inserted into the connector, the shield of the cable should first make contact with the outer shield.
- If the connector includes power and GND, the lead of power and GND need to be longer than the leads of signal.
- The connector needs to have a key to ensure proper insertion of the cable.
- See the standard USB connector for reference.

3.4 ESD Protection System Design Consideration

ESD protection system design consideration is covered in Section 2 of this document. The following are additional considerations for ESD protection in a system.

- Metallic shielding for both ESD and EMI
- Chassis GND isolation from the board GND
- Air gap designed on board to absorb ESD energy
- Clamping diodes to absorb ESD energy
- Capacitors to divert ESD energy
- The use of external ESD components on the DP/DM lines may affect signal quality and are not recommended.

4 References

- *USB 2.0 Specification*, Intel, 2000, http://www.usb.org/developers/docs/
- *High Speed USB Platform Design Guidelines*, Intel, 2000, http://www.intel.com/technology/usb/download/usb2dg_R1_0.pdf
- *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (SLLA122)

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