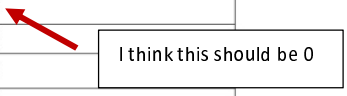
## Table 3-4. Register Pairs Saved and SP Positions for Context Saves

| Save Operation [1] | Register Pairs | Bit 0 of Storage Address SP Starts at Odd Address | SP Starts at Even Address |
|---|---|---|---|
| | | 1 SP position before step 8 | 1 |
| 1st | STO | 0 | 0 SP position before step 8 |
| | T | 1 | 1 |
| 2nd | AL | 0 | 0 |
| | AH | 1 | 1 |
| 3rd | PL [2] | 0 | 0 |
| | PH | 1 | 1 |
| 4th | AR0 | 0 | 0 |
| | AR1 | 1 | 1 |
| 5th | ST1 | 0 | 1 |
| | DP | 1 | 1 |
| 6th | IER | 0 | 0 |
| | DBGSTAT [3] | 1 | 1 |
| 7th | Return address (low half) | 0 | 0 |
| | Return address (high half) | 1 | 1 |
| | | 0 SP position after save | 0 |
| | | 1 | 1 SP position after save |




(1) All registers are saved as pairs, as shown.
(2) The P register is saved with 0 shift (CPU ignores current state of the product shift mode bits, PM, in status register 0).
(3) The DBGSTAT register contains special emulation information.