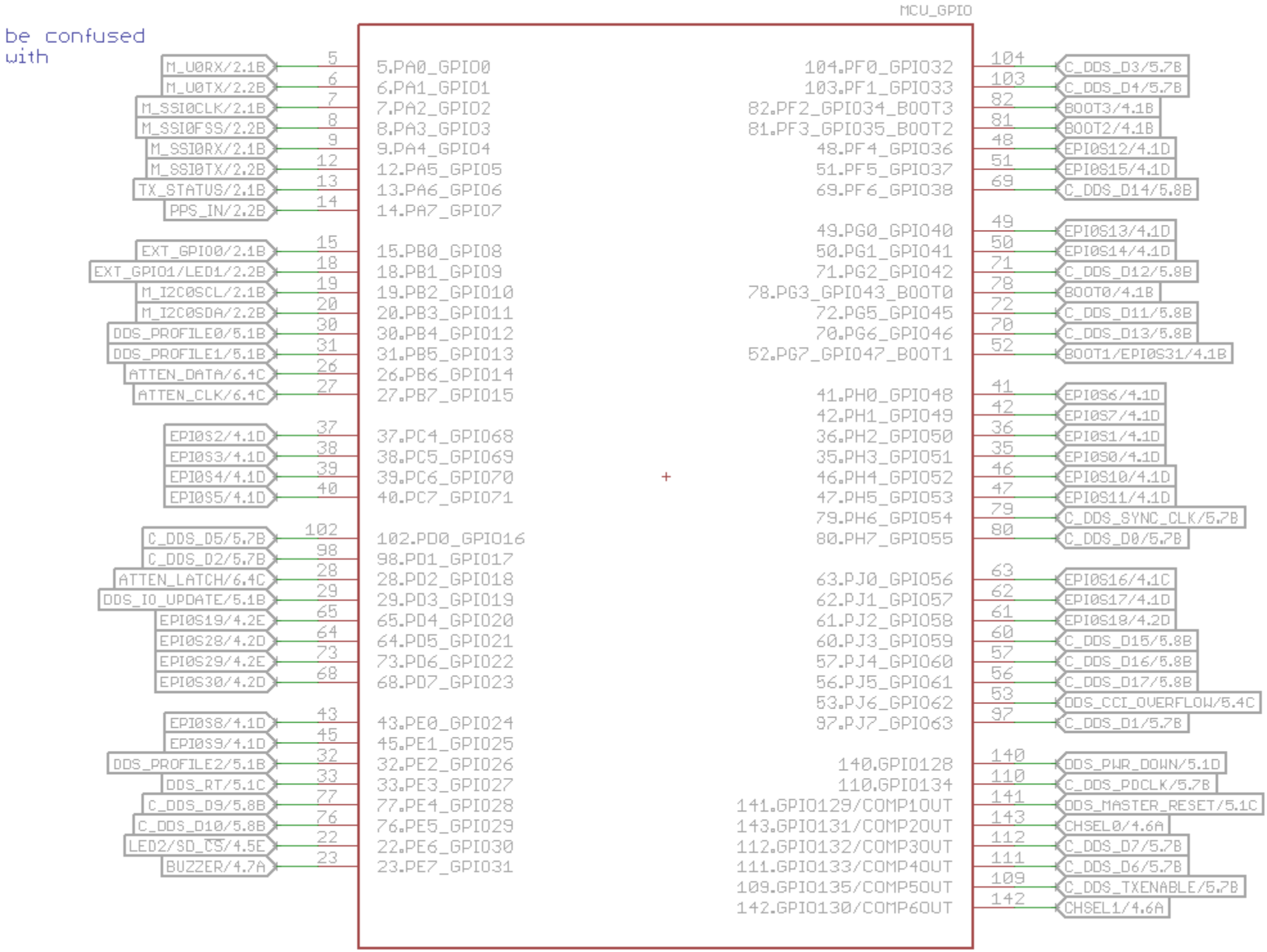
be confused
with

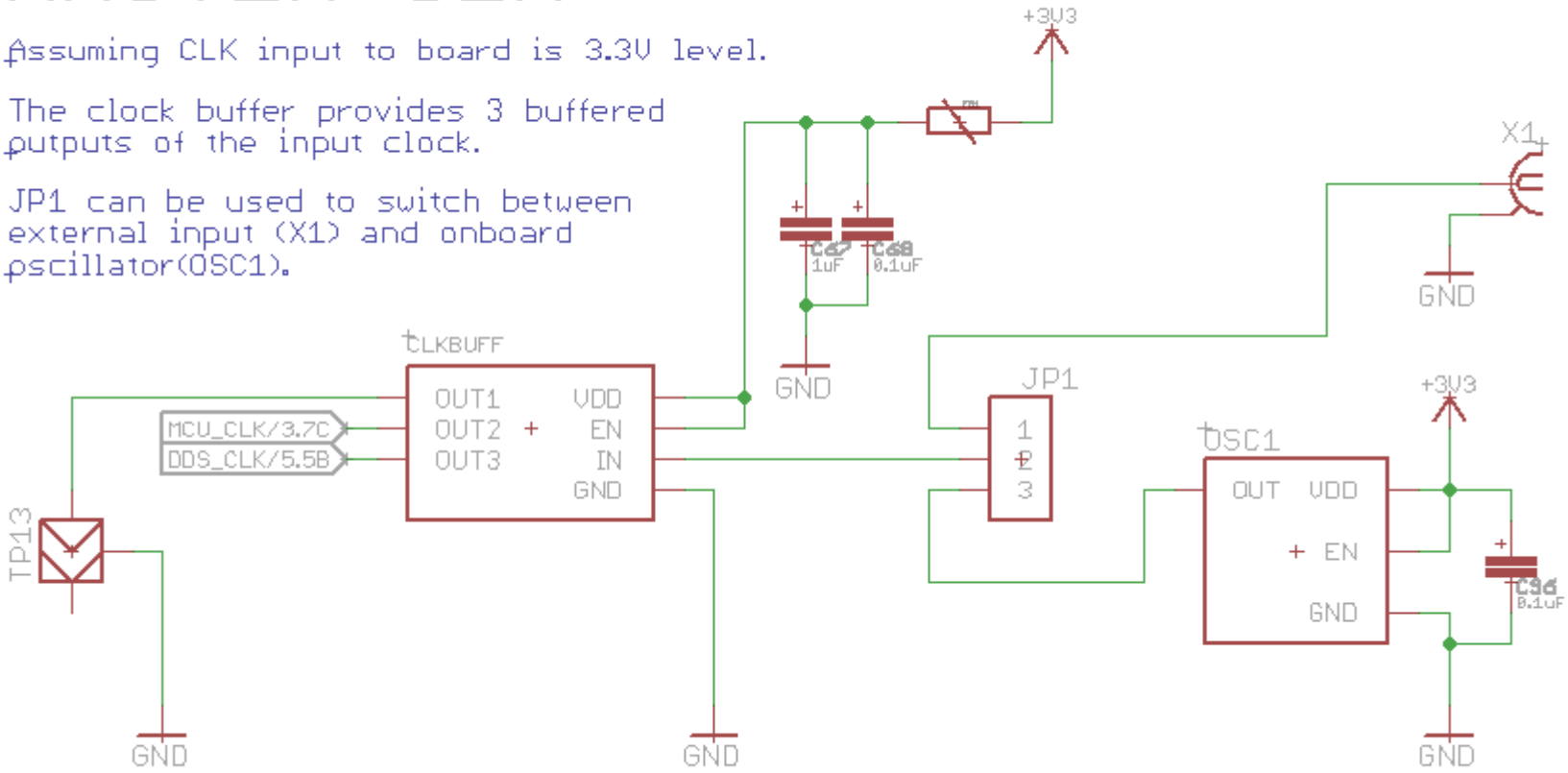


MASTER CLK

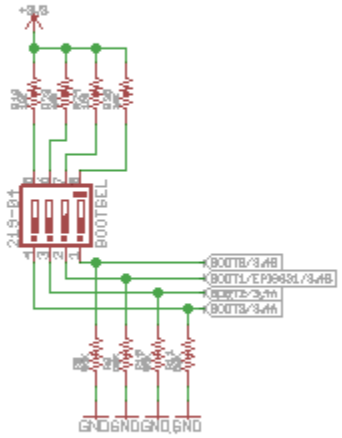
Assuming CLK input to board is 3.3V level.

The clock buffer provides 3 buffered outputs of the input clock.

JP1 can be used to switch between external input (X1) and onboard oscillator(OSC1).



BOOT SELECT

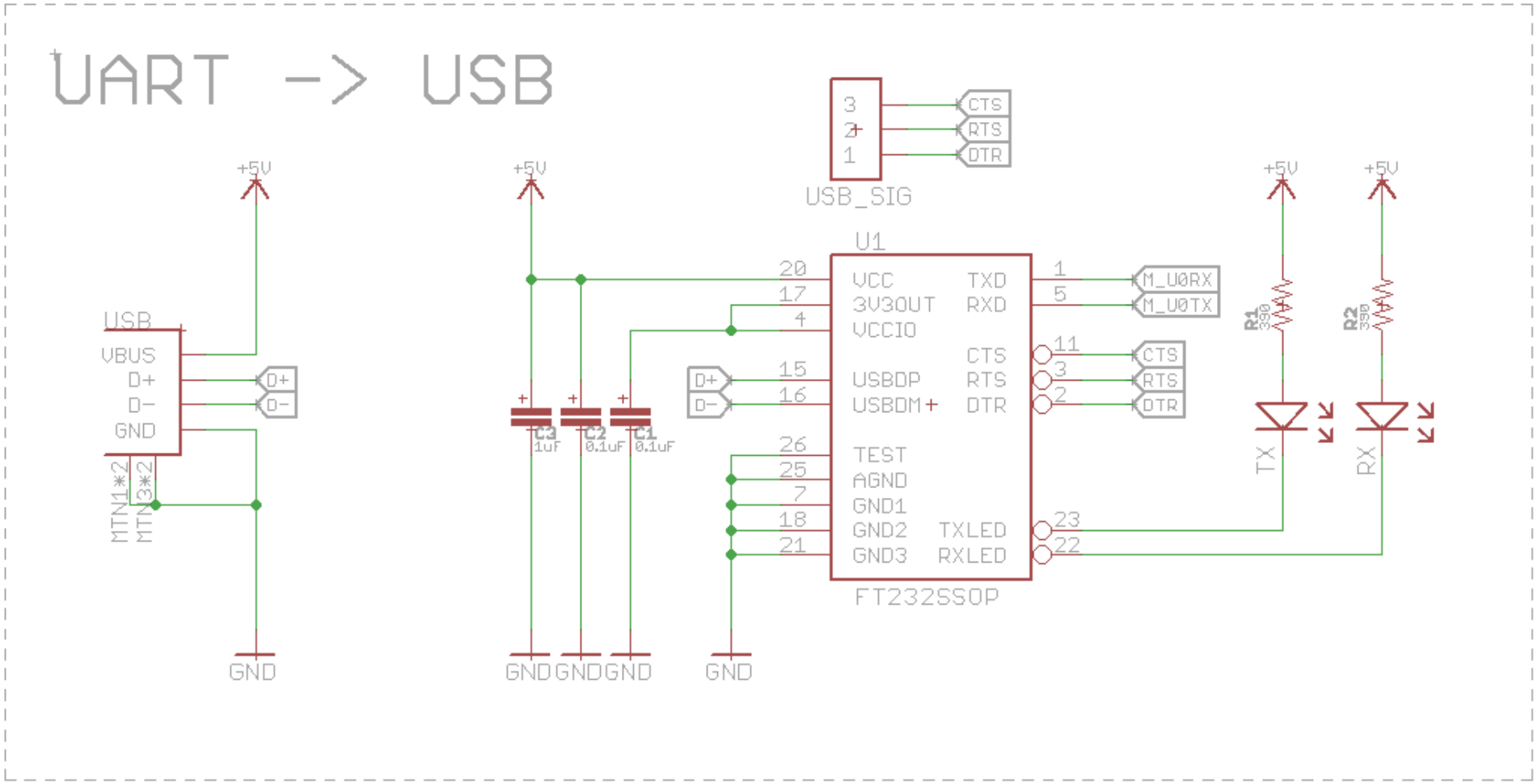


For nominal use, BOOTSEL is set to 0b0111.
This boots from Flash.

BOOT0 and BOOT2 are also available and controllable through the the MAINBOARD header. For example, setting BOOT0 and BOOT2 to 0 makes the MCU boot from serial peripherals.

Each of the BOOT pins can be used as GPIO post-boot. BOOT1 is already used for the EPIO interface for SDRAM. To enable this, both the on and off states of each of the DIP positions have pull-ups / pull-downs.

BOOTSEL	BOOT0	BOOT2	FUNCTION
0b0111	1	1	Boot from Flash
0b0111	0	0	Boot from Master SPI


UART -> USB
USB
VBUS
D+
D-
GND
MTN1*2
MTN3*2
+5V
GND
USB_SIG
3
2
1
CTS
RTS
DTR
U1
VCC
3V3OUT
VCCIO
USBDP
USBDM
TEST
AGND
GND1
GND2
GND3
TXD
RXD
CTS
RTS
DTR
TXLED
RXLED
20
17
4
15
16
26
25
7
18
21
1
5
11
3
2
23
22
M_U0RX
M_U0TX
FT232SSOP
C3 1uF
C2 0.1uF
C1 0.1uF
R1 330
R2 330
TX
RX