

be confused
with

M_U0RX/2.1B	5	5.PA0_GPIO0
M_U0TX/2.2B	6	6.PA1_GPIO1
M_SSI0CLK/2.1B	7	7.PA2_GPIO2
M_SSI0FSS/2.2B	8	8.PA3_GPIO3
M_SSI0RX/2.1B	9	9.PA4_GPIO4
M_SSI0TX/2.2B	12	12.PA5_GPIO5
TX_STATUS/2.1B	13	13.PA6_GPIO6
PPS_IN/2.2B	14	14.PA7_GPIO7
EXT_GPIO0/2.1B	15	15.PB0_GPIO8
EXT_GPIO1/LED1/2.2B	18	18.PB1_GPIO9
M_I2C0SCL/2.1B	19	19.PB2_GPIO10
M_I2C0SDA/2.2B	20	20.PB3_GPIO11
DDS_PROFILE0/5.1B	30	30.PB4_GPIO12
DDS_PROFILE1/5.1B	31	31.PB5_GPIO13
ATTEN_DATA/6.4C	26	26.PB6_GPIO14
ATTEN_CLK/6.4C	27	27.PB7_GPIO15
EPI0S2/4.1D	37	37.PC4_GPIO68
EPI0S3/4.1D	38	38.PC5_GPIO69
EPI0S4/4.1D	39	39.PC6_GPIO70
EPI0S5/4.1D	40	40.PC7_GPIO71
C_DDS_D5/5.7B	102	102.PD0_GPIO16
C_DDS_D2/5.7B	98	98.PD1_GPIO17
ATTEN_LATCH/6.4C	28	28.PD2_GPIO18
DDS_IO_UPDATE/5.1B	29	29.PD3_GPIO19
EPI0S19/4.2E	65	65.PD4_GPIO20
EPI0S28/4.2D	64	64.PD5_GPIO21
EPI0S29/4.2E	73	73.PD6_GPIO22
EPI0S30/4.2D	68	68.PD7_GPIO23
EPI0S8/4.1D	43	43.PE0_GPIO24
EPI0S9/4.1D	45	45.PE1_GPIO25
DDS_PROFILE2/5.1B	32	32.PE2_GPIO26
DDS_RT/5.1C	33	33.PE3_GPIO27
C_DDS_D9/5.8B	77	77.PE4_GPIO28
C_DDS_D10/5.8B	76	76.PE5_GPIO29
LED2/SD_CS/4.5E	22	22.PE6_GPIO30
BUZZER/4.7A	23	23.PE7_GPIO31

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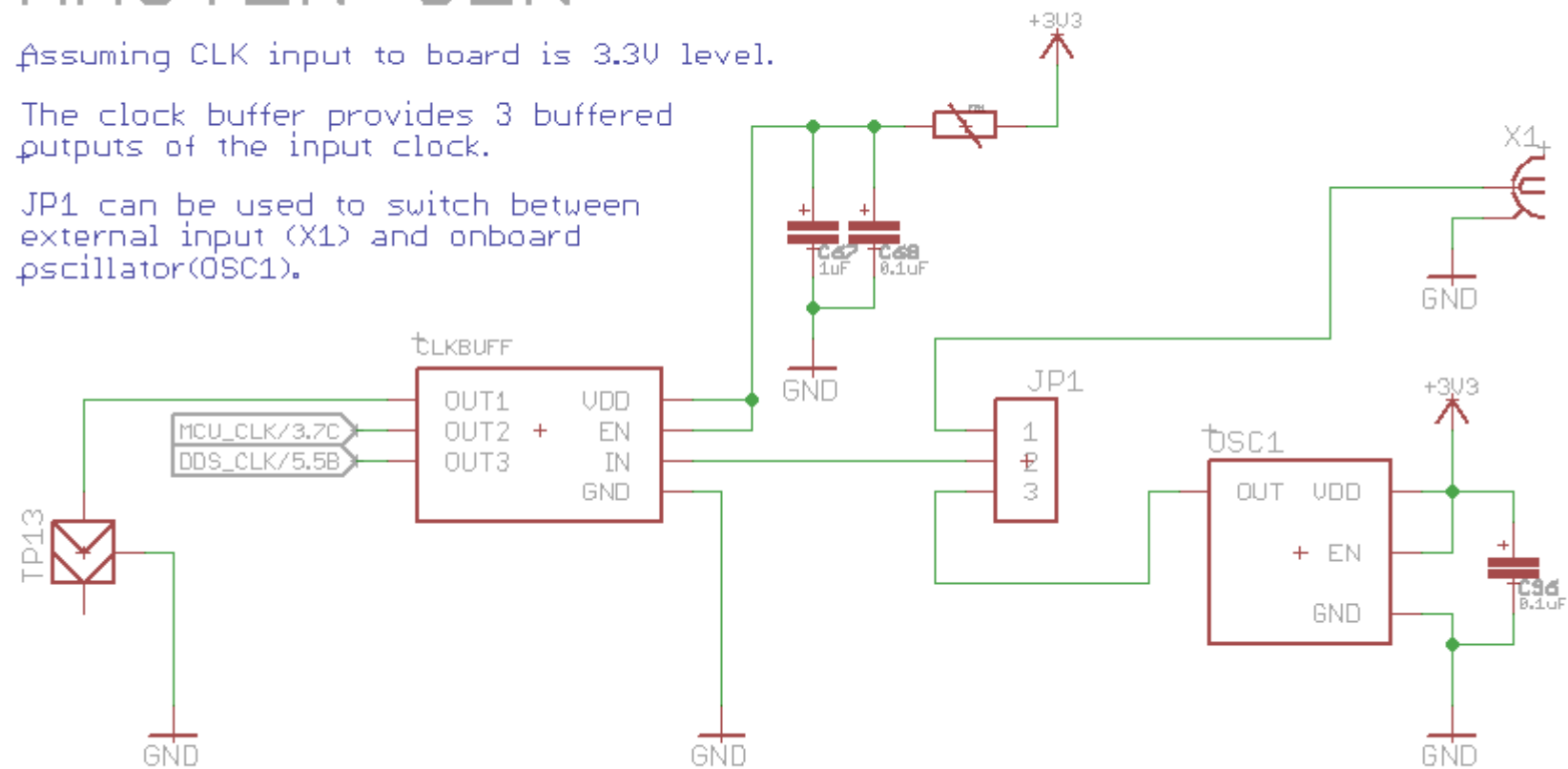
MCU_GPIO	
104.PF0_GPIO32	104 C_DDS_D3/5.7B
103.PF1_GPIO33	103 C_DDS_D4/5.7B
82.PF2_GPIO34_BOOT3	82 BOOT3/4.1B
81.PF3_GPIO35_BOOT2	81 BOOT2/4.1B
48.PF4_GPIO36	48 EPI0S12/4.1D
51.PF5_GPIO37	51 EPI0S15/4.1D
69.PF6_GPIO38	69 C_DDS_D14/5.8B
49.PG0_GPIO40	49 EPI0S13/4.1D
50.PG1_GPIO41	50 EPI0S14/4.1D
71.PG2_GPIO42	71 C_DDS_D12/5.8B
78.PG3_GPIO43_BOOT0	78 BOOT0/4.1B
72.PG5_GPIO45	72 C_DDS_D11/5.8B
70.PG6_GPIO46	70 C_DDS_D13/5.8B
52.PG7_GPIO47_BOOT1	52 BOOT1/EPI0S31/4.1B
41.PH0_GPIO48	41 EPI0S6/4.1D
42.PH1_GPIO49	42 EPI0S7/4.1D
36.PH2_GPIO50	36 EPI0S1/4.1D
35.PH3_GPIO51	35 EPI0S0/4.1D
46.PH4_GPIO52	46 EPI0S10/4.1D
47.PH5_GPIO53	47 EPI0S11/4.1D
79.PH6_GPIO54	79 C_DDS_SYNC_CLK/5.7B
80.PH7_GPIO55	80 C_DDS_D0/5.7B
63.PJ0_GPIO56	63 EPI0S16/4.1C
62.PJ1_GPIO57	62 EPI0S17/4.1D
61.PJ2_GPIO58	61 EPI0S18/4.2D
60.PJ3_GPIO59	60 C_DDS_D15/5.8B
57.PJ4_GPIO60	57 C_DDS_D16/5.8B
56.PJ5_GPIO61	56 C_DDS_D17/5.8B
53.PJ6_GPIO62	53 DDS_CCI_OVERFLOW/5.4C
97.PJ7_GPIO63	97 C_DDS_D1/5.7B
140.GPIO128	140 DDS_PWR_DOWN/5.1D
110.GPIO134	110 C_DDS_PDCLK/5.7B
141.GPIO129/COMP1OUT	141 DDS_MASTER_RESET/5.1C
143.GPIO131/COMP2OUT	143 CHSEL0/4.6A
112.GPIO132/COMP3OUT	112 C_DDS_D7/5.7B
111.GPIO133/COMP4OUT	111 C_DDS_D6/5.7B
109.GPIO135/COMP5OUT	109 C_DDS_TXENABLE/5.7B
142.GPIO130/COMP6OUT	142 CHSEL1/4.6A

MASTER CLK

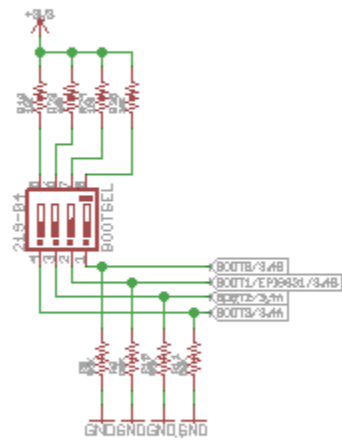
Assuming CLK input to board is 3.3V level.

The clock buffer provides 3 buffered outputs of the input clock.

JP1 can be used to switch between external input (X1) and onboard pscillator(OSC1).



BOOT SELECT



For nominal use, BOOTSEL is set to 0b0111. This boots from Flash.

BOOT0 and BOOT2 are also available and controllable through the MAINBOARD header. For example, setting BOOT0 and BOOT2 to 0 takes the MCU boot from serial peripherals.

Each of the BOOT pins can be used as GPIO post-boot. BOOT1 is already used for the EP10 interface for SDRAM. To enable this, both the on and off states of each of the DIP positions have pull-ups / pull-downs.

BOOTSEL	BOOT0	BOOT2	FUNCTION
0b0111	1	1	boot from Flash
0b0111	1	1	boot from Flash
0b0111	0	0	boot from Header (serial IO)

UART -> USB

