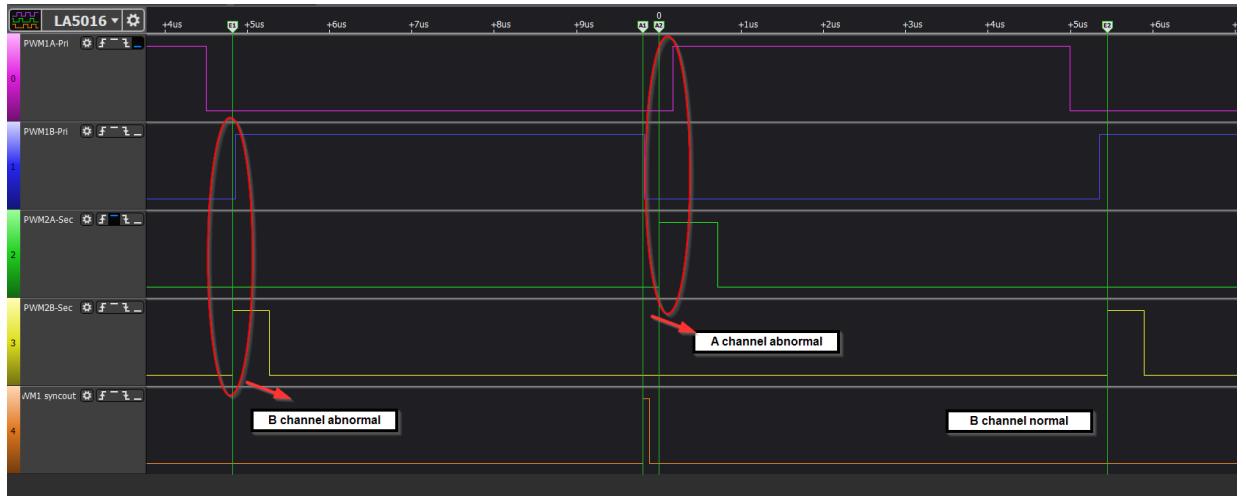


1. Channel B issue always happen before channel A

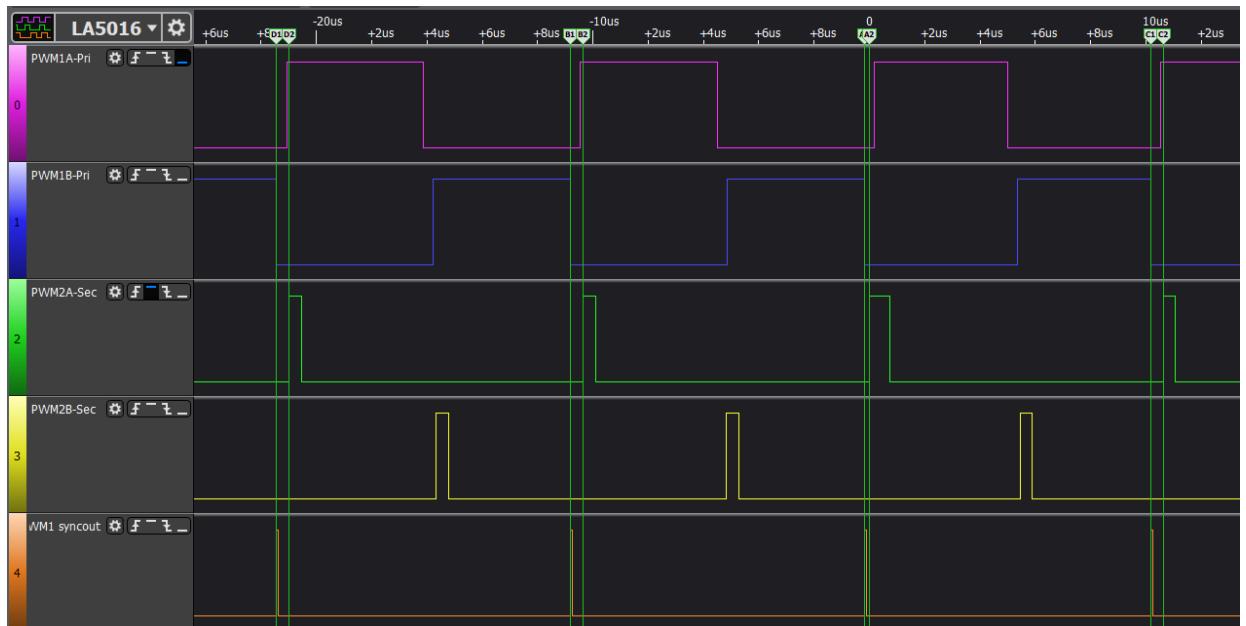


2. The abnormal sec wave dead band seems different. I compare the rising edge and falling edge with PWM syncout single.

```
// === Action Qualifier SubModule - PH1, SEC === //
//
// EPWMA high on CTR = 0
// EPWMA low on CTR = CMPA, in up count
// EPWMA low on CTR = PRD
```

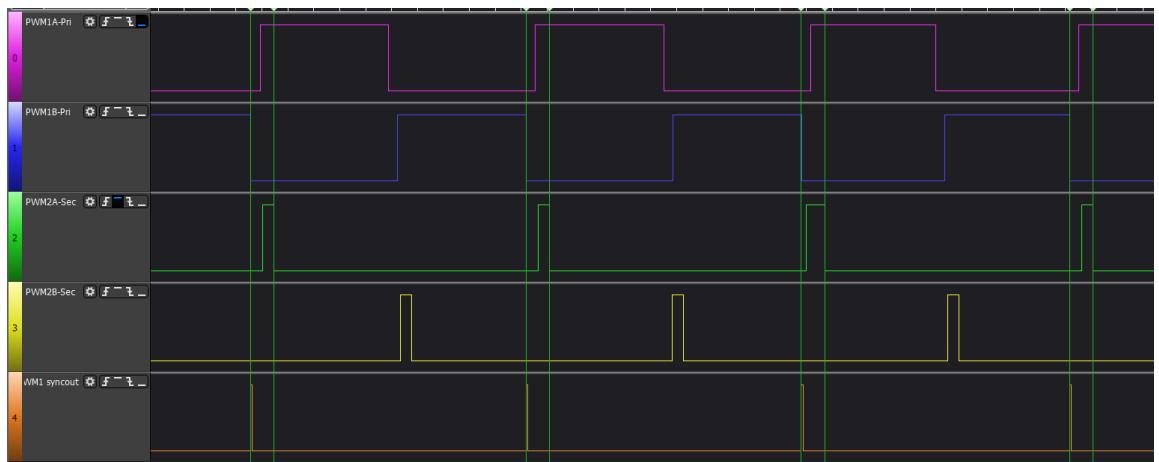
So the rising edge depends on the deadband, it seems abnormal one is too short.

In my view, This can also match with why make a delay of the PWM count can solve the issue. It is just choose not update the 'too short' deadband.



Pulse Measurements	
Timing Marker Pairs	
▼ A1 - A2 = 190ns	▼ x
A1 @ -190ns	
A2 @ 0ps	
▼ B1 - B2 = 465ns	▼ x
B1 @ -10.815us	
B2 @ -10.35us	
▼ C1 - C2 = 465ns	▼ x
C1 @ 10.16us	
C2 @ 10.625us	
▼ D1 - D2 = 465ns	▼ x
D1 @ -21.44us	
D2 @ -20.975us	

The falling edge depends on the CMPA, it is the same for abnormal and normal, so it is OK.



Timing Marker Pairs	
▼ A1 - A2 = 910ns	▼ x
A1 @ -190ns	
A2 @ 720ns	
▼ B1 - B2 = 910ns	▼ x
B1 @ -10.815us	
B2 @ -9.905us	
▼ C1 - C2 = 910ns	▼ x
C1 @ 10.16us	
C2 @ 11.07us	
▼ D1 - D2 = 910ns	▼ x
D1 @ -21.44us	
D2 @ -20.53us	

3. The control ISR is based for PWM3 ISR and frequency is 50K Hz? Am I right?

```
#define LLC_CONTROL_ISR_TRIGGER           INT_EPWM3
#define LLC_CONTROL_ISR_TRIGGER_ACK_GROUP  INTERRUPT_ACK_GROUP3
```

```
#define LLC_CONTROL_ISR_PERIOD_TICKS (uint32_t)(PWMSYSCLK_FREQ / LLC_CONTROL_ISR_FREQ)
```

Then my question is, why the Deadband and CMPA is same for 1st, 2nd and 4th time in my waveform, and different for 3rd one?

And I also checked the TRM, and I found this.

When DBRED/DBFED active is loaded with a new shadow value while DB counters are counting, the new DBRED/DBFED value only affects the NEXT PWMx edge and not the current edge.

Note

When DBRED/DBFED active is loaded with a new shadow value while DB counters are counting, the new DBRED/DBFED value only affects the NEXT PWMx edge and not the current edge.

Since global reload happened on zero, and DBRED is counting at zero, so I will suspect the DBRED will always delayed 1 PWM edge. If so, it can also explain why B channel will have issue before A channel.

However, I did not find a way to verify it.

At last, I also make a debug GPIO to see the rough time of one shot reload enable.

```
GPIO_writePin(FOR_DEBUG_PIN, 1);
EPWM_setGlobalLoadOneShotLatch(LLC_PRI1_PWM_BASE);
GPIO_writePin(FOR_DEBUG_PIN, 0);
```

It will happen one shot reload is happen really near PWM counter = zero, which makes analysis more difficult.

