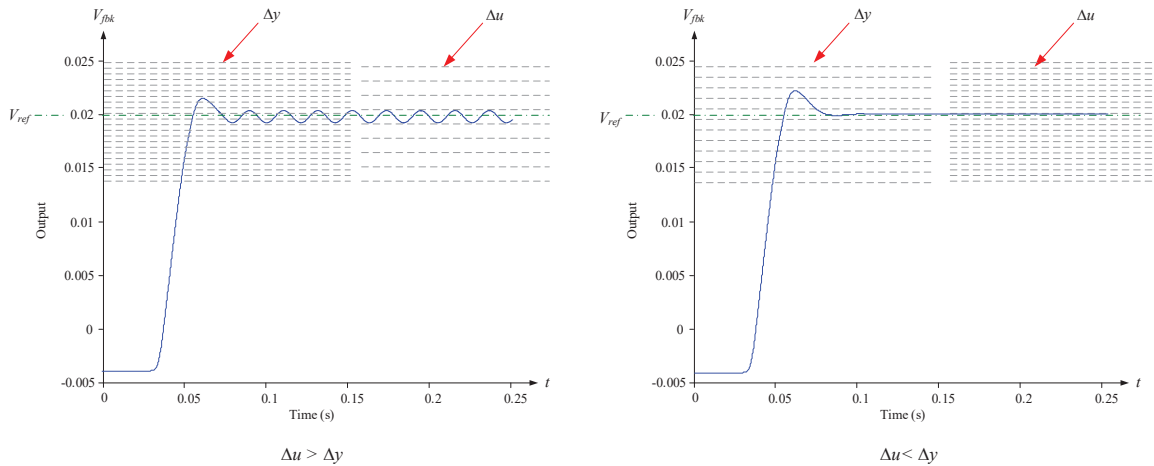


Resolution Limit Cycles

Limit cycles may appear if the sense resolution (Δy) is worse than the control resolution (Δu)



Limit cycle oscillation will be low amplitude & high frequency, and may not cause an issue in low bandwidth systems.

In general, the frequency of oscillation is not easily determined.

3. Implementation

- Sample rate selection
- **Scaling**
- Numerical considerations

- Digital PID control
- Phase compensators

The Limit Cycle Condition

To avoid a limit cycle condition we must have: $\Delta u < \Delta y$

$$\Delta y = \frac{V_{y\max}}{2^{N_2}}$$

$$\Delta u = \frac{V_{u\max}}{2^{N_1}}$$

In steady state, control and sense ranges are related by

$$V_{y\max} = |G(z)H(z)|_{z=1} V_{u\max} = K V_{u\max}$$

$$\frac{V_{u\max}}{2^{N_1}} < K \frac{V_{u\max}}{2^{N_2}}$$

$$2^{N_1} > \frac{1}{K} 2^{N_2}$$

❖ To avoid a steady-state limit cycle, control resolution must satisfy the inequality

$$N_1 > N_2 - \log_2 K$$

3. Implementation

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