Input Filter Design for Portable Power Management System

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1 Introduction

In a portable device, the input over-voltage stress is one of the most “notorious killers” of the system circuit and the ICs. The input-voltage-transient problem is related to the the power-up sequence. First plugging the wall adapter into an ac outlet and powering it up and then, plugging the wall adapter output into a portable device can cause input-voltage transients that damage the charger and dc-dc converters within the portable device.

Figure 1 shows a typical topology of battery charge system with power path selection circuit controlled by a charger IC. Two P-channel MOSFETs Q1 and Q2 in a back-to-back fashion connect the input to the system after the adapter powers up. Q3 will be on and Q1 and Q2 will be off if the adapter is unplugged and the battery pack is going to power the system directly. Figure 2 shows the typical input voltage and current spikes at adapter hot plug-in without carefully selecting the input capacitors. The input voltage spike goes as high as 32.6V that exceeds 30V, the typical absolute maximum voltage rating of a notebook charger control IC. Apparently, this may cause EOS (electrical over-stress) damage on the IC.

This application note presents how to minimize the input over-voltage stress while still keeping the cost and size reasonable.

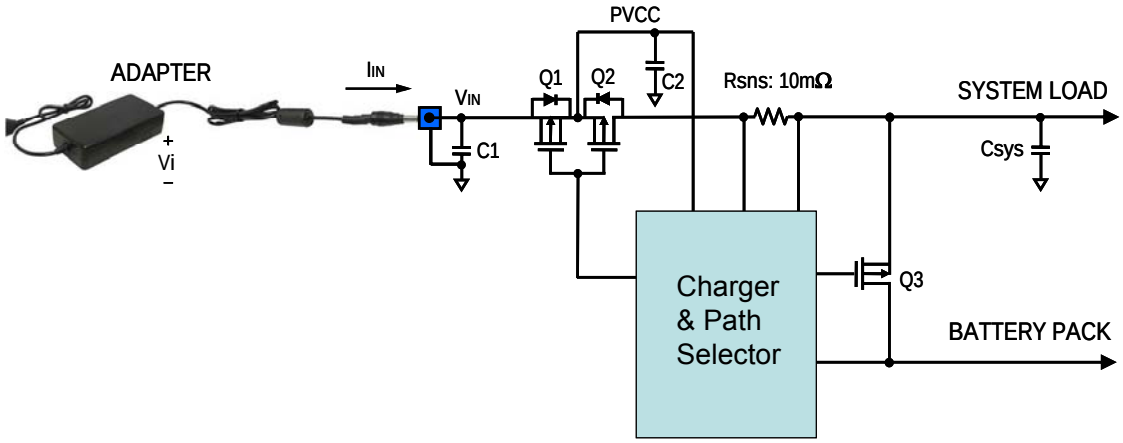


Figure 1: The typical configuration of a notebook charger and path selector

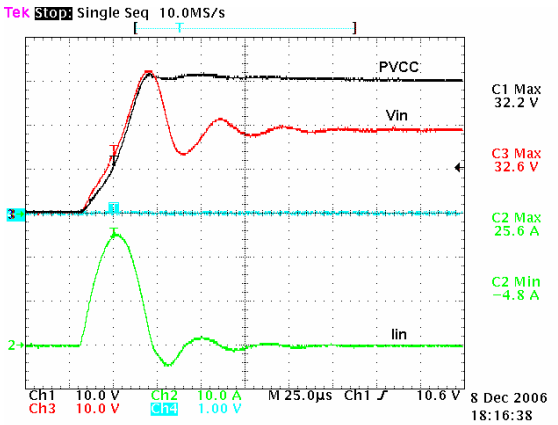


Figure 2: The input voltage and current waveforms at adapter hot plug-in.

2 Input Voltage Spike Calculation at Adapter Hot plug-in

Referring to Figure 1, the worst case of adapter insertion is the DC side insertion without battery. During the adapter plug-in, both Q1 and Q2 remain off. Only the body diode of Q1 may conduct. The equivalent circuit is shown in Figure 3. V_i is the adapter regulated voltage. R_i and L_i represent the stray resistance and inductance along the adapter cable and PCB interconnections. R_{C1} and R_{C2} represent the ESR (equivalent series resistance) of C_1 and C_2, respectively.

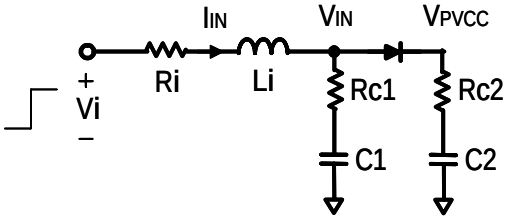
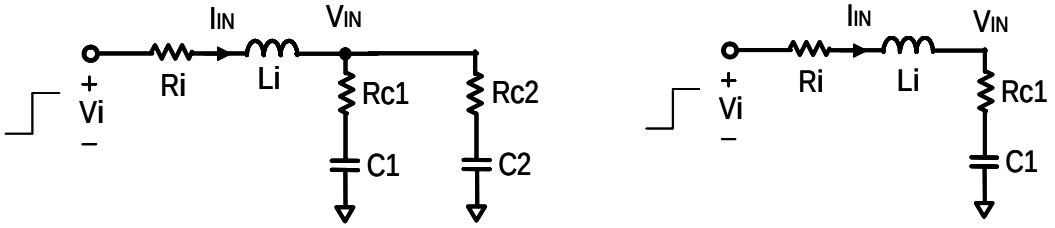


Figure 3: Equivalent circuit during adapter insertion.

When the input current I_{IN} is positive, the body diode of Q1 conducts, the equivalent circuit is shown in Figure 4(a). When the input current I_{IN} is negative, the body diode of Q1 turns off, the equivalent circuit is shown in Figure 4(b).



(a) $I_{IN}>0$ (a) $I_{IN}<0$

Figure 4: Equivalent circuit during adapter insertion

In terms of system protection, the major concern is the maximum voltage spike. As demonstrated in Figure 2, the peak voltage of the ringing in this resonant circuit is determined in the first cycle before I_{IN} drops to zero. Based on Figure 4(a), a simplified equivalent circuit, as shown in Figure 5, can be used to calculate the peak ringing voltage.

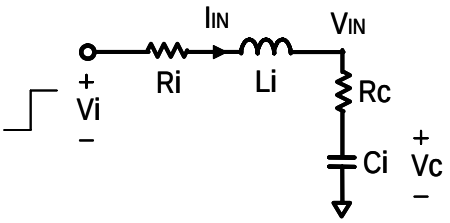


Figure 5: Simplified equivalent circuit during adapter insertion

In Figure 5,

$$R_C = \mathrm{Re}\left[\left(R_{C1} - j\frac{1}{\omega C_1}\right)//\left(R_{C2} - j\frac{1}{\omega C_2}\right)\right] \quad (1)$$

$$C_i = \frac{-1}{\omega \cdot \mathrm{Im}\left[\left(R_{C1} - j\frac{1}{\omega C_1}\right)//\left(R_{C2} - j\frac{1}{\omega C_2}\right)\right]} \quad (2)$$

It can be obtained that:

$$I_{IN}(t) = \frac{V_i}{Z_0} e^{-\frac{R_t}{2L_i}t} \sin \omega t \quad (3)$$

$$V_C(t) = V_i + \frac{V_i}{Z_0} e^{-\frac{R_t}{2L_i}t}\left(-\frac{R_t}{2}\sin \omega t - L_i \cdot \omega \cdot \cos \omega t\right) \quad (4)$$

The voltage on the input capacitor(s) is given by:

$$V_{IN}(t) = I_{IN}(t) \cdot R_C + V_C(t) = V_i + \frac{V_i}{Z_0} e^{-\frac{R_t}{2L_i}t}\left[\left(R_C - \frac{R_t}{2}\right)\sin \omega t - L_i \cdot \omega \cdot \cos \omega t\right] \quad (5)$$

in which,

$$R_t = R_i + R_C \quad (6)$$

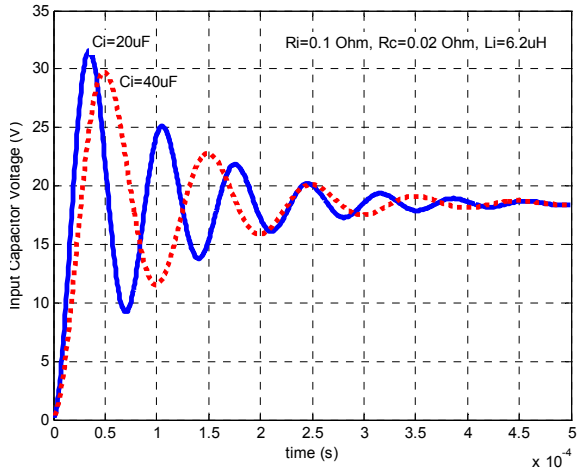
$$Z_0 = \sqrt{\frac{L_i}{C_i}} \quad (7)$$

$$\omega = \sqrt{\frac{1}{L_i C_i} - \left(\frac{R_t}{2L_i}\right)^2} \quad (8)$$

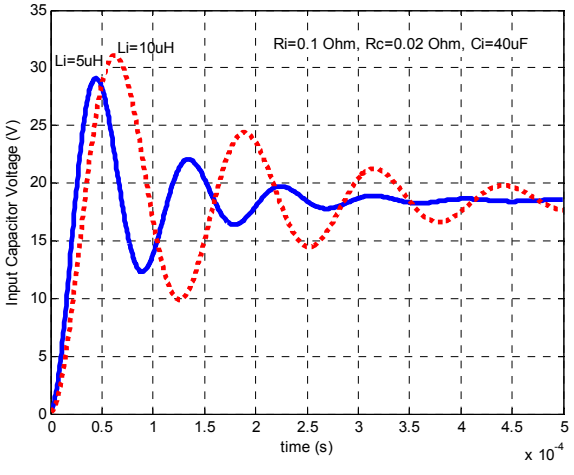
Applying a voltage step to the input capacitors through a long cable causes a large current surge that stores energy in the power-lead inductances. The transfer of this energy to the capacitor produces a voltage spike whose amplitude can be up to twice that of the original voltage step.

Figure 6 (a) demonstrates the input voltage response with various C_i. A higher C_i reduces the quality factor therefore helps damping the voltage spike. Figure 6 (b) demonstrates the effect of the input stray inductance L_i upon the input voltage spike. A higher L_i stores more parasitic energy that results in more significant ringing. Figure 6 (c) shows a higher capacitor ESR helps suppress the input voltage spike. The effect of the series input resistance R_i is illustrated in Figure 6(d).

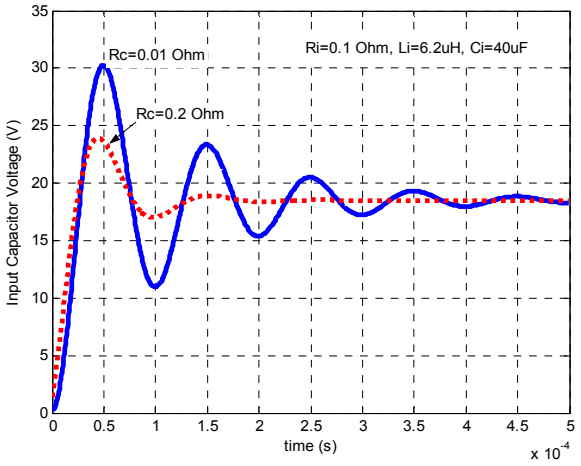
According to the parametric study in Figure 6, minimizing L_i, increasing C_i, Rc and R_i will help suppress the input voltage spike. However, the input stray inductance L_i and the resistance R_i are generally associated with the adapter cable, connectors and PCB layout, thus out of designer's control or hard to optimize. On the other hand, it is undesirable to add extra series resistance on the input power path since it will lower the efficiency. Therefore, the only two parameters for the designers to play with are C_i and R_C. This can be achieved by right capacitor selection and circuit design.



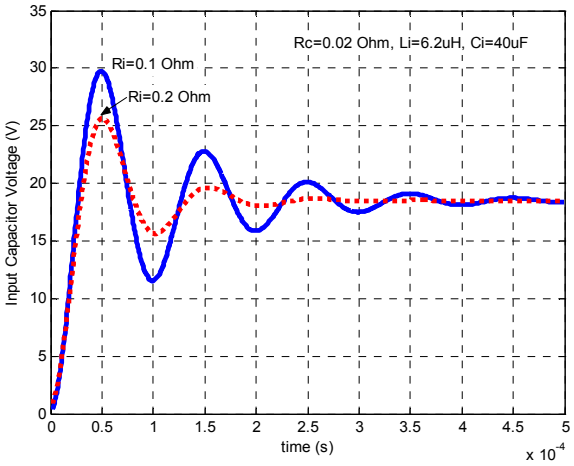
(a) V_{IN} with various C_i values



(b) V_{IN} with various L_i values



(c) V_{IN} with various R_C values



(d) V_{IN} with various R_i values

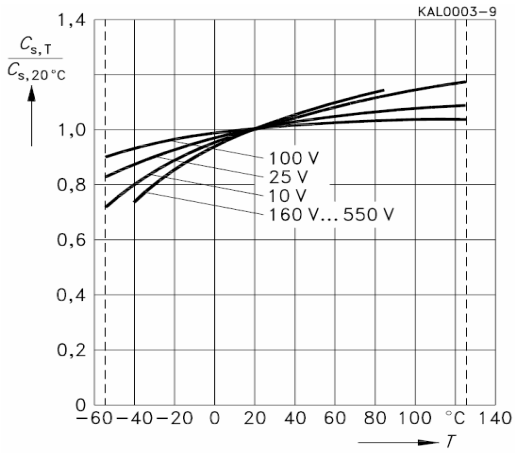
Figure 6: Parametric study of the input voltage

3 Introduction of Capacitors

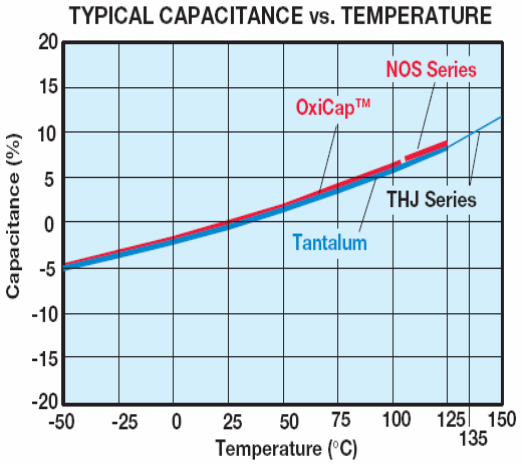
In portable electronic systems, ceramic, Tantalum and electrolytic capacitors are the most popular ones among the various capacitor candidates. Ceramic capacitors offer the advantages of small size, low ESR, high reliability and high rms-current capability. Aluminum capacitors normally have higher capacity, larger size and higher ESR. Tantalum capacitors own small size and high volumetric efficiency, and it has a higher reliability versus that of Aluminum capacitors.

3.1 Temperature dependence of capacitance

The capacitance of an electrolytic capacitor is not a constant quantity that retains its value under all operating conditions. The temperature has a considerable effect on the capacitance. With decreasing temperature, the viscosity of the electrolyte increases, thus reducing its conductivity. The resulting typical behavior is shown in Figure 7(a). The typical variation of a 25V capacitance is ±20%. The capacitance of a tantalum capacitor varies with temperature too, as shown in Figure 7(b). This variation itself is dependent to a small extent on the rated voltage and capacitor size, normally ±10%.



(a) Aluminum Electrolytic Capacitor



(b) Tantalum Capacitor

Figure 7: Temperature dependence of capacitance

The C0G and NP0 has an extremely stable capacitance with temperature, but the capacitance available is centered in the pF range. Adding a few chemical enhancers to increase the permittivity K to the 3000 range, gets the moderately stable dielectrics of X7R (±15% change over temperature range of -55°C to +125°C) and X5R types (±15% change over temperature range of -55°C to +85°C). The increased dielectric constant allows much higher capacitance per chip size, with a small sacrifice for temperature stability and some additional losses. Peaking the capacitance response at near normal room-ambient temperatures would be the Y5V and Z5U type of dielectric. The K achievable with this dielectric ranges from 6000 to above 10000 with some additional losses created. The relative capacitances of various dielectrics with temperature effects are compared in Figure 8.

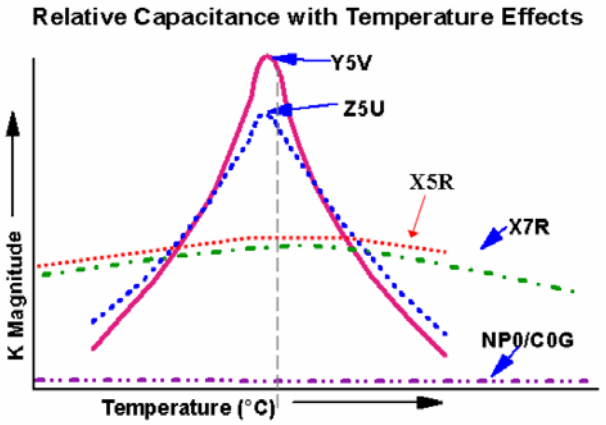


Figure 8: The relative capacitances of various dielectrics with temperature effects

3.2 ESR

ESR (equivalent series resistance) is dependent on the dissipation factor (DF) of the insulation material, as well as the resistance of the leads, plate material and plate terminations. The dielectric adds a resistance that appears to be proportional to the magnitude of the dielectric constant. The ESR value depends on frequency and capacitance by the following equation:

$$ESR = DF/(C \cdot \omega) \quad (9)$$

The dissipation factor DF is a ratio of the losses to the capacitive nature of the device. The C0G has extremely low DF, typically in the range of 0.10%. With the X7R and X5R dielectrics, the DF moves up to 2.5%, and with the Y5V, the DF moves to nearly 5%. The DF of a typical Aluminum electrolytic capacitor is a function of temperature and frequency, normally 2%-50% at room temperature wile that of a Tantalum capacitor can be up to 250%.

Figure 9 shows a comparison of ESR for ceramic, tantalum, and aluminum capacitors with a nominal value of 47µF.

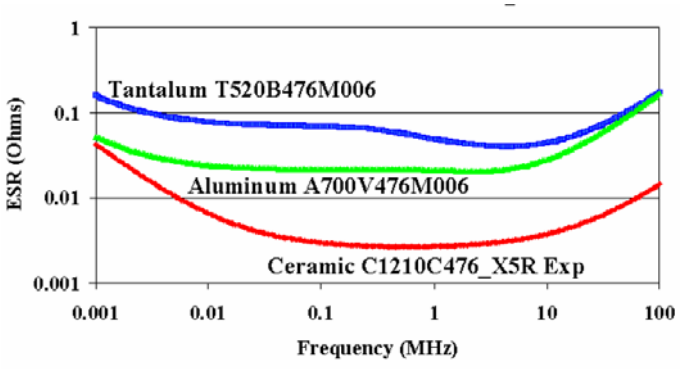


Figure 9: Comparison of the ESR of tantalum, aluminum and ceramic 47µF capacitors

Figure 10 shows a comparison of impedance for different types of capacitors with a nominal value of 10µF. The ESR of each capacitor can be roughly estimated from the minimum value of the curve.

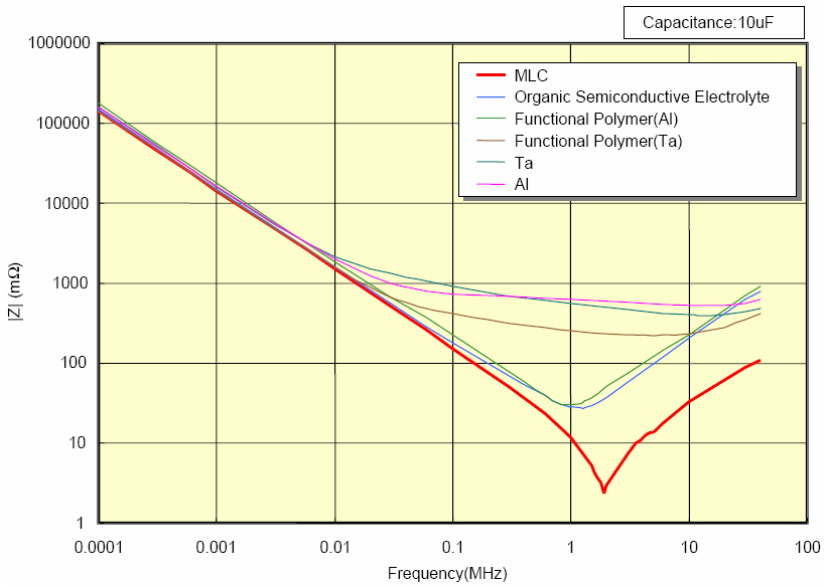


Figure 10: Impedance vs Frequency characteristics of various 10µF capacitors

4 Input Filter Design and Capacitor Selection

4.1 Criteria

An “outstanding” input filter design is based on the following criteria:

1) Safety
2) Reliability

3) Cost
4) Size
5) Performance

Safety is basically to avoid over-voltage and thermal issues. And these criteria are sometimes related with each other. For example, minimizing the input overshoot voltage makes it possible to use lower rating components, such as 25V capacitors instead of 30V or 35V capacitors, resulting in a lower cost and size.

4.2 Test conditions

Adapter: Compaq PPP012L 18.5V 4.9A
Capacitors:

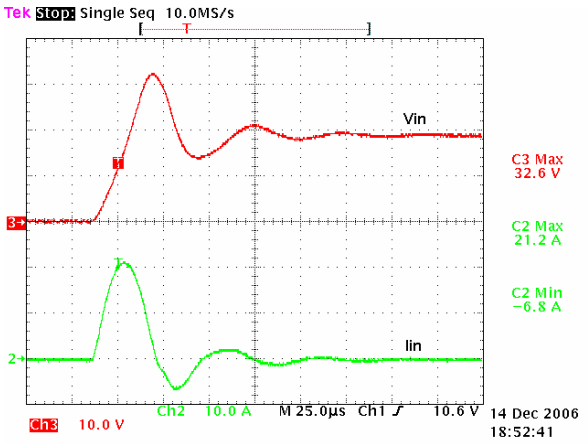
10μF(1206,X5R) ceramic capacitor: C3216X5R1E106K (TDK, 10μF, 25V, ±10%, 1206)
10μF(1812, X5S) ceramic capacitor: UMK432C106MM-T (Taiyo Yuden, 10μF, 50V, X5S, ±20%, 1812)
10μF(1210, Y5V) ceramic capacitor: ECJ-4YF1H106Z (Panasonic, 50V, Y5V, F, 20%/+80%, 1210)
4.7μF(1206, X7R) ceramic capacitor: C3216X7R1E475M (TDK, 4.7μF, 25V, X7R, ±20%, 1206)
22μF dry electrolytic capacitor: UUD1E220MCR1GS (Nichicon, 22μF, 25V, ±20%)
22μF Tantalum capacitor: TAJD226M025R (AVX, 22μF, 25V, ±20%)

Test Board: HPA207 (bq2475x EVM, Texas Instruments), Temperature: 22°C

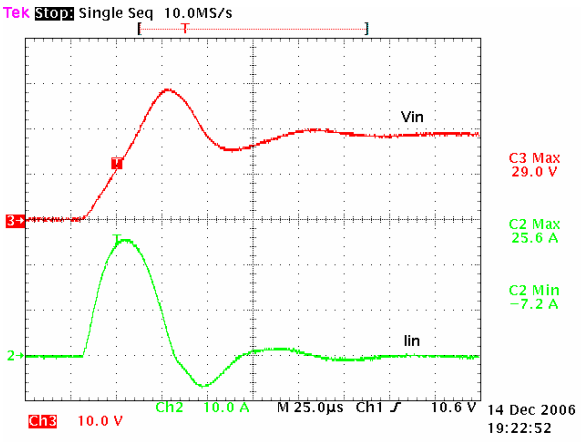
4.3 How to Reduce the Input Overshoot Voltage

In order to provide good decoupling for the IC power input, at least one low ESR, low ESL capacitor is needed to be placed very close to the PVCC pin of the IC. This decoupling capacitor(s) is normally ceramic, with its capacitance 1μF-10μF.

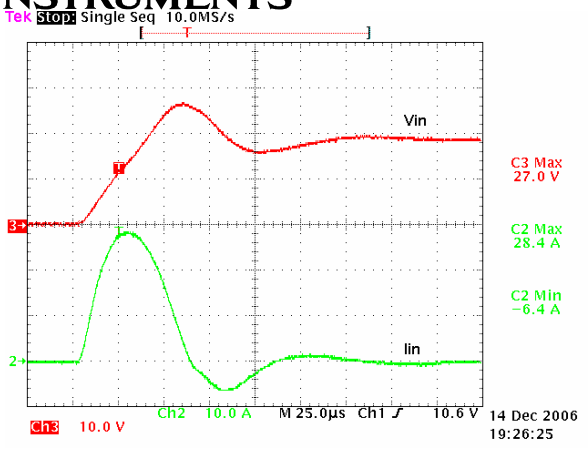
This capacitance is normally not adequate to suppress the input voltage spike. Therefore, more capacitors are needed to be put in parallel, either as C_1 or as part of C_2. However, the total ESR of n capacitors in parallel will drop to 1/n of the ESR of a single capacitor. The total damping effect will be compromised by the fact that R_i becomes n times lower. Figure 11 shows the measurement results of V_{IN} and I_{IN} with various number of 10μF (1206, X5R) ceramic capacitors in parallel. With only two in parallel, the V_{IN} peak voltage is 32.6V. It drops to 29.0V, by about 11%, with four in parallel. And it only drops by 18.4% with eight in parallel. Additionally, the peak voltage is still above 25V with even eight 10μF capacitors. Basically, this approach is not very promising both performance-wisely and cost-wisely.



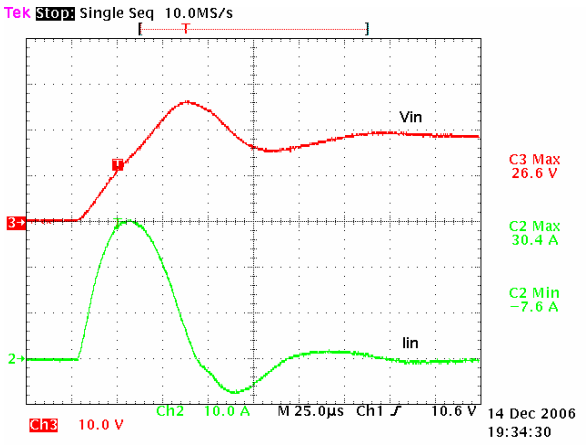
(a) C_i=2×10μF(1206,X5R)



(b) C_i=4×10uF(1206,X5R)



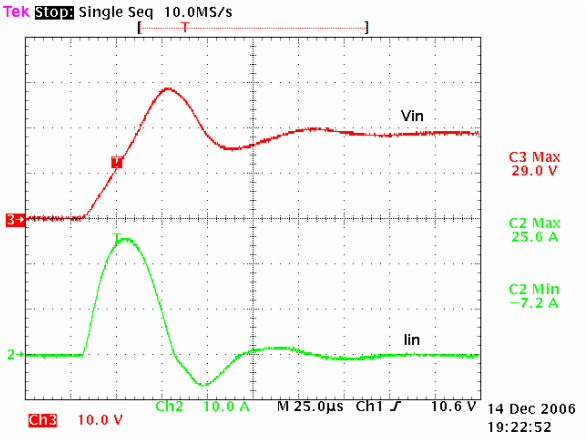
(c) C_i=6×10uF(1206,X5R)



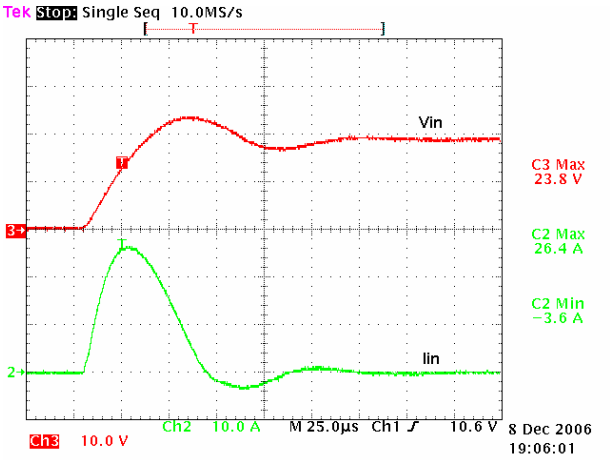
(d) C_i=8×10uF(1206,X5R)

Figure 11: Effect of applying more ceramic capacitors

Using high ESR ceramic capacitors is one of the solutions. Figure 12(b) shows the test waveform with 4×10uF(1812,X5S) high ESR ceramic capacitors. The peak voltage is much lower than that in Figure 12(a) with the same capacitance low ESR ceramic capacitors. However, 1812 ceramic capacitors are normally much more expensive than 1210 or 1206 capacitors with same capacitance.



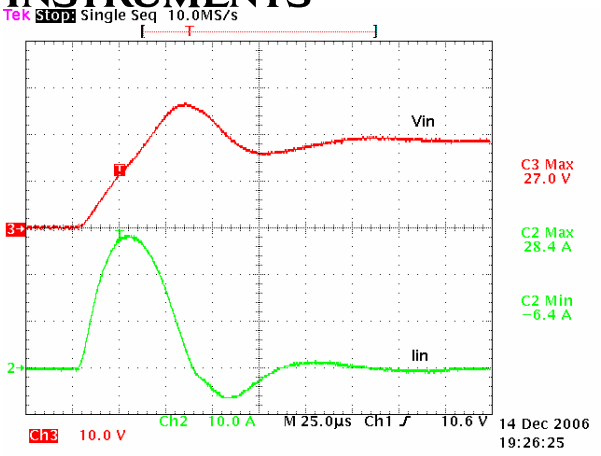
(a) C_i=4×10uF(1206,X5R), low ESR



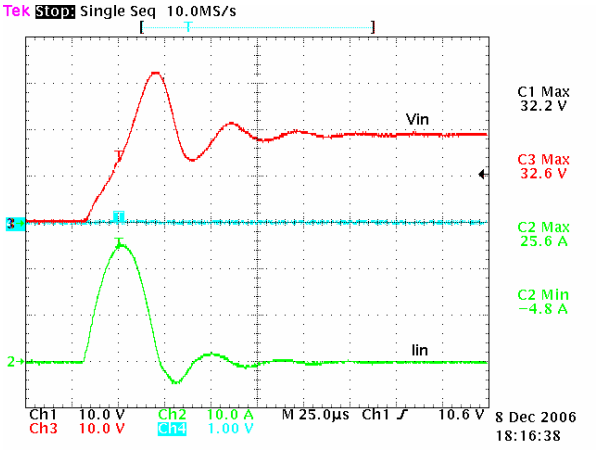
(b) C_i=4×10uF(1812,X5S), high ESR

Figure 12: Effect of ceramic capacitor ESR

Figure 13 compares the behavior of X5R capacitor and Y5V capacitor during the hot plug-in period. Due to the significant capacitance drop of Y5V material over temperature as demonstrated in Figure 8, the characteristic impedance of the resonant circuit increases and induces a higher voltage spike. Therefore, Y5V capacitors are not recommended in the input filter application.



(a) C_i=6×10uF(1206,X5R)



(b) C_i=6x10µF(1210, Y5V)

Figure 13: Effect of different ceramic dielectric materials

Another approach is to apply high ESR capacitors C_1 in parallel with the low ESR C_2. Figure 14 compares the total effective ESR of three cases:

1) $C_1+C_2=n\times10\mu F$ capacitors with the same 10mΩ ESR in parallel;

2) C_1= 20µF (ESR=100 mΩ) capacitor in parallel with $C_2=(n-2)\times10\mu F$ (ESR=10mΩ) capacitors (The total capacitance remains the same as that of case 1);

3) C_1= 20µF (ESR=200 mΩ) capacitor in parallel with $C_2=(n-2)\times10\mu F$ (ESR=10mΩ) capacitors (The total capacitance remains the same as that of case 1);

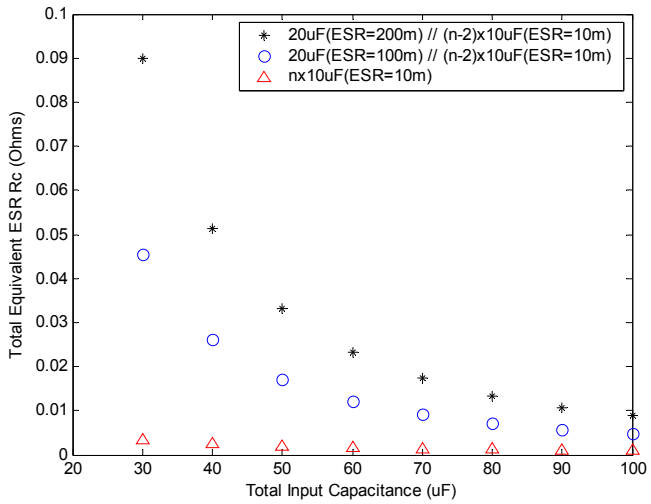


Figure 14: Total effective ESR with different capacitors in parallel

According to Figure 14, to achieve the same capacitance and a higher total ESR, one should apply a high ESR capacitor as C_1 and minimize the number of low ESR capacitors (C_2). Double the ESR of C_1 may double the total effective ESR.
Assuming C_1 and C_2 have fixed ESR, Figure 15 depicts the effect of C1 and C2 capacitances on R_C. The bigger the difference between C_1 and C_2, the higher the R_C.

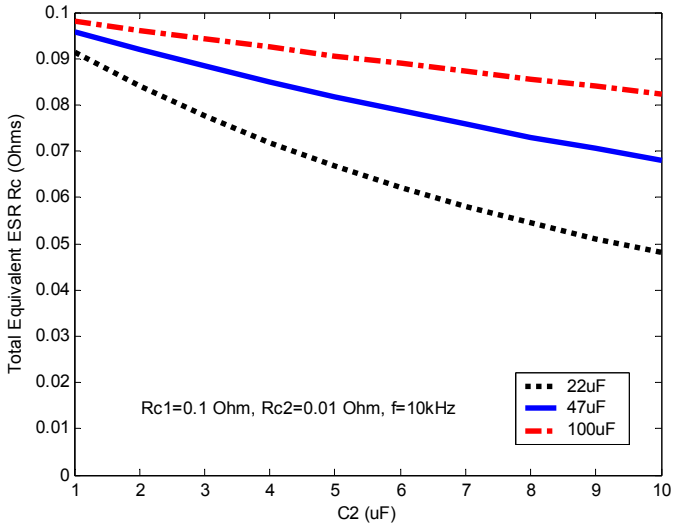


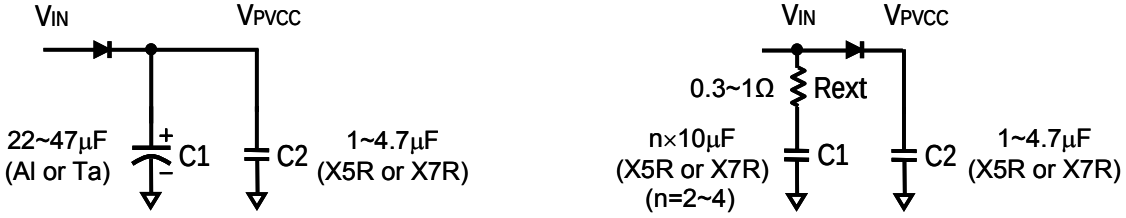
Figure 15: Total effective ESR vs C_2

4.4 Recommended Input Filter Design

Combining the conclusions above, we come up with the following input filter design tips:

- C_1: high capacitance (>20μF), high ESR (>300mΩ);
- C_2: low capacitance (1μF-4.7μF), low ESR ceramic, single capacitor

For notebook computer input filter applications, the two topologies in Figure 16 are recommended. In topology #1, high ESR capacitors such as Aluminum or Tantalum capacitors are selected as C_1 with its value from 22μF to 47μF. C_2 should be a small ceramic capacitor with the capacitance 1~4.7μF. Portable applications normally require the system to be able to stand negative input voltage. Due to the polarity of Aluminum and Tantalum capacitors, C_1 then has to be put after Q1 to avoid the reverse voltage. The major difference between topology #1 and #2 is that topology #2 applies an external resistor R_{ext} in series with some ceramic capacitors to achieve a high ESR. Depending on the design, topology #1 could be more cost-effective than #2 while the sizes are still comparable. Sometimes, ceramic capacitors are preferred in a portable electronic system due to their high reliability. In that case, topology #2 is a promising option and designer has the freedom to control the voltage spike magnitude by changing the resistance of R_{ext}.

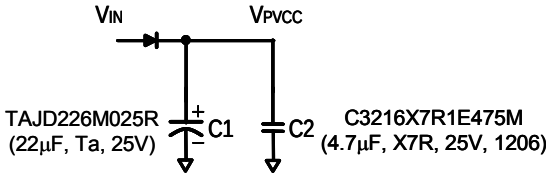


(a) Topology #1 (b) Topology #2

Figure 16: Recommended topologies and component selection

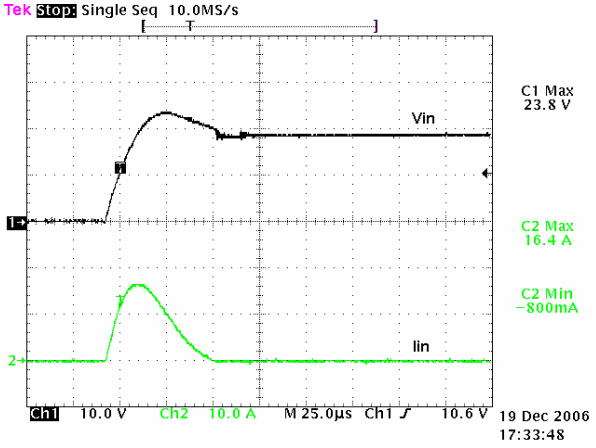
Based on these two topologies, three reference designs have been developed, as shown in Figure 17(a), (c) and (e). These reference designs have been verified with hot plug-in tests and the measurement results are shown in Figure 17(b), (d) and (f). After using Tantalum or Aluminum capacitor at the input or

adding external resistor in series with C_1, the input voltage spike has decreased dramatically. The total cost is lower than that of the 4×10μF (1812, X5S) solution while the size is smaller or comparable.

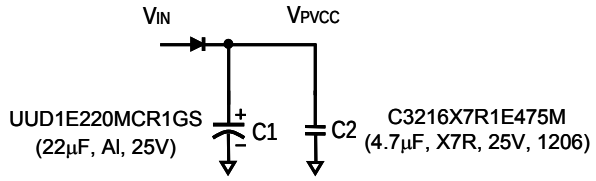


C_1: DF(max)=6%, ESR≈0.33 Ω@10kHz

(a) Design A: C_1=22uF(Tantalum), C_2=4.7uF(1206,X7R)

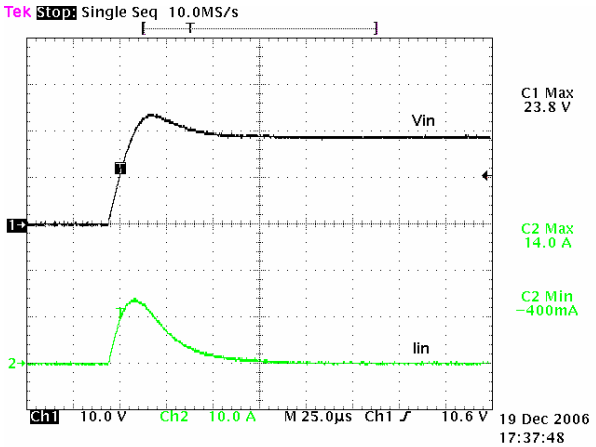


(b) Hot plug-in waveform of design A

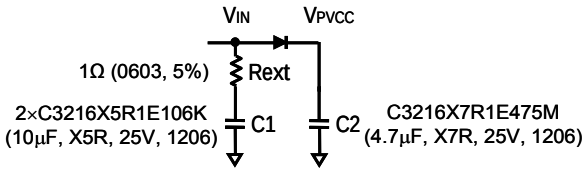


C_1: DF(max)=16%, ESR≈0.88 Ω@10kHz

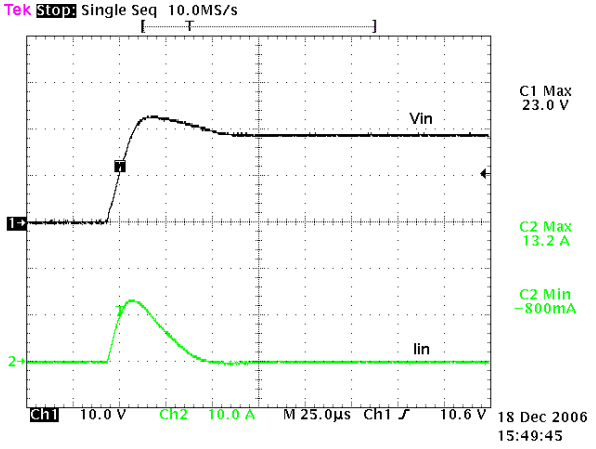
(c) Design B: C_1=22uF(Aluminum), C_2=4.7uF(1206,X7R)



(d) Hot plug-in waveform of design B



(e) Design C: C_1=2x10uF(1206,X5R), R_{ext}=1Ω, C_2=4.7uF(1206,X7R)



(f) Hot plug-in waveform of design C

Figure 17: Measurement results of three reference designs.