Buck Converter Modeling, Control, and Compensator Design
OUTLINE

• Three terminal PWM switch modeling
• Open loop transfer function
• Voltage Mode Control and Peak Current Mode Control
  • Closed loop transfer functions
  • Closed loop gain
  • Compensator Design
  • Pspice and Mathcad Simulation
  • Experimental verification
Voltage Mode Switching Regulator

Feedback Control To Achieve

• **Accuracy:** Steady-State Error
• **Speed:** Transient Response
• **Stability:** Gain and Phase Margin
Average Small Signal PWM Switch Modeling
Average Model

Nonlinear Characteristics for Switching Elements Q1 and Q2

Modeling Method:
1. Space Average Model-----Middlebrook (CIT)
2. Three Terminal Switch --- Vorperian (VPEC)
3. DC Transformer Based
PWM Switch in Basic DC-DC Converters

- A: Active Switch Node
- C: Common Node
- P: Passive switch (Diode)
Non-Linear PWM Switch

Where $D' = 1 - D$

DC Model

AC Model

Where $D' = 1 - D$
Average Model for Buck Regulator (Cont.)

\[ \bar{i}_{in} = \frac{I_p + I_v}{2} \cdot d = d \bar{i}_L \]

Transformer Characteristics

\[ \bar{i}_{in} = \bar{i}_L d \]
\[ \bar{v}_{PH} = \bar{v}_{in} d \]

Model valid only at CCM
What is Small Signal Model?

- Adding a small signal near the operating point

\[
\begin{align*}
  v_{in} & = V_{in} + \hat{v}_{in} \\
  i_{in} & = I_{in} + \hat{i}_{in} \\
  d & = D + \hat{d} \\
  i_L & = I_L + \hat{i}_L \\
  v_{PH} & = V_{PH} + \hat{v}_{PH}
\end{align*}
\]
Small Signal Average Model of three Terminal PWM Switch

\[ i_{in} = i_L d \]
\[ v_{PH} = v_{in} d \]

**Linearization**

\[ v_{in} = V_{in} + \hat{v}_{in} \]
\[ i_{in} = I_{in} + \hat{i}_{in} \]
\[ d = D + \hat{d} \]
\[ i_L = I_L + \hat{i}_L \]
\[ v_{PH} = V_{PH} + \hat{v}_{PH} \]

\[ \hat{i}_{in} = I_L \hat{d} + D \hat{i}_L \]
\[ \hat{v}_{PH} = V_{in} \hat{d} + D \hat{v}_{in} \]
Small Signal Average Model Buck Converter
Open Loop Line to Output Transfer Function (Buck)

\[ G_v = \frac{\hat{V}_o}{\hat{V}_{in}} \bigg|_{d=0} = D \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{Q\omega_0} + \frac{S^2}{\omega_0^2}} \]

\[ G_v = \frac{V_o}{V_{in}} \bigg|_{s=0} = D \]

\[ \omega_0 \approx \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_cC}, \quad \omega_{zL} = \frac{R_L}{L}, \quad Q \approx \frac{R}{\sqrt{\frac{L}{C}}} \]
Open Loop Line to Output Transfer Function (buck)

\[ G_v = \left. \frac{\hat{V}_o}{\hat{V}_{in}} \right|_{d=0} = D \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{Q \omega_o} + \frac{S^2}{\omega_o^2}} \]

\[ G_v = \left. \frac{V_o}{V_{in}} \right|_{s=0} = D \]

\[ \omega_o \approx \frac{1}{\sqrt{LC}} \quad \omega_z = \frac{1}{R_c C} \quad \omega_{zL} = \frac{R_L}{L} \quad Q \approx \frac{R}{\sqrt{\frac{L}{C}}} \]
Open Loop Control to Output Transfer Function (Buck)

\[ G_d = \left. \frac{\hat{v}_o}{\hat{d}} \right|_{\hat{v}_{\text{in}} = 0} = V_{\text{IN}} \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} \]

\[ G_d(\text{DC}) = \frac{V_o}{D} = V_{\text{IN}} \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} \]

\[ \omega_o \approx \frac{1}{\sqrt{Lc}}, \quad \omega_z = \frac{1}{R_cC}, \quad \omega_{zL} = \frac{R_L}{L}, \quad Q \approx \frac{R}{\sqrt{Lc}} \]
Control to Output Transfer Function (buck)

\[
G_d = \left. \frac{\hat{V}_o}{d\hat{v}_{in}} \right|_{\hat{v}_{in}=0} = V_{IN} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}
\]

\[
\omega_o \approx \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_cC}, \quad \omega_{zL} = \frac{R_L}{L}, \quad Q \approx \frac{R}{\sqrt{LC}}
\]
Open Loop Output Impedance

\[ Z_p = \left. \frac{\hat{V}_o}{\hat{i}_o} \right|_{\hat{d}=\hat{v}_{in}=0} \]

\[ Z_p = \frac{\hat{v}_o}{\hat{i}_o} = R_L \parallel R \cdot \frac{(1 + \frac{S}{\omega_z}) \cdot (1 + \frac{S}{\omega_z L})}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} \]

\[ Z_p(S = 0) = R_L \parallel R \]

\[ Z_p(s = \infty) = R_c \parallel R \]
Open Loop Output Impedance

\[ Z_p = \frac{\hat{V}_o}{\hat{i}_o} = R_L \parallel R \cdot \frac{(1 + \frac{S}{\omega_z}) \cdot (1 + \frac{S}{\omega_{zL}})}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} \]

\[ Z_p(S = 0) = R_L \parallel R \]

\[ Z_p(s = \infty) = R_c \parallel R \]

\[ \omega_o \approx \frac{1}{\sqrt{LC}} \], \[ \omega_z = \frac{1}{R_cC} \], \[ \omega_{zL} = \frac{R_L}{L} \], \[ Q \approx \frac{R}{\sqrt{\frac{L}{C}}} \]
Single Close Loop Controlled Switching Regulator
Small Signal Close Loop Controlled Switching Regulator

Small Signal Block Diagram

Converter
Power Stage
\[ \hat{v}, \hat{v}_o, \hat{v}_o, \ldots \]

Compensator
\[-A(S)\]

PWM
Comparador

Power Stage

\[ v_{in}, i_o, \hat{d}, \ldots \]

\[ v_{in}, i_o, \hat{d}, \ldots \]

\[ T \]

\[ -A(S) \]

\[ Fm \]

\[ Gd \]

\[ Zp \]

\[ GV \]
Open-loop Transfer Function

Open Loop Voltage Gain
(Open loop audio Susceptibility)

\[ G_v = \frac{\hat{v}_o}{\hat{v}_{in}} \text{ @ } \hat{i}_o = 0 \text{ and } \hat{d} = 0 \]

Open Loop Output Impedance

\[ Z_p = \frac{\hat{v}_o}{\hat{i}_o} \text{ @ } \hat{d} = 0 \text{ and } \hat{v} = 0 \]
Open-loop Transfer Function (Cont.)

Control to Output Transfer Function

\[ G_d = \frac{\hat{v}_o}{\hat{d}} \quad @ \quad \hat{v}_{in} = \hat{i}_o = 0 \]

Loop Compensator Gain

\[ A(s) = \frac{\hat{v}_c}{\hat{v}_o} \]

PWM Comparator Gain

\[ Fm = \frac{\hat{d}}{\hat{v}_c} \]
Small Signal PWM Comparator Gain $F_m$

$$F_m = \frac{dd}{dv_c} = \frac{\hat{d}}{\hat{v}_c} = \frac{1}{V_P}$$
Closed Loop Audio-Susceptibility (Line Trans. Response)

Audio Susceptibility

\[ \hat{V}_o = G_v \hat{V}_{in} + G_d \hat{d} \]
\[ \hat{d} = -F_m A \hat{V}_o \]
\[ \frac{\hat{V}_o}{\hat{V}_{in}} = \frac{G_v}{1 + G_d F_m A} = \frac{G_v}{1 + T} \]

Audio-Susceptibility Physical meaning: Line transient response

Loop Gain: \[ T = F_m G_d A \]

- High loop gain \( T \) will improve the line transient response
Closed Loop Output Impedance (Load Transient Response)

Closed Loop Output Impedance

\[ \hat{v}_o = Z_p \hat{i}_o - G_d F_m A \hat{v}_o \]

\[ \frac{\hat{v}_o}{\hat{i}_o} = \frac{Z_p}{1 + G_d F_m A} = \frac{Z_p}{1 + T} \]

Output Impedance Physical meaning: Load step transient response

- The smaller the output impedance, the faster the transient response
- Higher loop gain is desired
Loop Gain Analysis

Loop Gain Provides:

- **System performance analysis: Transient response**
- **Stability analysis:**
  - Absolute stability
  - Degree of stability
- **Design insight**
- **Measurement verification**
Function of Loop Gain $T$: Closed-Loop Audio Susceptibility

$$G_v = \frac{\hat{V}_o}{\hat{V}_{in}} = D \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_0} + \frac{s^2}{\omega_0^2}}$$

$$G_{CL} = \frac{\hat{V}_o}{\hat{V}_{in}} = \frac{G_v}{1 + T}$$

- The smaller $G_{CL}$, the faster line transient response
- Require higher bandwidth $f_c$
Function of Loop Gain $T$: Closed-Loop Output Impedance

\[ Z_P = \frac{\hat{v}_o}{\hat{i}_o} = R_L // R \cdot \frac{(1 + \frac{S}{\omega Z}) \cdot (1 + \frac{S}{\omega z_L})}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} \]

- ZCL used for load transient analysis
- The smaller $Z_{CL}$, the faster load transient response
- The minimum high frequency $Z_0$ is ESR
Closed-Loop Output Impedance

\[
Z_{CL} = \frac{\hat{v}_o}{\hat{i}_o} = \frac{Z_p}{1 + T}
\]

- When \( f \uparrow \)
  - C shorts and L open
  - Minimum \( Z_0 \): ESR
  - Smaller ESR, better load transient
  - Higher T, better load transient

\( \omega_{zL} = \frac{R_L}{L} \)
Ideal Loop Gain Characteristics

- High DC gain (Low frequency) for small DC error
- Wide bandwidth for fast transient response
- -20dB/dec slope near cross-over frequency for higher phase margin
- High attenuation at high frequency for noise reduction

Diagram:

- $|T|$ vs. frequency $f$
- $f_C$ (bandwidth)
- $f_0$
- Phase margin $\phi_m$
- Gain margin $G_m$
- $-180^\circ$
Examples of Loop Gain $T$

- **Single Order System**;

$$ T = \frac{G_m}{1 + \frac{S}{\omega_p}} $$

- Always stable
- $90^\circ$ phase margin

**$S=j\omega$**

**Definition**

*Magnitude* $= 20 \log |T|$  
*Phase* $= \text{Angle}(T)$

**$T=1/(1 + j)$ @ $S=j\omega_p$**

*Magnitude* $= -20 \log \sqrt{2}$$  
*Phase* $= -45 \degree$

**S-Plane**

- $(-1,0)$
- $Gm \ (S=0)$
Examples of Loop Gain $T$

- 2nd Order System: $T = \frac{G_m}{S + \frac{S^2}{\omega_o Q} + \frac{S^2}{\omega_o^2}}$

- Stable
- $\phi$ phase margin: may be very small
- Gain margin: infinite (theoretical)

S-Plane

$S = j\omega_o$

$|T| = 1$

$(-1,0)$

$G_m (S=0)$

$T = \frac{QG_m}{j}$
Basic Pole and Zero Characteristics

One Pole
- 45 degree at the Pole (frequency $f_p$)
- Total of 90° phase delay after $>10 f_p$
- -20 db/dec

One Zero
- 45° phase lead at the zero
- Total of 90° phase lead after $>10 f_z$
- +20db/dec

$$G(S) = \frac{1 + \frac{S}{10^3}}{1 + \frac{S}{10^5}}$$
The higher DC loop gain, the smaller the DC steady-state error

40dB DC loop gain, 1% error
Compensator Design Considerations
Objectives of Loop Gain Design

Objective:

- To shape the loop gain $T$ for achieving
  - High DC gain at low frequency
  - $>40$ degree phase margin
  - $>10$ dB gain margin
  - High bandwidth for fast transient response

$$T = G_d \cdot A(S) \cdot F_m$$
Load Transient Step Response vs Phase Margin

- The amount of ringing determines the phase margin
  - 45° phase margin is sufficient
- The crossover frequency is equal to the ringing frequency
  - Crossover frequency should be 1/5 or 1/10 of the converter switching frequency

\[
\omega_c = \frac{1}{5\omega} \quad \text{or} \quad \frac{1}{10\omega}
\]
Compensator Design Considerations (Voltage mode)

Compensator: Constant Gain

\[ T = G_d A F_m, \quad A(s) = K_c; \]
\[ T = F_m V_{IN} \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{Q\omega_0} + \frac{S^2}{\omega_0^2}} \cdot K_c \]
\[ \omega_0 \approx \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_c C}, \quad Q \approx \frac{R}{\sqrt{LC}} \]

- Low DC gain, need an integrator
- Almost 0° phase margin if \( \omega_z > 3 \omega_0 \)
- Stable if ESR zero \( \omega_z < 3 \omega_0 \)
Compensator Design Considerations (cont.)

Compensator: Integrator

\[ T = G_d A F_m, \quad A(s) = \frac{K_c}{s} \]

\[ T = F_m V_{IN} \frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{Q \omega_o} + \frac{s^2}{\omega_o^2}} \cdot \frac{K_c}{s} \]

\[ \omega_o \approx \frac{1}{\sqrt{L C}}, \quad \omega_z = \frac{1}{R_c C}, \quad Q \approx \frac{R}{\sqrt{L C}} \]

- Integrator: 90° delay; Double pole: 180° delay
- low bandwidth or unstable
- Need to introduce two zeros before cross-over frequency \( \omega_c \)

ESR Zero

Unstable

\[ -20\text{db/dec} \]

\[ -60\text{db/dec} \]

\[ -90^\circ \]

\[ -180^\circ \]

\[ -270^\circ \]
Type III Compensator Characteristics

\[ T_{\text{OPEN}} = G_d F_m \]
\[ T_{\text{CLOSE}} = G_d F_m A(s) \]

- Design based on OPEN LOOP GAIN
- An integrator for high DC gain
- Place two zeros around \( f_0 \) for compensating phase delay due to the integrator and double poles
- Two high frequency poles
  - to cancel ESR zero
  - to attenuate high frequency noise
  - to ensure the gain decreasing after \( f_c \)
  - to ensure the phase lag minimum at \( f_c \)
Type III Loop compensator Circuit

\[ A(S) = \frac{\hat{v}_c}{\hat{v}_o} = -\frac{Z_F}{Z_I}, \]

\[ Z_F = \frac{1}{SC_3} \parallel (R_2 + \frac{1}{SC_1}); \]

\[ Z_I = R_1 \parallel (R_3 + \frac{1}{SC_2}) \]

\[ A(S) = -\frac{K_I}{S} \frac{(1 + \frac{S}{\omega z_1}) \cdot (1 + \frac{S}{\omega z_2})}{(1 + \frac{S}{\omega p_1}) \cdot (1 + \frac{S}{\omega p_2})} \]

- **Zeros:**
  1. R2, C1;
  2. R1+R3, C2

- **Poles:**
  1. DC
  2. R2, C3 if C1>>C3
  3. R3, C2

**Compensator output**

\[ K_I = \frac{1}{R_1(C_1+C_3)}, \]
\[ \omega_{z1} = \frac{1}{R_2C_1}, \quad \omega_{z2} = \frac{1}{C_2(R_1+R_3)} \]
\[ \omega_{p1} = \frac{1}{R_3C_2}, \quad \omega_{p2} = \frac{1}{R_2\frac{C_1C_3}{C_1+C_3}} \]
Loop Gain Design (voltage mode)

\[ T = G_d AF_m \]

\[ T = F_m V_{IN} \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} \frac{K c (1 + \frac{S}{\omega_{z1}}) \cdot (1 + \frac{S}{\omega_{z2}})}{S \cdot (1 + \frac{S}{\omega_{p1}}) \cdot (1 + \frac{S}{\omega_{p2}})} \]

\[ \omega_o \approx \frac{1}{\sqrt{LC}}, \quad \omega_z = \frac{1}{R_c C}, \quad Q \approx \frac{R}{\sqrt{L/C}} \]

- Type III compensator: two zeros (\(\omega_{z1}, \omega_{z2}\)) and three poles (0, \(\omega_{p1}, \omega_{p2}\))
- Loop gain is proportional to the input voltage.

Need input voltage feed-forward function
Objective of Compensator Design

\[ T = G_d AF_m \]

\[ T = F_m V_{IN} \frac{1 + \frac{S}{\omega_z}}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} K_c (1 + \frac{S}{\omega_{z1}}) \cdot (1 + \frac{S}{\omega_{z2}}) \frac{S \cdot (1 + \frac{S}{\omega_{p1}}) \cdot (1 + \frac{S}{\omega_{p2}})}{S} \]

- Objective is to design a compensator, \( K_c, \omega_{z1}, \omega_{z2}, \omega_{p1}, \omega_{p2} \), to SHAPE the loop gain \( T \) for stability and optimum performance for given power stage parameters, \( \omega_z, \omega_o, Q, V_{IN}, \) and PWM gain \( F_m \).
Loop Gain Design Procedure (Case 1)

\[ T = F_m \]

\[ V_{IN}(1 + \frac{S}{\omega_z}) \cdot K_c(1 + \frac{S}{\omega_{z1}}) \cdot (1 + \frac{S}{\omega_{z2}}) \]

\[ 1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2} \cdot S \cdot (1 + \frac{S}{\omega_{p1}}) \cdot (1 + \frac{S}{\omega_{p2}}) \]

- Bandwidth \( f_c = (1/5-1/10) f_s \)
- \( \omega_{z1}, \omega_{z2} \) near \( \omega_o \)
- \( \omega_{p1} \) cancel ESR zero \( \omega_z \)
- \( \omega_{p2} = 10 \omega_c \)
- Determine \( K_c \)
- Select compensator R's and C's
Type III Compensator Design (Case II)

- An integrator for high DC gain
- Place two zeros around $f_0$
- Two high frequency poles to cancel ESR zero and increase gain attenuation at high frequency
Type II Compensator

- One zero and two poles
- if ESR zero is close to double pole
  \( \omega_z < 3 \omega_o \)

\[
A(S) = \frac{K_I}{S} \cdot \frac{1+\frac{S}{\omega_{z1}}}{1+\frac{S}{\omega_{p1}}}
\]
Loop Gain $T$ function of Input Voltage

$$T = F_m \left[ \frac{V_{IN}(1 + \frac{S}{\omega_z})}{1 + \frac{S}{Q\omega_o} + \frac{S^2}{\omega_o^2}} \right] \frac{K_c(1 + \frac{S}{\omega_{z1}}) \cdot (1 + \frac{S}{\omega_{z2}})}{S \cdot (1 + \frac{S}{\omega_{p1}}) \cdot (1 + \frac{S}{\omega_{p2}})}$$

- $T$ is function of $V_{IN}$
- Need feed-forward function to cancel $V_{IN}$ effect

Very little phase margin
Feed-Forward:
PWM ramp is function of the input voltage

\[
\frac{d}{V_{comp}} = \frac{1}{V_P}
\]

\[
F_m = \frac{dd}{dv_{comp}} = \frac{\hat{d}}{v_{comp}} = \frac{1}{V_P}
\]

\[
V_P = K V_{IN}
\]

\[
F_m = \frac{1}{KV_{IN}}
\]
Loop Gain with Feed-Forward Function

\[ T = G_d AF_m \]

\[ T = F_m \frac{V_{IN}}{1 + \frac{S}{\omega_z} + \frac{S^2}{\omega_o}} \]

\[ F_m = \frac{1}{KV_{IN}} \]

\[ T = \frac{1}{KV_{IN}} \frac{V_{IN}}{1 + \frac{S}{\omega_z} + \frac{S^2}{\omega_o}} \]

\[ K_c \left(1 + \frac{S}{\omega_{z1}}\right) \cdot \left(1 + \frac{S}{\omega_{z2}}\right) \]

\[ S \cdot \left(1 + \frac{S}{\omega_{p1}}\right) \cdot \left(1 + \frac{S}{\omega_{p2}}\right) \]

- Loop Gain is INDEPENDENT of input voltage.
- Fast line step transient response, Only depends on conversion speed of Vramp= f(VIN)
How to Measure the Loop Gain

\[ D = \frac{T_{on}}{T_s} \]

- Network Analyzer
- AP200
- \(a\) and \(b\): 20-50mV perturbation; \(c\): depends on output voltage
Modeling, Simulation and Test Example

TPS40200

- Voltage mode PWM controller
- Input Voltage range: 4.5V to 50V
- Input Voltage Feed Forward function
  \[ \text{PWM ramp voltage} = \frac{\text{VIN}}{10} \]
- Programmable switching frequency
- Vout: 0.7V to 90% of VIN

\[ \text{VIN}=20V, \text{VOUT}=5V, \text{fs} = 300kHz, L=47uH, C_o=22uF/10m\Omega \]
Buck Converter with Voltage Mode and Type III Compensator

\[ D = \frac{T_{on}}{T_s} \]

\[ V_{IN} \]

Gate driver

PWM Comparator

\[ V_{C} \]

\[ V_{REF} 0.7V \]

\[ R_{ESR} 5m\Omega \]

\[ L: 47\mu H, 0.25\Omega \]

\[ C_0 22\mu F \]

\[ R \]

\[ C_3: 10p \]

\[ R_2: 23.2k \]

\[ C_1: 1.5n \]

\[ R_1 30.9k \]

\[ R_3 1.15k \]

\[ C_2 1n \]

\[ R_{x} 4.99k \]
PWM small signal average model

Type III Compensator

Loop gain test perturbation

PWM gain
Simulation and Test Results

PSPICE Simulation Results

Test Results

Load Step Transient: 0.4A to 0.8A
Simulation and Test Results

PSPICE Simulation Results

Test Results

Load Step Transient: 0.1A to 1.5A
Loop Bandwidth Simulation: Mathcad and Pspice

**Mathcad**

- **Bandwidth**: 35kHz
- **Phase Margin**: 65 degree

**Pspice**

- **Bandwidth**: 45kHz
- **Phase Margin**: 70 degree
Thanks!

Current Mode Loop Compensator Design will be next time