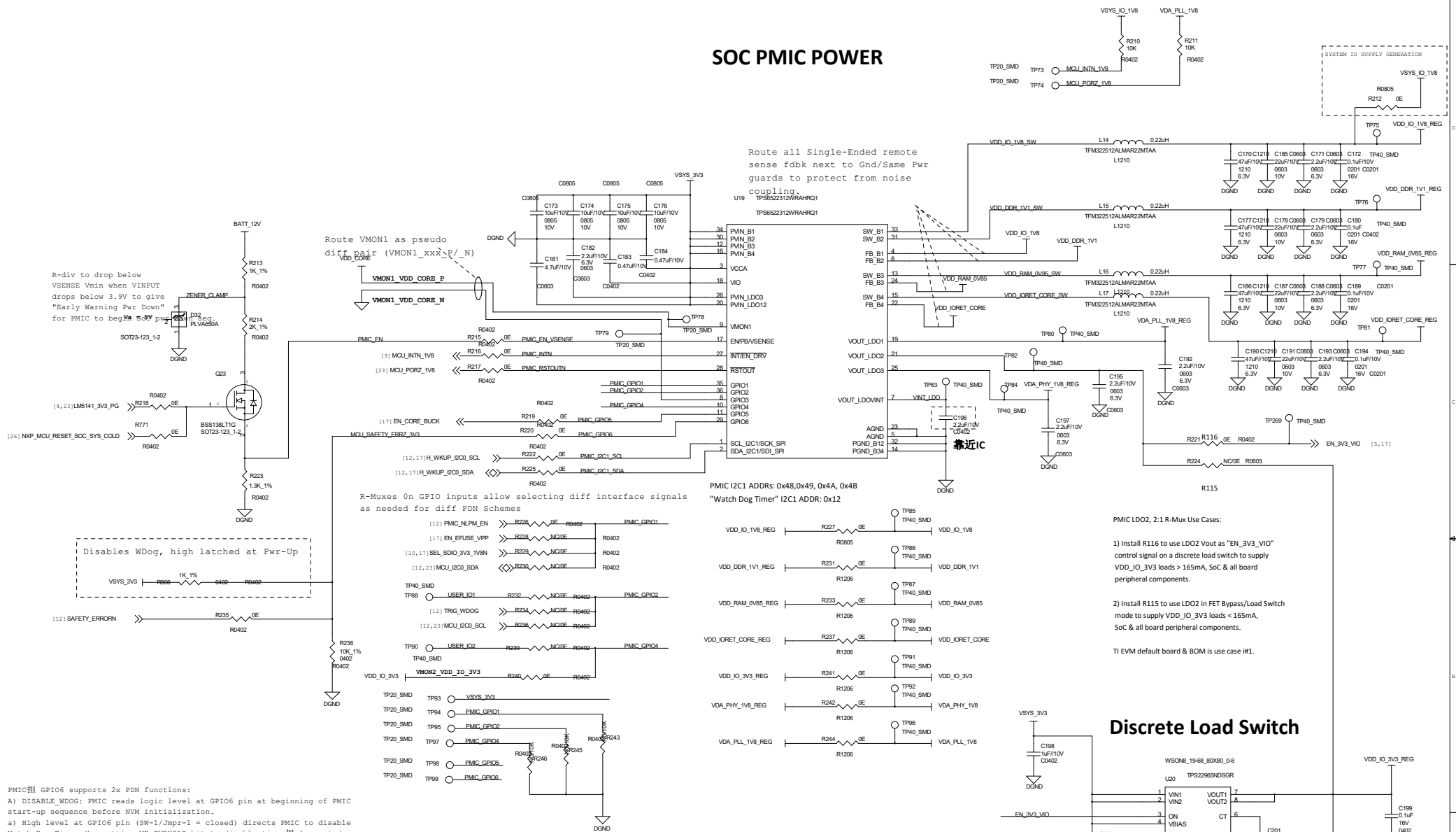


SOC PMIC POWER



PMIC GPIO_1 & GPIO_2, 2:1 R-Mux Use Cases:

- 1) Install R85 to support SoC's Partial IO Ret low power mode that needs PMIC_nLPM_EN connected to GPIO1.

- 2) Install R82 to support alternative Trigger WDog timer mode of operation.

TI EVM default board & BOM supports Use Case #1

Note:
Previous J7xxx PDNs used a 2nd, indep I2C Ch (MCU_I2C0_SCL/SDA) for WDOG operations.
Burton PMIC has limited GPIOs, so 1x I2C Ch will be timed multiplexed (PMIC control/settings & WDOG ops) in order to support low pwr modes.

SWITCH (SW2 - 5)	Description
CLOSED	Disables WDog, high latched at Pwr-Up
OPEN (Default)	Enables WDog, low latched at Pwr-Up