Application Report
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Understanding and Designing an Active Clamp Current Mode Controlled Converter Using the UCC2897A

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ABSTRACT

The UCC2897A Current Mode Active Clamp PWM Controller offers a highly integrated feature set resulting in precision control required for an active clamp forward or flyback converter. The UCC2897A data sheet contains all the design details necessary for accurately programming the device. However, there are significant design considerations and trade-offs unique to the active clamp power stage that must be defined prior to setting up the control device. Using the active clamp forward topology as an example, the clamp, power stage and control loop compensation is detailed in the following application note, which is intended to complement the information presented in the UCC2897A data sheet. This information is also applicable to the UCC2891/2/3 and 4.

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1 Introduction

The single ended forward converter is a popular choice for single and multiple output power supplies within the range of 50 W to 500 W. While there are several widely used techniques for achieving transformer reset, the active clamp approach is by far the best in terms of simplicity and optimal performance. ZVS (zero voltage switching), lower switch voltage stress, extended duty cycle range and reduced EMI (electro-magnetic interference) combined with significant efficiency improvements are just a few of the reasons to consider the active clamp reset technique.

One of the disadvantages associated with the active clamp is the need for a precise duty clamp. If not clamped to some maximum value, increased duty cycle can result in transformer saturation or additional voltage stress on the main switch which can be catastrophic. Another disadvantage has been the need for an advanced control technique to synchronize delay timing between the active clamp and main switch gate drive. One of the many features of the UCC2897A is the programmable maximum duty cycle clamp accurate to within ±3 percent. With a programmable delay time between the main switch and clamp switch, the disadvantages historically associated with controlling the active clamp are non-existent when the UCC2897A is used as the control device.

The UCC2891/2/3/4 family adds flexability by offering the capability to drive either a P-channel or N-channel clamp switch in either a high-side or low-side configuration.

For any power supply design, the success of meeting a set of given design specifications starts with a carefully designed power stage, control loop and finally setting up the PWM controller. For the active clamp forward topology there are some additional considerations that shall be discussed within the context of the following design example. While the example presented herein highlights the use of the UCC2897A PWM control IC, the design procedure for the power stage, active clamp, control loop and PWM set-up as well as the theoretical development pertaining to ZVS are applicable to the UCC2891/2/3/4 family as well.

2 Active Clamp Switching Fundamentals

Before the power stage can be designed, it is important to first understand the basic timing that is fundamentally unique to the active clamp reset. References [6] and [7] present eight distinct switching intervals, delving deeply into the active clamp current commutation. Using a low-side active clamp configuration as an example, a complete switching cycle, t0–t4, can be simplified and explained by four distinct switching intervals as detailed in Figure 1 through Figure 4.

2.1 t0–t1: Power Transfer

During this state power is transferred to the secondary as the main switch, Q_{MAIN}, is conducting and, under the right conditions, has just turned on. The primary current is flowing through the channel resistance of Q_{MAIN} and is made up of the transformer magnetizing current plus the reflected secondary current. On the secondary side, the forward synchronous rectifier, Q_F, is on and carrying the full load current. In the previous state, the load current was in the synchronous rectifier, Q_R, which is turning off as Q_F is being turned on so they are both subjected to some turn-on loss.

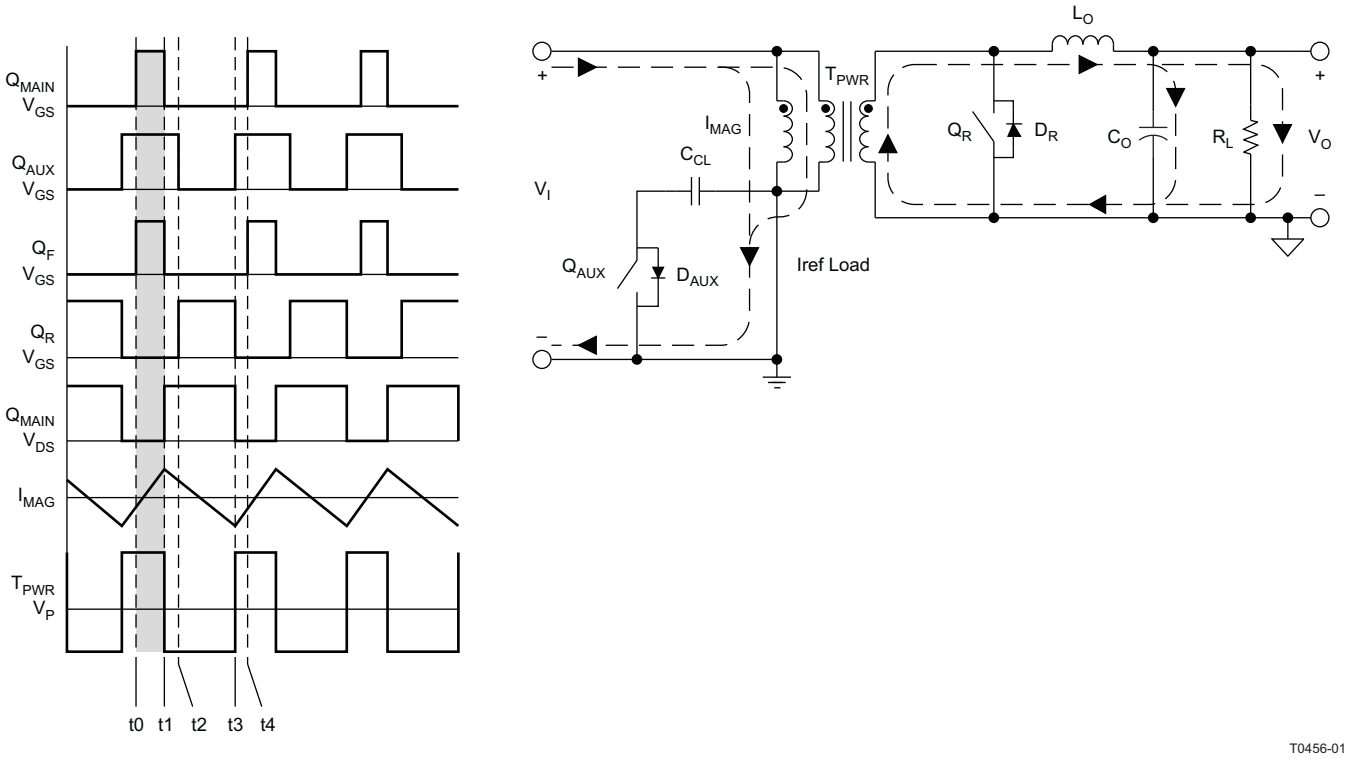

Figure 1. t0 to t1 Power Transfer Interval

2.2 t1–t2: Resonant

This is the resonant state that occurs within each switching cycle. During this state Q_{MAIN} has turned off under ZVS and the primary current remains continuous as it first charges up the drain to source capacitors of Q_{MAIN} and discharges the drain to source capacitor of Q_{AUX}. Then it is diverted through the body diode, D_{AUX}, of the clamp switch, Q_{AUX}. Because of the direction of the primary current flowing through D_{AUX}, Q_{AUX} must be a P-channel MOSFET (body-diode pointing down) for low-side active clamp applications. Since the secondary load current is freewheeling, there is no reflected primary current, so the only current flowing through D_{AUX} is the transformer magnetizing current. Therefore the body-diode conduction loss of Q_{AUX} is minimal and the conditions are set for Q_{AUX} to turn on under ZVS. The delay time between Q_{MAIN} turn-off and Q_{AUX} turn-on, also known as the resonant period, distinguishes the active clamp from other single ended transformer reset methodologies. On the secondary side, the voltage across the secondary winding has collapsed as it reflects the primary side voltage. This should result in a near zero voltage transition of the current into the body diode of QR as the winding reverses voltage polarity. The total load current will now be carried through the body diode of Q_R.

The winding voltage will continue to increase and the increase of the voltage in the new polarity will now cause Q_R to turn on.

For high current applications the body-diode conduction loss of D_R, can be a major contributor to total power loss, and is often one of the key factors limiting higher frequency operation. However, the conduction of D_R is also necessary for Q_R to turn on under ZVS. Although not possible with self-driven synchronous rectification, we would prefer to minimize the conduction time of D_R ideally to zero, but still allow Q_R to turn-on under ZVS. A detailed description of this transition is available in references [10].

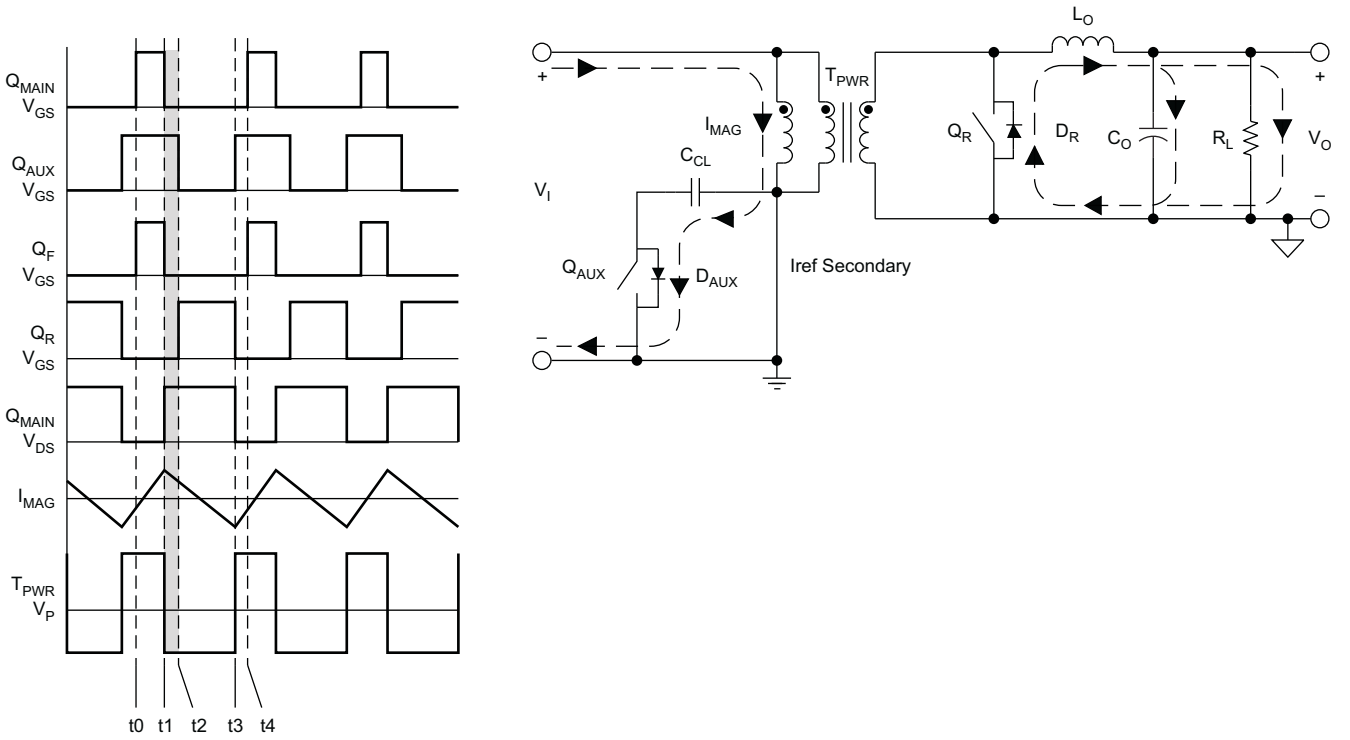

Figure 2. t1 to t2: Resonant Interval

2.3 t2–t3; Active Clamp

This is the active clamp state where the transformer primary is reset. Although the schematic of Figure 3 shows an immediate reversal of the primary current, the transition from positive to negative current flow is actually smooth and had really begun during the previous state when the magnetizing current had reached its maximum positive peak value. On the primary side, Q_{AUX} is now fully turned-on as the difference between the input voltage, V_{IN}, and the clamp capacitor voltage is now applied across the transformer primary. Q_{AUX} is subject to minimal conduction loss as only the magnetizing current is flowing through the channel resistance. Conversely, on the secondary side, Q_R is carrying the full load current through its channel resistance and is experiencing high conduction loss.

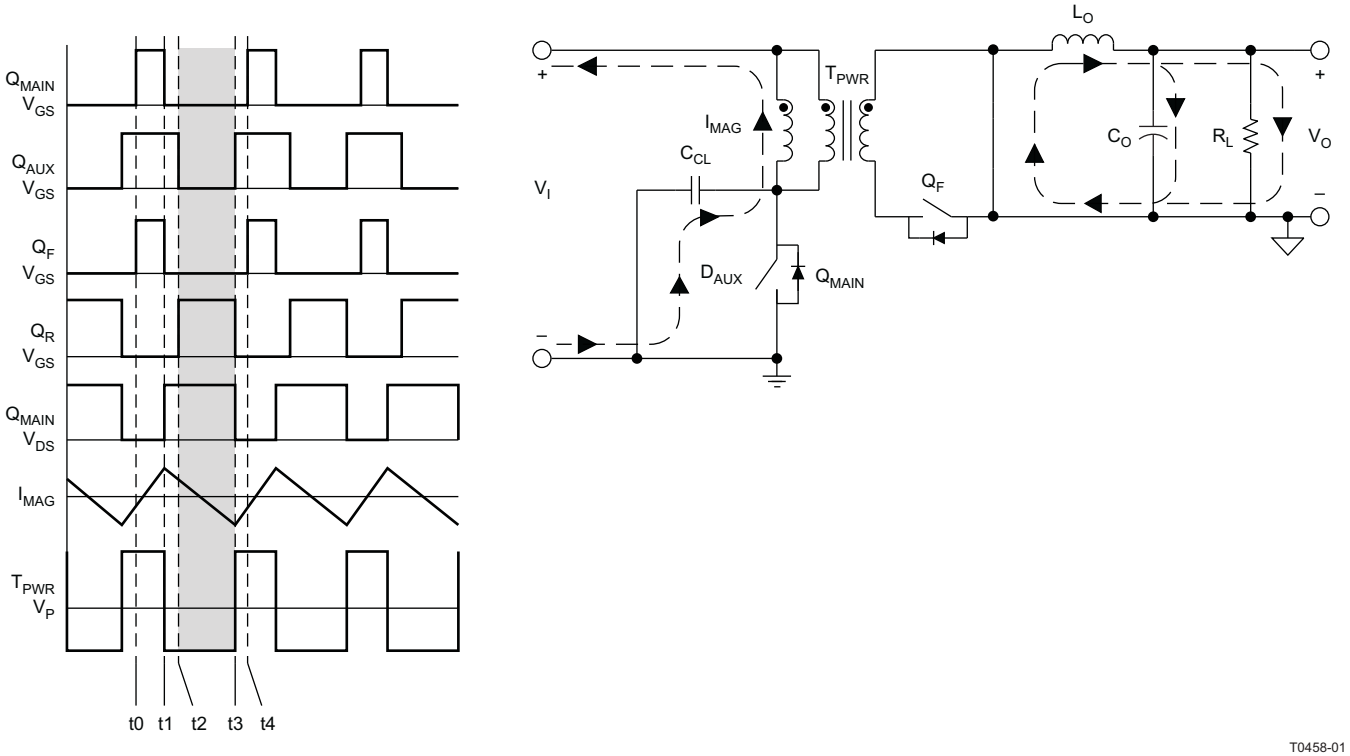

Figure 3. t2 to t3: Active Clamp Reset Interval

2.4 t3–t4: Qaux OFF to Qmain ON

This is not a resonant transition. During this state Q_{AUX} has turned off under ZVS and the magnetizing current starts to decrease the voltage on the drain to source parasitic capacitor of the Q_{AUX} and Q_{MAIN} FETs resulting in a voltage decrease on the Q_{MAIN} drain to source capacitance and a negative voltage increase on the drain to source capacitance of Q_{AUX}.

This change in voltage results in a decrease in voltage across the primary winding and the change in voltage is reflected to the secondary. Changing the secondary voltage requires current to change the drain to source capacitance of Q_F and the gate capacitances of both Q_F and Q_R. This results in the primary side magnetizing current being diverted to the secondary to alter the voltage on the gate to source capacitances of the secondary switches and slows the rate of change of voltage on Q_{MAIN}.

This means that the magnetizing current is transitioning the voltage on the primary side drain to source capacitances, the gate-to-source and gate-to-drain capacitances of Q_F and both the secondary side gate capacitances. In the EVM this would take longer than is available to achieve zero volts across the primary of the transformer. It is important to note that even if zero volts were achieved across the primary, no further voltage transition would be achieved unless the reflected magnetizing current were greater than the current through Lo. The current through Lo is being pulled out of the body diode of Q_R and unless the reflected magnetizing current exceeds this current this will continue and will hold the voltage across the secondary at zero volts.

At the point where Q_{MAIN} is turned on the voltage on the transformer will be somewhere between the peak positive voltage on the FET (approximately 2 times Vin) and Vin. However, when the FET Q_{MAIN} is turned on, the magnetizing current through the primary winding will be flowing from Q_{MAIN} into the transformer and will be small in comparison to the load current. The only current that will immediately discharge through the FET Q_{MAIN} is the capacitive charge of the Q_{MAIN} and Q_{AUX} FETs because of primary side leakage inductance.

At the completion of this sequence, the circuit is back in the t0 state.

The current through Q will rapidly build up to the reflected output current as a function of the leakage inductance and V_{IN}.

A detailed explanation of this transition is presented in reference [11].

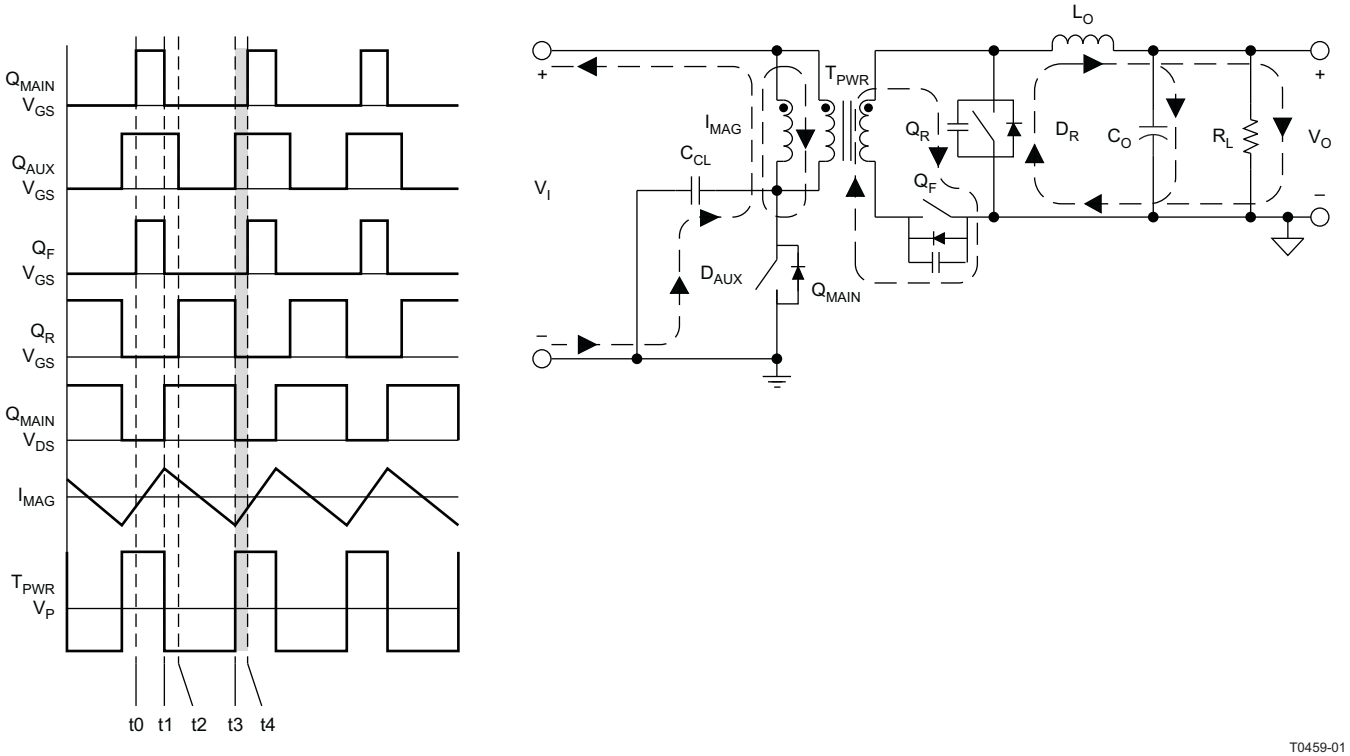

Figure 4. t3 to t4: Qaux "OFF" to Qmain "ON" Interval

3 Design Specifications

To demonstrate the benefits of the UCC2897A Active Clamp PWM controller, a 100 W forward converter capable of delivering up to 30 A at 3.3 V output is designed. The converter must operate from a telecom input voltage of 36 V<V_{IN}<72 V. Some of the key electrical design specifications are listed in Table 1. Mechanically, a target of fitting the design within an industry standard half-brick has also been imposed.

Table 1. UCC2897A Design Example Specifications

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	36	48	72	V
V_{ON}	Input turn-on voltage		35		
V_{OFF}	Input turn-off voltage		34		
η	Full load efficiency	85%	90%		
D	Duty cycle			0.6	
V_O	Output voltage	3.135		3.465	V
$\Delta V_{O(R/P)}$	Output voltage ripple		33		mVpp
I_O	Output load current	0		30	A
I_{LIM}	Output current limit			32	
F_{SW}	Switching frequency	225		275	kHz
BW	Control loop bandwidth	5		10	
ϕM	Phase margin	30		60	Degrees
T_A	Ambient temperature		25	40	°C

4 Power Stage Design

A top-level diagram of the critical components that make up the active clamp forward converter power stage is shown in Figure 5.

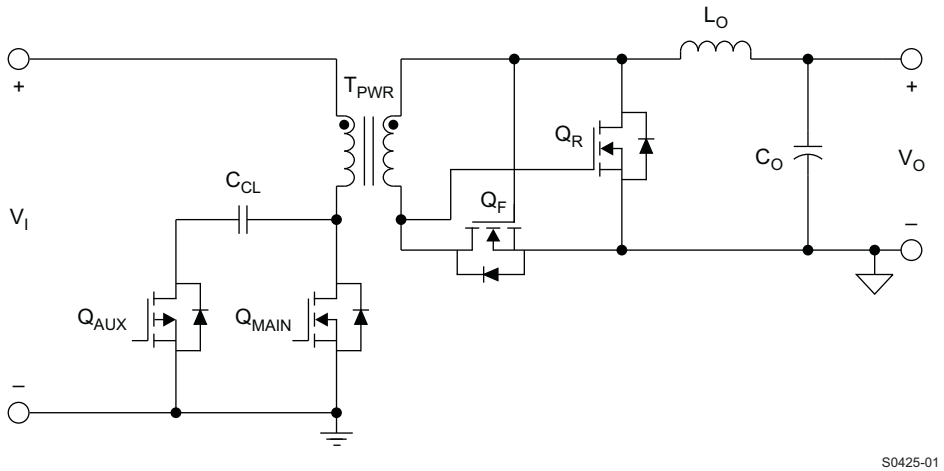

Figure 5. Active Clamp Forward Converter Power Stage

The active clamp portion of the power stage consists of the auxiliary (AUX) switch, Q_{AUX}, and the clamp capacitor, C_{CL}. Because Q_{AUX} is referenced to the primary side ground, this is referred to as a low-side clamp configuration. The details of the active clamp components are discussed in section 4.3.

For a 3.3 V output with 30 A of output current, synchronous rectification is used on the output side to maintain high efficiency especially at maximum load current. For ease of use and simplicity, self-driven synchronous rectification is chosen as shown by the forward rectifier, Q_F and the reverse rectifier, Q_R. The UC2897A has a soft turn off feature that prevents self oscillation of the secondary self driven synchronous rectifiers (reference [12]) during shutdown making this an attractive option.

The power stage design begins with selecting the secondary side output components.

4.1 Output Power Stage Design

The maximum duty cycle for a forward converter using a third winding reset scheme is normally limited to 50%. RCD clamp and resonant reset forward converters can slightly exceed 50 percent, but the active clamp reset can easily push the maximum duty cycle to 60 percent and has even been used as high as 70 percent in some lower voltage applications. For this example the maximum duty cycle, during normal operation, is limited to 60 percent at 36V input. At 72 V input the duty cycle is approximately 30 percent.

The output inductor, L_O, can be calculated by first assuming a maximum allowable inductor ripple current, ΔI_{LO}.

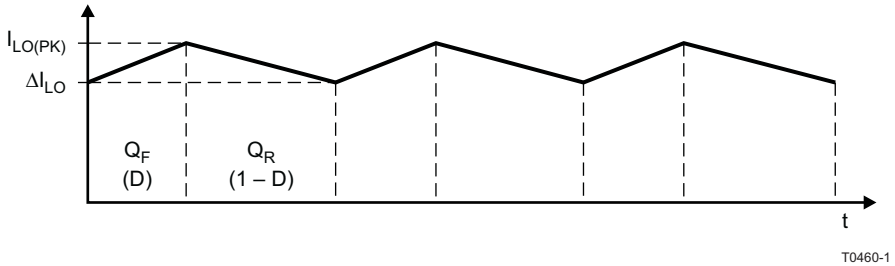

Figure 6. Output Inductor Current Waveform

4.1.1 Output Inductor

Assuming a peak-to-peak inductor ripple current equal to 15 percent of the maximum output current, Faraday's Law (1) can be applied to solve for L_O, as given by (2).

Defining the first set of variables for the equations we will be using throughout this document we have:

VO = 3.3 V	Vin_min = 36 W	Fosc_min = 225 kHz	Dmax = 0.6	ΔILo = 15%
IO = 30 A	Vin_max = 72 V	Fosc_max = 275 kHz	Dmin = 0.3	

Now using these variables, we can calculate the minimum required inductance needed as below:

$$L_O = \left(\frac{V_O}{\Delta I_{LO} \times I_O \times f_{OSC\_MIN}} \right) \times (1 - D_{MIN}) \quad (1)$$

$$L_O = 2.281\ \mu H \quad (2)$$

Rounding up results in less ripple current through the inductor, while rounding down allows more ripple current and a smaller inductor value. Bear in mind, that as ΔI_{LO} is allowed to increase, the RMS ripple current into the output capacitor increases, as does any switching loss experienced by the output rectifiers. These are the trade-offs that must be looked at when deciding on the optimal value of L_O. For this design, off the shelf (OTS) planar magnetics are used because of their low mechanical profile and repeatable design characteristics. The PA0373 from Pulse is a 2 µH planar design rated at 30 Adc, with a saturation current rating of 35 A. The PA0373 also includes a 1:4 (main to auxiliary) coupled winding that can be used for a primary referenced bootstrap bias, V_{BOOT}.

Using (3), the actual value of ΔI_{LO} (4) can be back-calculated for the chosen value of L_O equal to 2µH.

$$\Delta I_{LO} = \left(\frac{V_O}{L_O \times f_{OSC\_MIN}} \right) \times (1 - D_{MIN}) \quad (3)$$

$$\Delta I_{LO} = 5.133\ A \quad (4)$$

A current of 5.133 A_{PP} translates to 17 percent of the total load current, which is more than acceptable in terms of allowable inductor ripple current. Using (5) the maximum RMS inductor current is calculated as 30.04 A_{RMS}, which is nearly equal to the maximum load current. However, for higher values of ΔI_{LO} this calculation can serve as a design check to assure that the output inductor is not operating near saturation.

Where Ton and Toff are defined by:

$$t_{ON} = \left(\frac{1}{f_{OSC\_MIN}} \right) \times D_{MIN} \qquad t_{OFF} = \left(\frac{1}{f_{OSC\_MIN}} \right) \times (1 - D_{MIN})$$

$$I_{LO(RMS)} = \left[\left[\int_{0_{SEC}}^{t_{ON}} \left(I_O - \frac{\Delta I_{LO}}{2} + \frac{\Delta I_{LO} \times t}{t_{ON}} \right)^2 \times dt + \int_{0_{SEC}}^{t_{OFF}} \left(I_O - \frac{\Delta I_{LO}}{2} + \frac{\Delta I_{LO} \times t}{t_{OFF}} \right)^2 \times dt \right] \times f_{OSC\_MIN} \right]^{0.5}$$

$$I_{LO(RMS)} = 30.037\ A \quad (5)$$

4.1.2 Bootstrap Bias Supply

During the freewheeling period when QR is conducting, the voltage across the output inductor is simply the regulated output voltage. And since the PA0373 uses a 1:4 (NBOOT) coupled winding, an expression can be written relating V_{OUT} to V_{BOOT} assuming a Schottky diode drop of 0.5 V.

We will set the turns ratio and forward volt drop of the Schottky as below:

N1o = 4
Vfd = 0.5 V

Then solving equation (6) results in the expected voltage on V_{BOOT}.

$$V_{BOOT} = V_O \times N1_O - V_{fd} = 12.7 \text{ V} \quad (6)$$

The coupled winding technique, shown in Figure 7, works well under normal steady state conditions, however notice from (6) that the actual value of V_{BOOT} is dependant upon V_{OUT}. During abnormal operation such as over-current or short circuit current conditions, V_{OUT} is no longer in regulation causing the converter to operate in a hiccup mode as V_{BOOT} drops below the undervoltage lockout threshold of the PWM controller. If the PWM must remain fully functional during fault conditions where V_{OUT} drops out of regulation, then a separate regulated bias voltage must be derived and dedicated to maintaining V_{BOOT} above the UCC2897A undervoltage lockout threshold.

This is done in the EVM because the capacitance needed to provide enough energy storage for start up (reference [13]) was calculated (equations 7, 8 and 9) and was unacceptable large for an EVM. However, the separate regulator bus can create problems in short circuit conditions as the pulse by pulse current limiting prevents the device from hitting the shutdown overcurrent limit and going into hiccup mode and the voltage to the chip will not drop out.

Because of this, the converter is not designed to handle long term overcurrent conditions on the output.

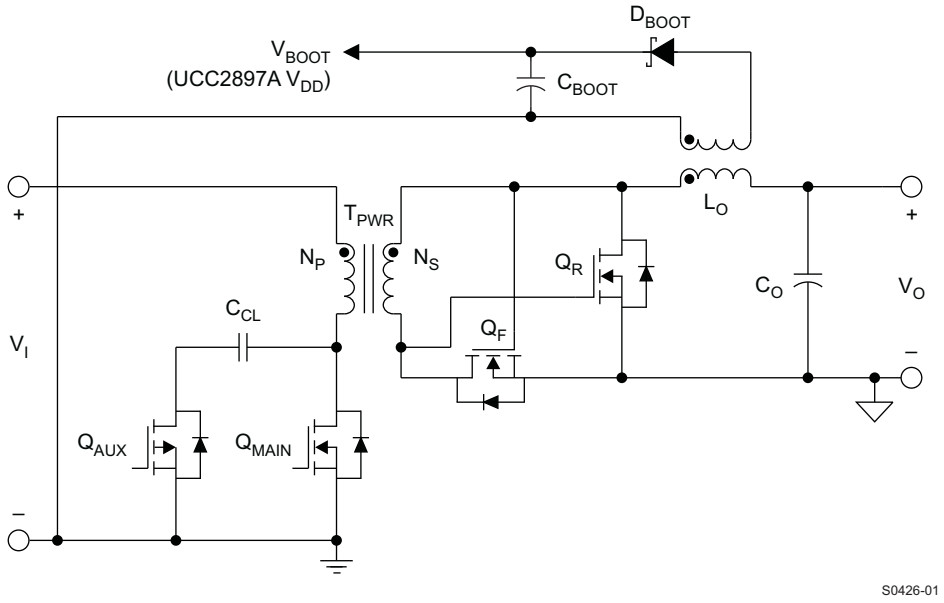

Figure 7. UCC2897A Bootstrap Bias Supply

From the UCC2897A data sheet, the minimum start-up voltage is 12.5 V, and the maximum startup current is 500 μA and a run current of 3 mA.

The UVLO will turn the device off at a minimum of 4.4 V below the start up voltage. To this current has to be added the drive current for the power transistors for the time it will take to bring the output voltage up to the designed voltage and provide power to the device through the bootstrap circuit. This is the charge needed to switch on each gate times the frequency.

The Vref capacitor charge is also supplied from this capacitor so that charge must be included

- Iic is the internal current required by the device for operation
- QgM will be defined as the gate charge of the MAIN FET.
- QgA will be defines as the gate charge on the AUX FET
- Tss is the time required to go from "ON" to having the output at nominal voltage.
- CVref is the capacitance of the reference capacitor that is charged to a maximum of 5.15 V
- Vhysterisis is the difference between the start voltage and the shutdown voltage.
- Qreqd will be the charge needed for startup.

It should be noted that the switching of the output does not happen until the soft start capacitor reaches 2.5 V and the peak will be 5.0 V, so the switching of the output devices only occurs over half the rise time and that is reflected in the equation by dividing the switching frequency in half.

$$Q_{REQD} = \left[\frac{f_{SW}}{2} \times (Q_{qM} + Q_{qA}) + I_{ic} \right] \times t_{SS} + V_{REF} \times C_{VREF} \tag{7}$$

$$C_{BOOT} = \frac{Q_{REQD}}{V_{hysterisis}} \tag{8}$$

$$C_{BOOT} = 285.568\ \mu F \tag{9}$$

These equations did not account for the variations in the Iss current. If Tss is the minimum acceptable start time then the Iss to charge the Css capacitor would be the maximum of 18.5 µA but the longest Tss would be when the Iss current is at 10.5 µA. This would result in a Tss of 1.85 the minimum and result in **the required a C_{BOOT} capacitance increasing to approximately 500 µF**.

As stated before the method chosen was a separate series regulator and because of that, the capacitance around the device that was required was only sufficient to provide the drive current to the output FETs and suppress the noise from the switching.

4.1.3 Output Capacitor

The output capacitor is chosen based upon many application specific variables such as cost, size, functionality and availability. This example determines the minimum output capacitance based upon an allowable output ripple voltage equal to 1 percent of the regulated output voltage, or roughly 33 mVpp.

For half the "ON" time of the main switch and for half the "OFF" time the current in positive (greater than the output DC and increasing to half the peak to peak value and then decreasing to zero. Therefore the charge into the capacitor is the result of a triangular shaped current with a peak of half the peak current ripple current and an approximate time of one divided by twice the frequency

Having already calculated the inductor ripple current from (4), the minimum output capacitance is calculated from (10 and 11) and is 173 µF as shown in (11).

$$\text{Charge} = \frac{0.5 \times \Delta I_{LO}}{2 \times f_{OSC\_MIN}} = 5.704\ \mu C \tag{10}$$

$$C_{OUT\_MIN} = \frac{\text{Charge}}{1\% \times V_O} = 172.84\ \mu F \tag{11}$$

The capacitance value given by (11) only affects the capacitive component of the output ripple voltage, and the final selected value is dominated by $R_{ESR(OUT)}$ and transient considerations. Limiting the output ripple voltage to 33 mVpp, the total $R_{ESR(OUT)}$ of the output capacitor needs to be less than (12) as given by (13).

$$R_{ESR} = \frac{1\% \times V_O}{\Delta I_{LO}} \tag{12}$$

$$R_{ESR} = 6.429\ m\Omega \tag{13}$$

If transient response is a design consideration, then the selection of output capacitance can be derived from examining the transient voltage overshoot, V_{OS}, that can be tolerated during a step change in output load current. By equating the inductive energy with the capacitive energy, C_O can be derived as shown below:

$$C_O = \frac{L_O \times \left(I_{STEP\_MAX}^2 - I_{STEP\_MIN}^2\right)}{\left(V_{OS\_MAX}^2 - V_{OS\_MIN}^2\right)} = 671.642\ \mu F \tag{14}$$

For a load step change from no load to 50 percent of full load and limiting the transient voltage overshoot to 3 percent of the regulated output voltage, CO is calculated to be 672 µF as shown in (14).

Two 330 µF, 6.3 V POSCAP capacitors are placed in parallel with a 10 µF ceramic capacitor as a good trade off between transient performance, small size and cost. The 6TPD330M POSCAP from Sanyo has a maximum $R_{ESR(OUT)}$ of 10 mΩ and a maximum ripple current rating of 4.4 ARMS.

From (Equation 14), notice that C_O is proportional to L_O, which is also dependant upon F_{SW} and ΔI_{LO}. As a side note, this is the reason that interleaved power stages are so popular. The ripple cancellation effect reduces ΔI_{LO} allowing much higher frequency operation which in turn reduces L_O. A smaller value of L_O results in a smaller value of C_O, which greatly reduces the L_OC_O time constant of the power stage allowing for extremely fast transient response.

Unfortunately for active clamp designs the limiting factor for response time is not the output L/C but the primary side magnetizing inductance and the clamp capacitor resonant frequency, times a factor equal to $(1–D)^2$. For this reason though we will use this capacitance, the output will have significant over and undershoot due to the low frequency response imposed by the topology.

4.1.4 Synchronous Rectifiers

There are many considerations for appropriately choosing MOSFETs used in self-driven synchronous rectifier applications. In a self-driven application the MOSFET gate-to-source voltage is ideally derived directly from the transformer secondary. As a result, the gate drive voltage is not regulated but instead varies as a function of the input voltage and transformer reset voltage, divided by the transformer turns ratio. If the input voltage range is wider than two to one, self driven synchronous rectification may not be an option and a control driven solution should instead be considered. Therefore, a good starting point is to perform a rough calculation to determine what the transformer turns ratio needs to be and then based upon the input voltage range, the variation in synchronous rectifier gate drive voltage can be calculated. By writing an equation for the volt-seconds balance across the output inductor an equation for the minimum secondary voltage, $V_{S(MIN)}$, is given by (15).

$$V_{S\_MIN} = \frac{V_O}{D_{MAX} - \left(\frac{t_{r(QMAIN)} + t_{f(QMAIN)} + t_d}{t_{SW}} \right)} \tag{15}$$

Since the value for the rise and fall time of Q_{MAIN} and the delay time (as shown in Figure 2 and Figure 4) are not yet known, a worst case value of 3 percent of the minimum total period can initially be assumed and used to solve (15).

$$V_{S\_MIN} = \frac{3.3\ V}{0.6 - \left(\frac{0.109\ \mu s}{3.64\ \mu s} \right)} = 5.789\ V \tag{16}$$

Knowing the minimum input voltage, the result of (16) can now be used to calculate the primary to secondary transformer turns ratio as given in (17).

$$N = \frac{N_P}{N_S} = \frac{V_{IN\_MIN}}{V_{S\_MIN}} = 6.219 \tag{17}$$

Rounding (17) down to the next lowest integer results in a turns ratio of 6, assuring that the minimum secondary voltage is greater than the result determined by (16). As was mentioned previously, the gate-to-source voltage of the synchronous MOSFETs is not regulated, so the next step is to determine how much the V_{GS} of each MOSFET varies for a turns ratio of 6 over the full input voltage range.

The V_{GS} of Q_F varies proportionally with the input voltage divided down by the transformer turns ratio. For 36 V<V_{IN}<72 V, the gate-to-source voltage of Q_F varies between 6 V<$V_{GS(QF)}$<12 V, which is sufficient to fully enhance even a standard MOSFET. For the reverse MOSFET, Q_R, the gate-to-source voltage is derived from the transformer reset voltage divided down by the transformer turns ratio. Unique to the active clamp topology is the fact that the reset voltage is non-linear, and this is further discussed in Section 4.3. For 36 V<V_{IN}<72 V, the gate-to-source voltage of QR varies between 8 V<VGS(QR)<5 V (except during transient conditions however the FETs chosen have a gate to source voltage of ±20 V and this would put the 150 V primary side FETs in avalanche before the gates would reach their maximums).

Selection of appropriate MOSFETs also depends upon knowing the RMS current and maximum drain-to-source voltage. From the schematic shown in Figure 5 it is apparent that the V_{GS} of Q_F is the same as the V_{DS} of Q_R, and the V_{GS} of Q_R is the same as the V_{DS} of Q_F. Therefore having already calculated what the V_{GS} is for each MOSFET, the V_{DS} is also now known.

Referring back to the inductor current waveform shown in Figure 6, the peak current seen by Q_F and Q_R can be calculated by (18).

$$I_{PKREFL} = I_O + 2\ A + \frac{\Delta I_{LO}}{2} \tag{18}$$

Q_F must be rated to withstand the peak current, as defined by (18) and the RMS current, as defined by (19), during the power transfer interval. The peak includes 2 amps overcurrent while the RMS does not.

$$t_{ON\_MAX} = \frac{D_{MAX}}{f_{OSC\_MIN}} \qquad t_{ON\_MAX} = 2.667\ \mu s$$

$$I_{QF(RMS)} = \left[\left[\int_{0_{SEC}}^{t_{ON\_MAX}} \left(I_O - \frac{\Delta I_{LO}}{2} + \frac{\Delta I_{LO} \times t}{t_{ON\_MAX}} \right)^2 \times dt \times f_{OSC\_MIN} \right]^{0.5} \right]$$

$$I_{QF(RMS)} = 23.266\ A \tag{19}$$

Conversely, the freewheeling MOSFET, Q_R, must be rated to carry the maximum RMS current, as defined by (20), during the active clamp reset interval.

$$t_{OFF\_MAX} = \frac{1 - D_{MIN}}{f_{OSC\_MIN}} \qquad t_{OFF\_MAX} = 3.111\ \mu s$$

$$I_{QR(RMS)} = \left[\left[\int_{0_{SEC}}^{t_{OFF\_MAX}} \left(I_O - \frac{\Delta I_{LO}}{2} + \frac{\Delta I_{LO} \times t}{t_{OFF\_MAX}} \right)^2 \times dt \times f_{OSC\_MIN} \right]^{0.5} \right]$$

$$I_{QR(RMS)} = 25.13\ A \tag{20}$$

The maximum RMS currents are nearly equal for each MOSFET, so the same device can be used for Q_F and Q_R. The calculated parameters for each MOSFET are summarized in Table 2, and then used to specify the necessary parameters (with 20% margin added).

Table 2. Synchronous Rectifier MOSFET Specifications

PARAMETER	Q_F	Q_R
CALCULATED PARAMETERS		
V_{GS}	6 V < V_{GS} < 12 V	8 V < V_{GS} < 5 V
V_{DS}	8 V < V_{DS} < 5 V	6 V < V_{DS} < 12 V
I_D (I_{RMS})	23.3 A	25.1 A
SPECIFIED PARAMETERS		
$V_{GS(MAX)}$	15 V	15 V
$V_{DS(MAX)}$	15 V	15 V
$I_{D(MAX)}$ (I_{RMS})	30 A	30 A
$R_{DS(ON)}$	Extremely Low	Extremely Low
Q_G	Average	Average
Number of MOSFETs(1)	2	2

(1) As determined by equations (27) and (32).

During turn-off the synchronous rectifiers of an active clamp forward converter switch at near zero voltage. During turn-on, Q_F experiences some switching loss, but Q_R turns-on under ZVS conditions. Because of the high levels of average current each device must carry, a MOSFET with extremely low on resistance should be selected. However, Q_F may still experience some switching loss, so it is desirable not to blindly select the absolute lowest $R_{DS(ON)}$ device, but still pay close attention to the gate charge characteristic.

The HAT2165 device from Renesas has an $R_{DS(ON)}$ and Q_G of 2.5 mΩ and 33 nC specified at 4.5 V V_{GS}. The absolute maximum electrical ratings for the HAT2165 are V_{DS}=30 V, V_{GS}=±20 V and I_D=55 A. The device is available in a low profile LFPAK package which is a thermally enhanced version of an industry standard SO8 package. The junction to ambient thermal impedance is approximately 60°C/W when the LFPAK is mounted on a 40 mm × 40 mm, 1 oz copper pad. Designing for an ambient environment, T_A, of 40°C, and placing a design limit on the maximum allowable junction temperature equal to 75 percent of the absolute maximum junction temperature, the maximum power dissipation that can be tolerated within a single LFPAK can be estimated by (21).

$$P_{QF(LIM)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} = \frac{(0.75 \times 150°C) - 40°C}{60°C/W} = 1.25\ W/MOSFET \quad (21)$$

A quick calculation of the total power dissipated should be done to determine how many parallel MOSFETs must be used for Q_F and Q_R, in order to maintain a maximum power dissipation of 1.25 W per MOSFET.

4.1.4.1 Q_F Power Loss Calculations

All of the following Q_F calculations are performed under the worst case operating conditions of minimum V_{IN}, maximum D and maximum I_O. For the switching loss calculation of (24), the rise time, $t_{R(QF)}$, can be approximated by (22), assuming that the sink resistance between the transformer winding and the gate of Q_F is less than 3 Ω, and at minimum V_{IN}, V_{GS} is equal to 6 V. From the manufacturer's data sheet, the gate charge, Q_G of the HAT2165H is approximately 33 nC. Since this device turns off under ZVS, the fall time is neglected.

Defining the variables

Qg = 33 nC
Rg = 3 Ω
Vgs = 6 V
Vf = 1 V
Vds_max = 5 V
TbdQF = 50 ns

We get the following results:

$$t_{r(QF)} = \frac{Q_G \times R_G}{V_{GS}} \qquad t_{r(QF)} = 16.5 \text{ ns} \tag{22}$$

$$P_{SW\_QF} = V_{DS\_MAX} \times t_{r(QF)} \times f_{OSC\_MIN} \tag{23}$$

$$P_{SW\_QF} = 509.231 \text{ mW} \tag{24}$$

And since the QF synchronous rectifier is turning off at near ZVS, there is some body-diode conduction loss at turn-off. For the purpose of loss estimation only, a worst case body-diode conduction time of 50 ns is a reasonable estimate as applied to (25).

$$t_{BD\_QF} = 50 \text{ ns}$$

$$P_{BD\_QF} = V_f \times I_{QF(RMS)} \times f_{OSC\_MIN} \times t_{BD\_QF} = 261.745 \text{ mW} \tag{25}$$

The conduction losses due to RMS current flowing through the MOSFET channel resistance are straight forward as given by (26). The worst-case channel resistance is defined in the data sheet.

$$r_{DS(on)\_QF} = 3.3 \text{ m}\Omega$$

$$P_{C\_QF} = I_{QF(RMS)}^2 \times r_{DS(on)\_QF} = 1.786 \text{ W} \tag{26}$$

There are also some small but additional losses associated with charging and discharging the MOSFET gate capacitance, but most of this loss is recovered to the output load when self-driven synchronous rectification is used. For applications using control driven synchronous rectification, these same losses are dissipated in the MOSFET driver as long as the driver impedance is much greater than the internal MOSFET impedance. For this example, gate charge losses are therefore neglected for the purpose of sizing the Q_F and Q_R MOSFETs.

The maximum power loss for a single Q_F, HAT2165H MOSFET is estimated by (27).

$$P_{QF(MAX)} = P_{C\_Q_F} \times P_{BD\_Q_F} + P_{SW\_Q_F} = 2.557 \text{ W} \tag{27}$$

Power dissipation of 2.56 W would result in a junction temperature of 193°C, for operation in a 40°C ambient exceeding the150°C limit. The number of parallel QF MOSFETs required maintaining the 112°C junction temperature design limit is given by (28).

$$Q_{F(NUMBER)} = \frac{P_{QF(MAX)}}{P_{QF(LIM)}} = 2.046 \tag{28}$$

Using 2 FETs will result in a junction temperature of 117°C at 40° on the board. This is still well below the150°C limit.

4.1.4.2 Q_R Power Loss Calculations

All of the following Q_R calculations are performed under the worst case operating conditions of maximum V_{IN}, minimum D and maximum I_O. Since the Q_R synchronous rectifier is turning on and off under ZVS conditions, switching losses are neglected. However, there is greater body-diode conduction loss than for the Q_F case. For the purpose of loss estimation only, a worst case body-diode conduction time of 150 ns is a reasonable estimate as applied to (29).

$$t_{BD\_QR} = 150 \text{ ns}$$

$$P_{BD\_QR} = V_f \times I_{QR(RMS)} \times f_{OSC\_MIN} \times t_{BD\_QR} = 848.151 \text{ mW} \quad (29)$$

The conduction losses due to RMS current flowing through the MOSFET channel resistance are straight forward as given by (30).

$$R_{DS(on)\_QR} = 3.3 \text{ m}\Omega$$

$$P_{C\_QR} = I_{QR(RMS)}^{2} \times R_{DS(on)\_QR} = 2.084 \text{ W} \quad (30)$$

The maximum power loss estimate for a single Q_R, HAT2165 LFPAK MOSFET is estimated by (31).

$$P_{QR(MAX)} = P_{C\_QR} + P_{BD\_QR} = 2.932 \text{ W} \quad (31)$$

The number of parallel Q_R MOSFETs required maintaining the 112°C junction temperature design limit is given by (32).

$$Q_{R(NUMBER)} = \frac{P_{QR(MAX)}}{P_{QF(LIM)}} = 2.346 \quad (32)$$

The junction temperature maximum should be no more than 128 degrees or 85%. Though the design says to be safe we should use more than 2 FETs, each FET will be only 14% over the worst case limit of 75% of the maximum allowable temperature and should be OK. If this were a production design root sum square analysis would be done and should show that the design is safe.

4.2 Power Transformer Considerations

For simplicity, the PA0810 OTS planar transformer from Pulse was chosen. Rated up to 140 W and measuring less than 10 mm high, the PA0810 is a good choice for module power applications requiring low-profile passive components. The PA0810 uses two primary windings of six turns each, and two single turn secondary windings. As determined from (17), a turns ratio of six must be maintained by connecting the two primary windings in parallel and the two secondary windings in parallel. This reduces the dc winding resistance by half, greatly reducing the I^2R conduction losses.

Since the PA0810 is part of a configurable family of planar transformers, its design and construction may not be optimal for all situations. Many applications might demand more than is possible from an OTS transformer solution, such as smaller size, fewer windings, increased primary to secondary isolation or higher efficiency.

At 250 kHz the transformer losses are dominated by core loss, occurring from time varying flux swing through the transformer's BH curve and conduction loss, resulting from the RMS current flowing through the planar windings. The flux swing, ΔB, is first determined from (33) containing a constant specific to the effective area of the PA0810 core geometry (Kxf) is found in the manufacturer's data sheet).

$$K_{XF} = \frac{179211.461}{10m^2}$$

$$\Delta B = \frac{K_{XF} \times V_{IN\_MIN} \times D_{MAX}}{f_{OSC} \times N_P} = 2.581 \times 10^3 \text{ gauss} \tag{33}$$

The result of (33) can now be applied to (34) (also available in the manufacturer's data sheet) to determine the core loss.

$$P_{CORE} = C_{CL} \times \left(\frac{\Delta B}{\text{gauss}}\right)^{2.5} \times \left(\frac{f_{OSC}}{\text{kHz}}\right)^{1.8} = 1.114 \text{ W} \tag{34}$$

The copper losses are a result of RMS currents flowing through the primary and secondary windings. The average current through the secondary was defined previously by (19).

From the data sheet we have Lmag on the primary as 86.25 µH. This gives us a total magnetic current change of

$$I_{MAG} = \frac{V_{IN\_MIN} \times D_{MAX}}{f_{OSC} \times L_{MAG}} = 1.002 \text{ A} \tag{35}$$

However the magnetic current change is nearly evenly balanced about zero so the peak current is only half of that value. We can determine the peak current in the primary from

$$I_{PRI\_PK} = \left(\frac{I_O + \frac{\Delta I_{LO}}{2}}{N} \right) + \frac{I_{MAG}}{2} = 5.929 \text{ A} \tag{36}$$

The Primary side RMS current consists of the sum of the currents when the QMAIN is on plus the current when QAUX is on.

$$I_{PRI(RMS)} = \left[\left[\int_{0_{SEC}}^{\frac{D_{MAX}}{f_{OSC}}} \left[\frac{I_O}{N} - \frac{\frac{\Delta I_{LO}}{N} + I_{MAG}}{2} + \left(\frac{\frac{\Delta I_{LO}}{N} + I_{MAG}}{\frac{D_{MAX}}{f_{OSC}}} \right) \times t \right]^2 \times dt + \int_{0_{SEC}}^{\frac{1-D_{MAX}}{f_{OSC}}} \left(\frac{\frac{I_{MAG}}{N} \times t}{\frac{1-D_{MAX}}{f_{OSC}}} \right)^2 \times dt \right] \times f_{OSC} \right]^{0.5}$$

$$I_{PRI(RMS)} = 3.912 \text{ A} \tag{37}$$

For thermal purposes the RMS current is derived and the value is expressed in (37).

From the manufacturer's data sheet, the DC resistances of the transformer primary and secondary (paralleled windings) are given as 11.25 mΩ and 0.875 mΩ respectively. These values can now be used along with the known transformer RMS currents to calculate the conduction losses as given by (38).

$R_{DC\_PRI} = 11.25 \text{ m}\Omega$ $R_{DC\_SEC} = 0.875 \text{ m}\Omega$

$$P_{CU} = I_{PRI(RMS)}^2 \times R_{DC\_PRI} + I_{QF(RMS)}^2 \times R_{DC\_SEC} = 0.646 \text{ W} \tag{38}$$

The maximum transformer power loss can now be calculated by (39).

$$P_T = P_{CORE} + P_{CU} = 1.76 \text{ W} \tag{39}$$

From the temperature curves given in the manufacturer's data sheet, 1.76 W of total power loss results in approximately 40°C rise above ambient temperature. Therefore the maximum anticipated temperature of the transformer is approximately 80°C, as given by (40).

$$T_{T(PWR)} = \Delta T_{T(PWR)} + T_A = 40°C + 40°C = 80°C \tag{40}$$

4.3 Active Clamp Circuit

The active clamp operates on the principle that the magnetizing energy in the transformer is balanced. This means that under stable conditions, the integral of the voltage across the primary winding over a cycle should sum to zero. When the QMAIN is on the voltage across the primary is equal to the voltage on the input, Vin. This voltage is present for the time the QMAIN is on which corresponds to the duty cycle "D". For a steady state condition this can be expressed as

$$V_{IN} \times D \tag{41}$$

When the QMAIN turns off, if the system is in balance the voltage across the primary winding is:

$$V_{PRI\_AUX\_ON} = \frac{V_{IN} \times D}{1 - D} \tag{42}$$

But there is one terminal of the primary still connected to the Vin line. This means that under steady state conditions the voltage across the clamp capacitor when the QAUX is on will be:

$$V_{CL} = V_{IN} + V_{PRI\_AUX\_ON} = V_{IN} + \frac{V_{IN} \times D}{1 - D} = \frac{V_{IN}}{1 - D} \tag{43}$$

There will be slight variations to this during a cycle as the magnetizing current first charges the Cr capacitor and then discharges the capacitor but this is the normal voltage that both the Q_{MAIN} and the Q_{AUX} will experience.

However, during transient conditions this voltage will change as the control loop responds to the need to correct the output voltage and this results in an imbalance of the magnetizing current. This imbalance results in a resonance in the circuit between the primary side magnetizing inductance and the clamp capacitor. But as these two components are only connected during the time when Q_{AUX} is on, the resonant frequency has a $(1\text{-}D)^2$ factor. As D is being changed by the control circuit, the effective resonant frequency is changing dynamically.

To determine the actual voltage the FETs under steady state conditions, we must look at the duty cycle and the associated voltages more carefully.

First define the duty cycle as a function of the input voltage knowing the turns ratio primary to secondary is 6:1.

$$D = \frac{V_O}{\frac{V_{IN}}{N}} \tag{44}$$

This yields actual duty cycles ranging from 0.275 to 0.55. These do not correspond to the defined minimum and maximum we have been working with. Since the calculated maximum is less than the defined maximum we should have no problem.

Next, we have to calculate the voltage that will appear across the primary of the transformer when Q_{MAIN} is off as a function of the input voltage and duty cycle. Then the voltage across the clamp capacitor Cr can be calculated.

The voltage across the clamp capacitor will be the sum of the input voltage Vin and the voltage across the primary when the Q_{MAIN} is off. This is also the voltage that will be across the FETs when they are off.

$$V_{PRI} = \frac{V_{IN} \times D}{1 - D} \tag{45}$$

$$V_{CR} = V_{PRI} + V_{IN} \tag{46}$$

These equations give the voltage that would be expected in normal operation and are shown in the Figure 8 as a function of the input voltage.

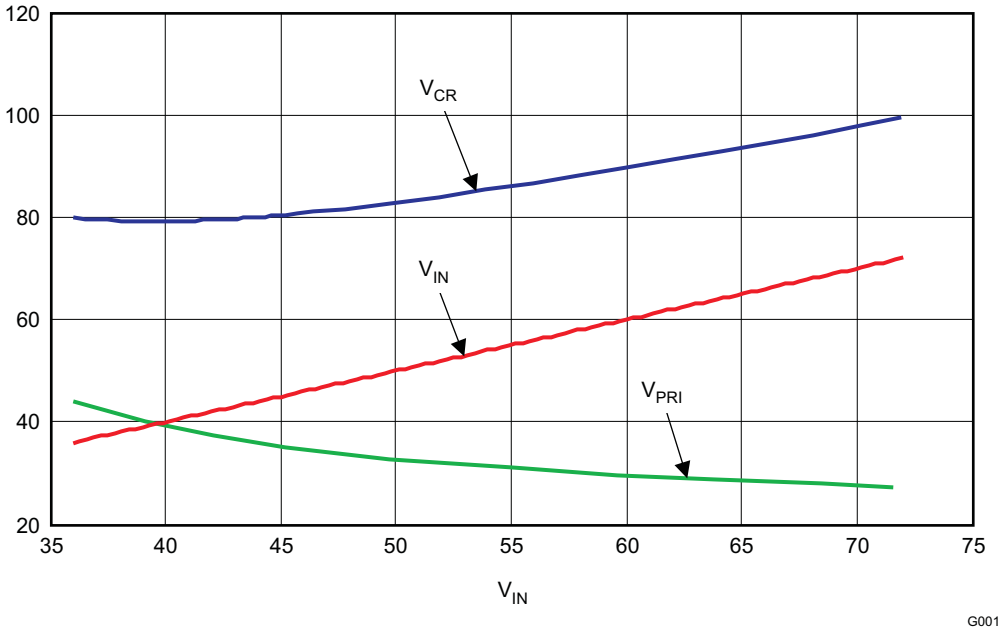

Figure 8. Reset and Clamp Capacitor as a Function of Input Voltage Under Steady State Conditions

However, during transient events the resonance between the Cr capacitor and the primary side magnetizing current will result in a transient voltage appearing across the Cr capacitor (reference [8]) and hence across the transistors. To allow for this variation it is safer to assume that the voltage across the capacitor and FETs will be significantly greater than the values defined in equation 46 and shown in the graph. Since we are using 150 volt FETs we should have enough margin on the primary side but we also have to check the secondary side. The secondary side gate voltage limits are 20 V. To impact the gate the primary side voltage across the winding would have to approach 120 volts. Even at minimum input voltage, this would put the primary side FETs into avalanche.

4.3.1 Low-Side Clamp Gate Drive

Since it has already been established that Q_{AUX} must be a ground referenced P-channel device, a negative gate drive voltage is required to fully turn this device on. However, the UCC2897A does not produce output voltage levels below ground reference. Using a gate drive circuit applied to the low-side clamp, the P-channel MOSFET can be directly driven from the UCC2897A as shown in Figure 9.

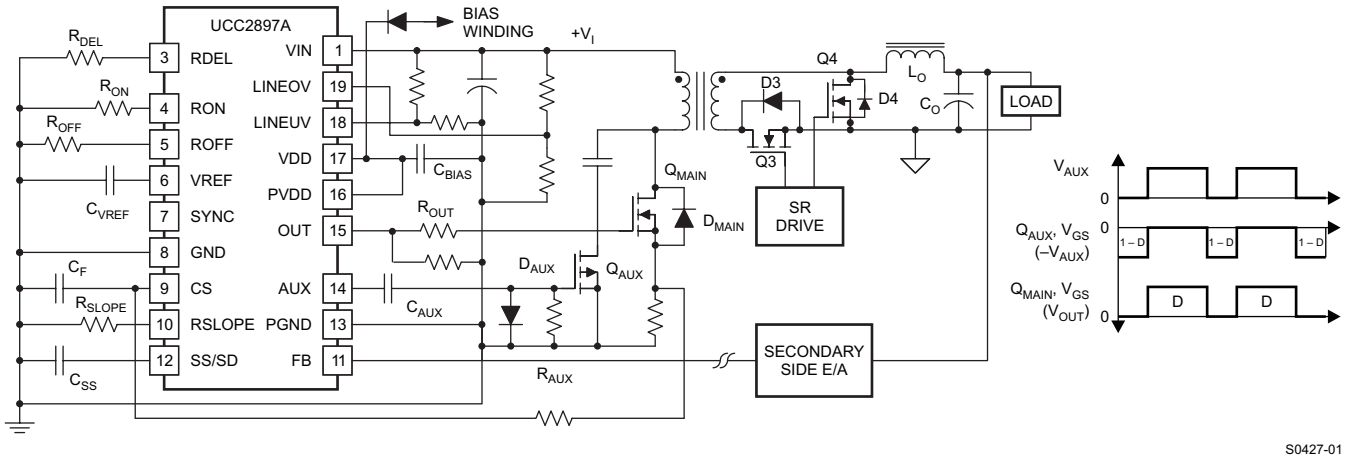

Figure 9. Low-Side Clamp and Gate Drive Circuit

The first time the UCC2897A AUX voltage goes positive, the Schottky diode, D_{AUX}, is forward biased and the capacitor, C_{AUX}, is charged to $–V_{AUX}$ volts. The capacitor voltage then discharges through R_{AUX}. If the time constant of R_{AUX} and C_{AUX} in (47) is much greater than the PWM period, then the voltage across C_{AUX} remains relatively constant and the resultant gate to source voltage seen at Q_{AUX} is $–V_{AUX}$ with a peak positive value of zero volts. Therefore, V_{AUX} is effectively shifted below ground and is now adequate for driving the gate of the ground referenced Pchannel MOSFET, Q_{AUX}.

$$R_{AUX} \times C_{AUX} \cong \frac{100}{f_{SW}} \tag{47}$$

The value of C_{AUX} is determined by arbitrarily choosing R_{AUX} to be 1kΩ, and solving (48).

$$C_{AUX} = \frac{100}{1\,k\Omega \times 250\,kHz} = 0.4\,\mu F \tag{48}$$

4.3.2 Selecting The Clamp Capacitor

The first consideration for sizing the clamp capacitor is to know what the appropriate voltage rating must be over the full range of VIN (shown in Figure 8). It is probably wise to choose a capacitor with a slightly higher voltage rating than the ratings of the FETs.

The value of the clamp capacitor is primarily chosen based on the amount of allowable ripple voltage that can be tolerated. Also, it is assumed that the value of the capacitor is large enough to approximate the clamp voltage as a constant voltage source. However, according to (46) VCr changes with input voltage. Whenever a line transient or sudden change in duty cycle is commanded, it takes some finite amount of time for the clamp voltage, and therefore the transformer reset voltage, to adapt. Larger capacitor values result in less voltage ripple but also introduces a transient response limitation. Smaller capacitor values result in faster transient response, at the cost of higher voltage ripple and higher voltage resonances in step load/line resonances. Ideally the clamp capacitor should be selected to allow some voltage ripple, but not so much as to add additional drain-to-source voltage stress to QMAIN and on the terminals of the self driven secondary side switches. Another factor that must be considered is the transient response of the control loop as the capacitor acting in resonance with the magnetizing inductance of the transformer primary will introduce a pole/zero into the current feedback loop that is a function of $(1\text{-}D)^2$ and will limit the response time of the feedback loop.

Eventually what you will be trading off is the switching FET voltage verses the response time of the control loop as the faster the response the higher the voltage on the Cr capacitor verses saturation limits of the transformer.

Allow approximately 20 percent voltage ripple while paying close attention to VDS of QMAIN and the gate to source voltages of the secondary side rectifiers and the volt-second limitations of the transformer.

A simplified method for approximating C_{CL}, is to solve for C_{CL} such that the resonant time constant is much greater than the maximum off-time. While additional factors such as the power stage time constant and control loop bandwidth also affect transient response, this approach, stated in (49), assures that transient performance is not compromised, at least from the active clamp circuit point of view.

$$2 \times \pi \times \sqrt{L_{MAG} \times C_{CL}} > t_{OFF\_MAX} \tag{49}$$

By solving (49) for C_{CL}, and multiplying the result by a factor of 10 to assure that the inequality of (49) holds true, (49) can be rewritten as (50), expressing C_{CL} in terms of known design parameters:

$$C_{CL} > 10 \times \left(\frac{(1 - D_{MIN})^2}{L_{MAG} \times (2 \times \pi \times f_{SW})^2} \right) \tag{50}$$

Once C_{CL} is calculated by (51), the final design value may vary slightly after the clamp capacitor ripple voltage is measured in circuit.

$$C_{CL} > \frac{10 \times (1 - 0.275)^2}{86.25\ \mu H \times (2 \times \pi \times 250\ kHz)^2} = 24.699\ nF \tag{51}$$

4.4 Primary MOSFET (Q_{MAIN}) Selection

Since the clamp voltage has already been determined from (46), the drain-to-source voltage stress of Q_{MAIN} is also known. Figure 8 shows that the maximum voltage stress over the full input range should be limited to 100 V. Also, the peak drain current of Q_{MAIN} is known from (36). The maximum RMS drain current occurs at minimum input voltage and maximum load current and is 3.895 A as given by (52).

$$I_{QMAIN(RMS)} = \left[\left[\int_{0_{SEC}}^{\frac{D_{MAX}}{f_{OSC}}} \left[\frac{I_O}{N} - \frac{\frac{\Delta I_{LO}}{N} + I_{MAG}}{2} + \left(\frac{\frac{\Delta I_{LO}}{N} + I_{MAG}}{\frac{D_{MAX}}{f_{OSC}}} \right) \times t \right]^2 \times dt \right] \times f_{OSC} \right]^{0.5}$$

$$I_{QMAIN(RMS)} = 3.895\ A = I_{PRI(RMS)} \tag{52}$$

Therefore selecting a MOSFET with a 150 V V_{DS} rating (this allows a 50% surge for the transient conditions) and an ID rating of at least 6.45 A insures a greater than 35 percent design safety margin. The Si7846DP from Vishay Siliconix is a 150 V, 6.7 A, N-channel MOSFET available in thermally enhanced SO8 PowerPAK™ package.

From the manufacturer's data sheet, the total gate charge is approximately 35 nC and the expected on-resistance is 41 mΩ for a 12 V applied gate drive.

Using the $I_{PRI(RMS)}$ current from (52), the conduction loss due to primary current flowing through the channel resistance of Q_{MAIN} is determined from (53). Note that (37) includes the current through Q_{AUX} as well as the Q_{MAIN} current.

$$P_{C(QMAIN)} = I_{PRI(RMS)}^2 \times R_{DS(QMAIN)} = 3.895\ A^2 \times 41\,m\Omega = 0.622\ W \tag{53}$$

As explained in Section 4.4.1, Q_{MAIN} always turns off under ZVS, but will be subject to some turn-on losses from the capacitances on the FETs, as represented by (55). The input voltage condition chosen was low input because it was felt that the conduction losses which are worse at low line would be worse case. We will also be discharging the gate to drain capacitance of Q_{AUX}.

From the charge diagram for the gate in the data sheet, the charge is about 30 nC for a change of Vds of 75 volts and 8 volts on the gate.

This is an effective capacitance of 300 pF.

$$C_{GDEFF} > \frac{Q_{GC\_}Q_{MAIN}}{V_{CL120}} = 302.083\ pF \tag{54}$$

$$P\_SWITCHING\_MAINLV = 0.5 \times \left(C_{GDEFF} + C_{OSS\_QMAIN\_100V} + C_{OSS\_QAUX\_100V}\right) \times V_{CL}^2 \times f_{OSC}$$

$$P\_SWITCHING\_MAINLV = 0.482\ W = P_{SW(QMAIN)} \tag{55}$$

When Q_{MAIN} turns on, Q_{AUX} has already turned off. The primary side magnetizing current is relatively low and because the magnetizing current is needed to charge the drain to source capacitance of Q_{MAIN}, Q_{AUX} and through the transformer, the gates of the secondary FETs, the voltage across Q_{MAIN} does not fall quickly.

This process is described in detail in reference [11]. A short summary is below:

When the Q_{AUX} turns off the magnetizing current and the leakage current are both going into the source, Vin. As a result current is drawn from the drain to source capacitance of Q_{MAIN} and Q_{AUX} causing the voltage across Q_{MAIN} to start to collapse (see Figure 10). However, this causes the voltage across the primary winding to decrease and this is reflected across to the secondary. This collapse on the secondary requires current to discharge the capacitance that is on the secondary windings. This secondary current is provided by the magnetizing current which in turn robs the primary side of current resulting in a continuing decrease in primary current from Q_{MAIN} and Q_{AUX}.

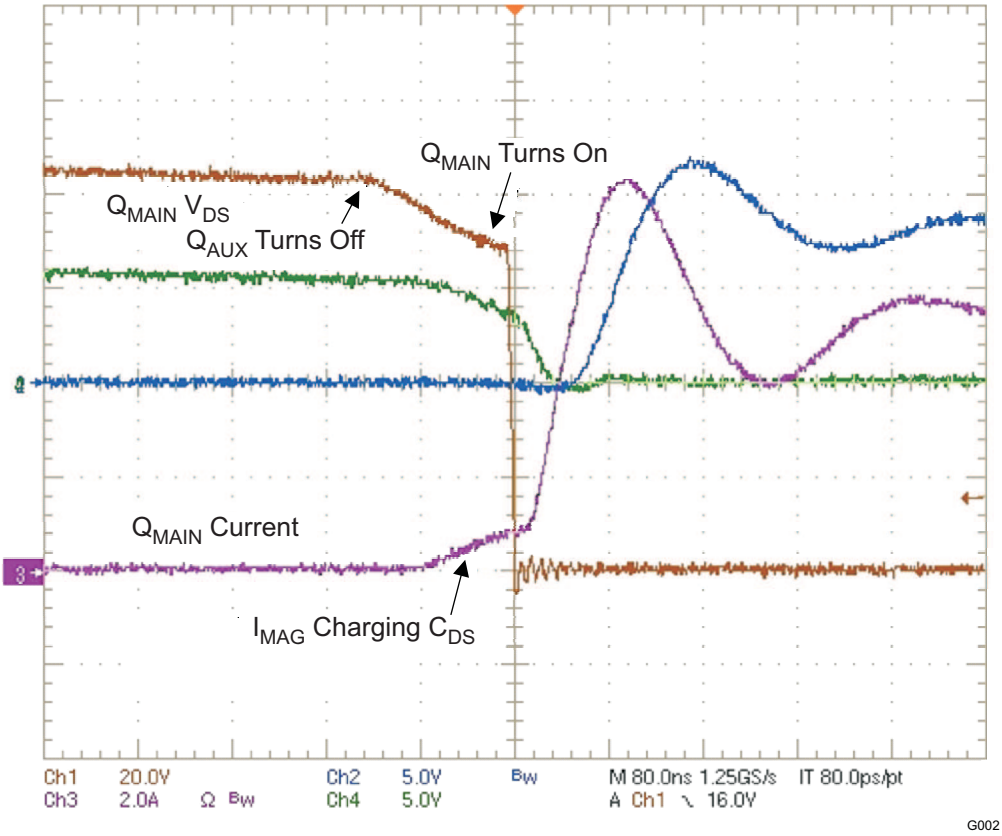

Figure 10. Scope Shot of Qaux Turn-Off/Amain Turn On

This process would take an extended time and would only fall to zero volts across the primary so because of duty cycle limitations it is assumed that the full voltage is across Q_{MAIN} and Q_{AUX} at the instant of turnon. It is also assumed that the current through the primary winding is reverse to that which would be induced by Q_{MAIN} being on and that there is some leakage inductance so Q_{MAIN} is turning on into at least a zero current condition as far as Q_{MAIN} is concerned. For losses then the only losses through Q_{MAIN} will be the capacitive discharge of the drain to source capacitance of Q_{MAIN} itself and of Q_{AUX} assuming that there is no Miller induced turn on of Q_{AUX}.

$$P_{QMAIN(MAX)} = P_{C(QMAIN)} + P_{SW(QMAIN)} = 0.622\ W + 0.482\ W = 1.104\ W \quad (56)$$

A quick check of the maximum junction temperature of QMAIN is calculated to be 89.4 °C as shown in (65).

$$T_J = \left(R_{\theta JA} \times P_{QMAIN(MAX)}\right) + T_A = \left(52^\circ C/W \times 1.104\ W\right) + 40^\circ C = 97.4^\circ C \quad (57)$$

97.4°C is less than 75 percent (113°C) of the absolute maximum junction temperature of 150°C. Never the less, when laying out the PCB, placing additional copper area under the drain tab of the Q_{MAIN} PowerPAK™ also helps to lower the junction temperature.

4.4.1 Primary MOSFET (Q_{MAIN}) ZVS Considerations

The ability to ZVS QMAIN is one of the primary motivations for using the active clamp. Detailing the conditions for ZVS first requires an understanding of the contributing parasitic elements as shown in Figure 11.

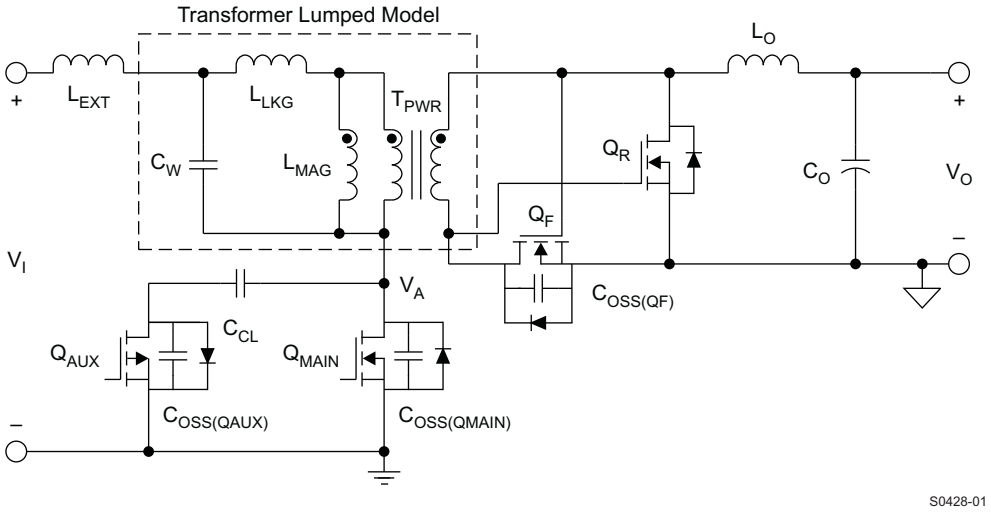

Figure 11. Active Clamp Power Stage With Parasitic Elements

The conditions for ZVS are that the drain-to-source voltage must be zero prior to Q_{MAIN} switching off and that the voltage across Q_{AUX} must be zero before Q_{AUX} switches on. This condition is achieved when the voltage at node V_A, shown in Figure 12, is resonantly driven from zero volts to Vcl within the set time interval. Therefore, for the purpose of ZVS, the circuit of Figure 11 can be reduced to a simple resonant circuit as shown in Figure 12.

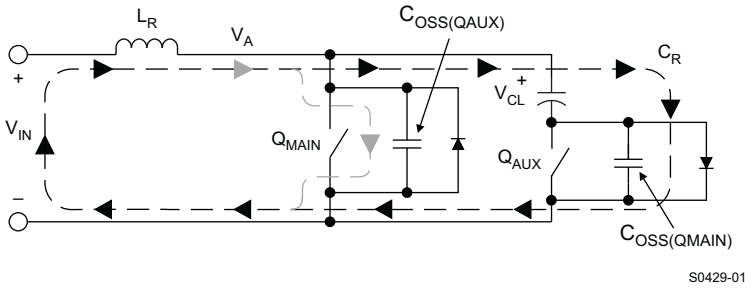

Figure 12. Simplified ZVS Resonant Circuit

During the t1–t2 interval, Q_{MAIN} has just turned off and Q_{AUX} is about to turn on. As $C_{OSS(QMAIN)}$ is charged to V_A, the voltage across Cr the body-diode of Q_{MAIN} is reverse biased and the current that was previously flowing through the channel resistance of Q_{MAIN} is now diverted to $C_{OSS(QMAIN)}$ and $C_{OSS(QAUX)}$.

This current consists of two identifiable components, the load current and the magnetizing current.

The first the load current will continue to flow until the voltage on the drain of Q_{MAIN} reaches the voltage on the input. At that point, it will cease to flow.

However the magnetizing current has no other path and will continue to flow driving the voltage on both drain to source capacitors up until the voltage on the drain of Q_{AUX} reaches one diode drop above ground. At this point the magnetizing current then flows through Cr and the diode of Q_{AUX}. The voltage on Cr has been increasing but because CR is so large compared to the $C_{OSS(QMAIN)}$ and $C_{OSS(QAUX)}$ that it could be ignored during this short interval of time. The voltage on $C_{OSS(QAUX)}$ is one diode drop below ground and Q_{AUX} can be turned on in a ZVS state.

This is described in detail in reference [10].

However, the full load current plus the magnetizing current is flowing through the leakage inductance and this tries to drive the current through the primary. Some of the magnetizing current will be diverted to bias the secondary side capacitances. The majority of the magnetizing current will continue to charge the drain to source capacitances of the primary side FETs until the drain to source capacitances voltage of Q_{AUX} reaches zero and the magnetizing current then starts to go through the parasitic diode of the FET.

At this point the AUX FET can be turned on.

4.5 Input Capacitance

The active clamp forward converter is a buck derived power topology with a pulsed AC input current having a high input di/dt content, as shown in Figure 13.

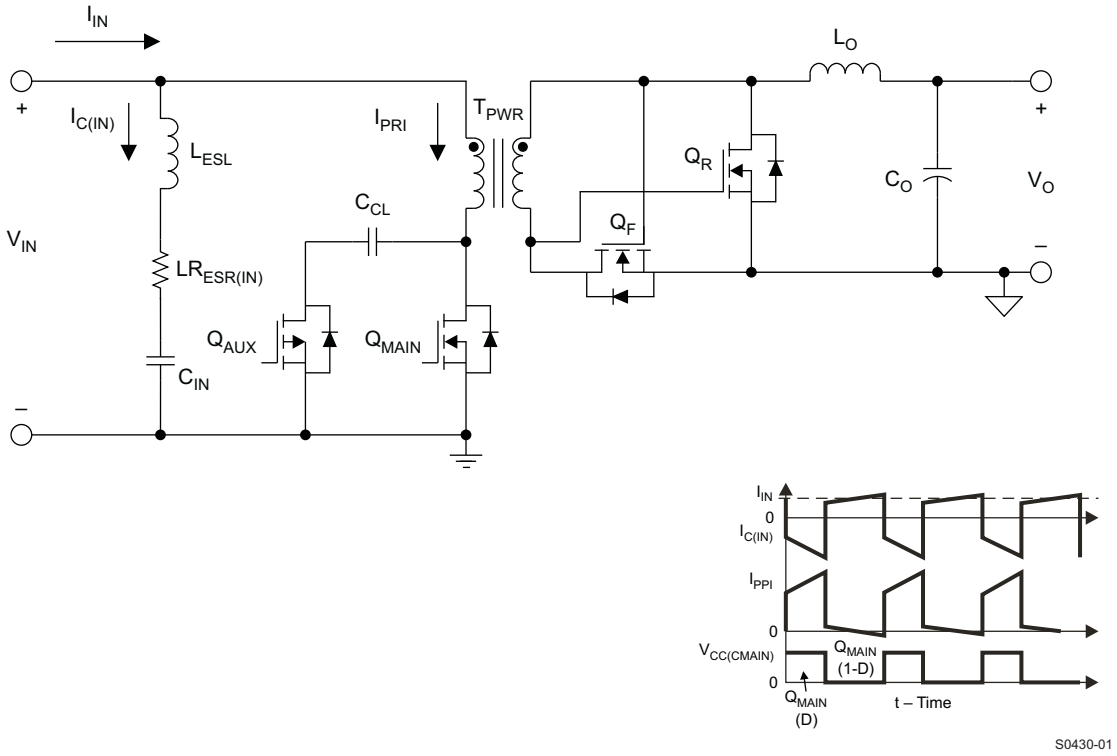

Figure 13. Primary Power Stage Current Waveforms

The DC output current is 30 Amps and if we assume a 50% duty cycle which is usually the worst case for RMS current for the input capacitor this translates into a *DC component* of 2.5 amps in when Q_{MAIN} is off and 2.5 amps during the “ON” time of QMAIN because of the 6 to 1 turns ratio of the transformer.

The output inductor during that time has a peak to peak current ramp of 3.667 amps which is balanced about the DC level so when the Q_{MAIN} turns on, it is about 1.83 amps below the DC and by the time Q_{MAIN} turns off it is 1.83 amps above the DC level. This translates to the primary as 0.611 amps peak to peak or 0.3 amps above and below the current pulse during the *ON* time of Q_{MAIN}.

In addition, the magnetizing current during the *ON* time of QMAIN from the primary side inductance is calculated to be 1.02 Amps. This too will be balanced about zero over each half of the transition or ±0.5 amps.

The DC current into the supply is equal to half of the *DC component* needed because that is average DC current over a 50% duty cycle of 5 amps.

To calculate the RMS current we now have to perform an integration of the square of the current over a cycle divided by the time of that cycle and take the square root of that integral. These integrals are not perfectly balanced as they would be in reality for calculating the RMS current they are close enough.

The integrals for the D and 1-D are calculated separately assuming 50% duty cyce then summed for the RMS current.

$$\mathrm{INteg\_on} = \int_{0\ \mathrm{sec}}^{2\ \mu\mathrm{s}} \left[\left[2.5\ \mathrm{A} - (0.5\ \mathrm{A} + 0.3\ \mathrm{A}) + \left(\frac{1\mathrm{A} + 0.6\ \mathrm{A}}{2\ \mu\mathrm{s}} \times \mathrm{t} \right) \right]^2 \right] \mathrm{dt} \tag{58}$$

$$INteg\_off = \int_{0\ sec}^{2\ \mu s}\left[\left[2.5\ A + (0.5\ A) - \left(\frac{1\ A}{2\ \mu s} \times t\right)\right]^2\right] dt \tag{59}$$

$$IRMS\_inputcap = \left[(INteg\_on + INteg\_off) \times 250\ kHz\right]^{0.5}$$

$$IRMS\_inputcap = 2.529\ A \tag{60}$$

Applying a 25 percent design margin, the input capacitance should be rated to handle at least 3.16 ARMS capacitor current.

For initially choosing the input capacitor it is assumed that the change in ripple voltage is capacitive dominant, although at higher frequency operation L_{ESL} and $R_{ESR(IN)}$ can dominate over C_{IN}. The minimum required input capacitance that would limit the voltage ripple to 5% of the minimum input voltage is given by (62). It is assumed that the worst case ripple current will occur at approximately 50% duty cycle.

The charge coming out of the capacitor during the time the main switch is on and assuming that the input current remain constant is defined in (61).

$$IN\_Q = \int_{0\ sec}^{2\ \mu s}\left[\left[2.5\ A - (0.5\ A + 0.3\ A) + \left(\frac{1\ A + 0.6\ A}{2\ \mu s} \times t\right)\right]\right] dt = 5 \times 10^{-6} C \tag{61}$$

This charge should not result in a voltage change across the capacitor of more than 5% of the minimum input voltage.

$$Cin = \frac{IN\_Q}{36\ V \times 0.05} = 2.778\ \mu F \tag{62}$$

Because the amount of input ripple voltage is large compared to the capacitor ripple current, the $R_{ESR(IN)}$ of the input capacitor is less of a concern than for the output capacitor. Nonetheless, the minimum required $R_{ESR(IN)}$ should still be checked by (63).

$$R_{ESR(IN)} < \frac{0.05 \times V_{IN(MIN)}}{\left(I_{PRI(PK)} + \left(\frac{I_{MAG}}{2}\right)\right)} = \frac{0.05 \times 36\ V}{5A + \frac{1\ A}{2} + \frac{0.3\ A}{2}} = 318.584\ m\Omega \tag{63}$$

For a maximum V_{IN} of 72 V, multilayer ceramic is the most viable capacitor choice. Using two or more parallel ceramic capacitors easily satisfies the $R_{ESR(IN)}$ requirement from (63) while also introducing minimal parasitic inductance. The C4532X7R2A225 is a 2.2 µF, 100 V multilayer ceramic capacitor from TDK rated for 2.5 ARMS at 300 kHz, with an $R_{ESR(IN)}$ of 4 mΩ. Three parallel capacitors are chosen giving a total input capacitance of 6.6µF.

4.6 Current Sensing

The UCC2897A has two current sense thresholds. The pulse by pulse current threshold minimum voltage is 0.43 volts and can go as high as 0.53 volts. This is the threshold that must be met at full load.

The hiccup mode threshold is 0.71 to 0.81 volts. In most cases this will never be encountered as the pulse by pulse current threshold turns the switch off before it can be reached.

The goal of current mode control is to modulate the *ON* time of Q_{MAIN} based upon the error voltage and the current flowing in the output inductor. Because the output current is so high, current sensing is done on the primary side where the switched load current is reduced by the transformer turns ratio. Primary side current sensing can be done using either a small current sense resistor placed in series with the source of Q_{MAIN} or a current sense transformer. When designing for high efficiency, the total losses associated with each approach should be considered.

The resistive current sensing approach is shown in Figure 14, along with the approximate voltage waveform seen across the current sense resistor.

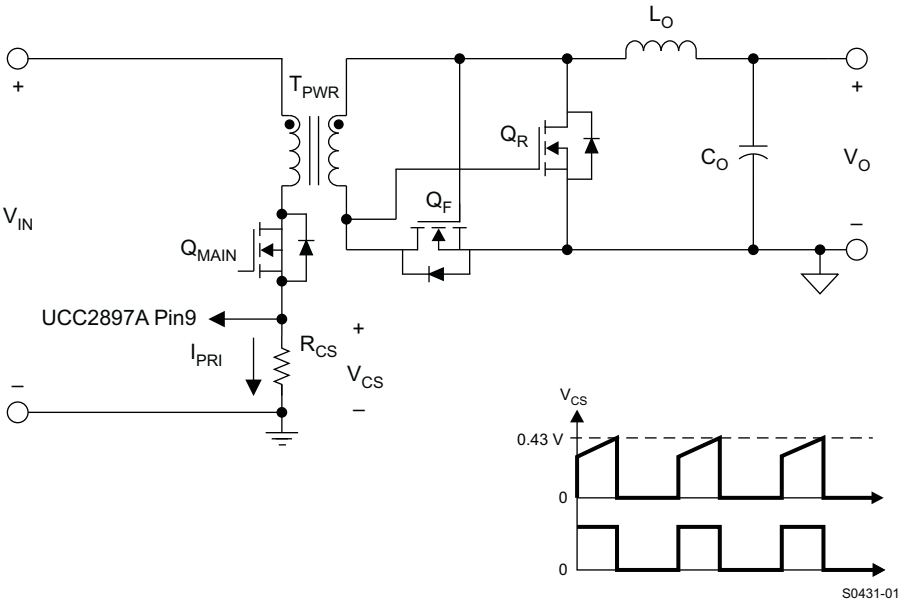

Figure 14. UCC2897A Resistive Current Sensing

From (36), the peak primary current is 5.93A for I_{OUT}=30 A plus half of the output inductor ripple current, but for setting the current limit, the peak primary current is equal to 6.25 A corresponding to I_{LIM}=32 A when you include the primary side magnetizing current. The value of R_{CS} is given by (64).

$$R_{CS} = \frac{V_{CS}}{I_{PRI(CL\_PK)}} = \frac{0.43\ V}{6.25\ A} = 0.069\ \Omega \tag{64}$$

Using the primary RMS current of 4.42 A from (37), the maximum power dissipated in the nominal current sense resistor is given by (65).

$$P_{RCS} = I_{PRI(RMS)}^{2} \times R_{CS} = (3.912\ A)^2 \times 0.069\ \Omega = 1.056\ W \tag{65}$$

Dissipating 1.0 W in the current sense resistor would result in an overall efficiency penalty of about 1%. The impact of this approach should be compared to using a current sense transformer as shown in Figure 15.

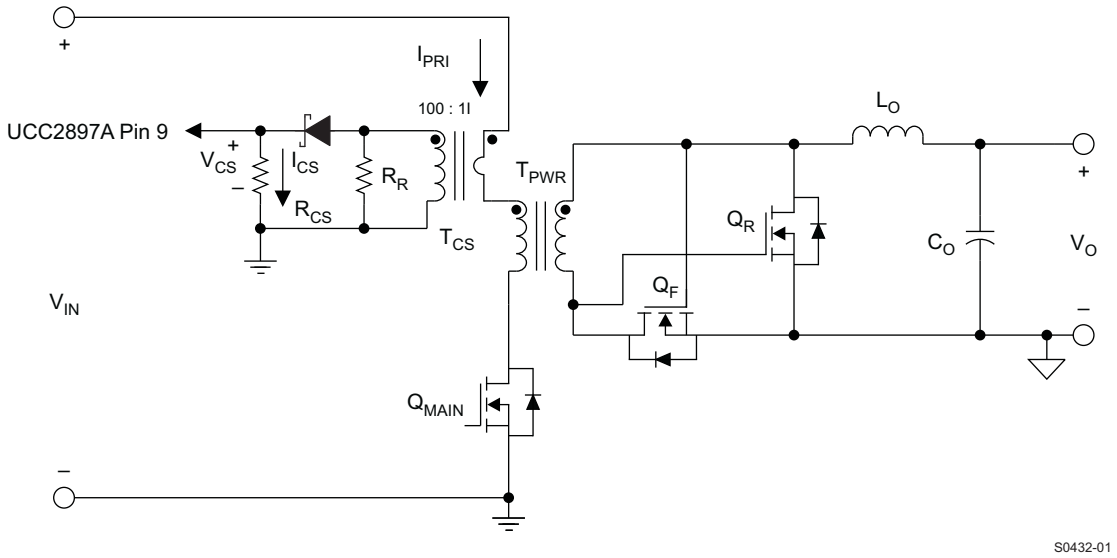

Figure 15. Current Sensing With a Current Sense Transformer

Consider the current sense transformer, T_{CS}, shown in Figure 15. The current flowing through RCS is the primary current, I_{PRI}, reduced by the current sense transformer turns ratio. For a current transformer turns ratio of 100 to 1, I_{CS} during peak current limit is determined by (66).

$$I_{CS(CL\_PK)} = I_{PRI(CL\_PK)} \times \frac{1}{N_{CS}} = \frac{6.25\ A}{100} = 62.5\ mA \tag{66}$$

And from $I_{CS(CL\_PK)}$, the current sensing resistor is calculated by (67).

$$R_{CS} = \frac{V_{CS}}{I_{CS(CL\_PK)}} = \frac{0.43\ V}{62.5\ mA} = 6.88\ \Omega \tag{67}$$

Using the primary RMS current of 4.42 A from (37), the maximum power dissipated in the 6.9 Ω current sense resistor is given by (68).

$$P_{RCS} = \left(\frac{I_{PRI(RMS)}}{N_{CS}}\right)^2 \times R_{CS} = \left(\frac{3.895\ A}{100}\right)^2 \times 6.9\ \Omega = 10.468\ mW \tag{68}$$

Because of the early release of the EVM the current sense resistor on the EVM is 4.64 Ω and the current limit point is approaching 44 A.

For T_{CS}, the P8208 100:1 current sense transformer from Pulse is rated to handle up to 10 A of primary current, and has a maximum height of less than 5 mm. The largest contribution of power dissipation comes from the primary current flowing through the single turn dc resistance. For the P8208, the dc resistances are 6 mΩ for the single turn primary and 5.5 Ω for the 100 turn secondary. The current sense transformer conduction losses are given by (69) and (70).

$$P_{TCS(PRI)} = I_{PRI(RMS)}{}^2 \times R_{PRI} = (3.912\ A)^2 \times 6\ m\Omega = 91.822\ mW \tag{69}$$

$$P_{TCS(SEC)} = \left(\frac{I_{PRI(RMS)}}{N_{CS}}\right)^2 \times R_{SEC} = \left(\frac{3.912\ A}{100}\right)^2 \times 5.5\ \Omega = 8.417\ mW \tag{70}$$

The Schottky rectifier used in the sensing circuit of Figure 15, also adds a small amount of power dissipation as a product of the RMS current and diode voltage drop when the diode is conducting. Assuming a forward voltage drop, V_F, of 0.6 V, the power dissipated in the diode can be approximated by (71).

$$P_{CS(DIODE)} = V_F \times \left(\frac{I_{PRI(RMS)}}{N_{CS}}\right)^2 = \left(\frac{3.912\ A}{100}\right)^2 \times 0.6\ V = 23.472\ mW \tag{71}$$

The final component to consider is R_R, which is used to reset the current sense transformer during the off-time. Since R_{CS} is much smaller than R_R, the secondary RMS current always flows to R_{CS} when the diode is conducting. When the current sense diode is non-conducting, R_R is present to maintain current flowing in the transformer secondary necessary for reset. Therefore the reset volt-seconds are determined by the value of R_R. R_R should be selected such that the transformer reset time is shorter than the minimum reset time of the power transformer, T_{PWR}. Increasing R_R has the effect of reducing the reset time but increasing the reset voltage, causing additional voltage stress to the current sensing diode. For minimal voltage stress on the current sense diode, an approximation for R_R is given by (72).

$$R_R = \frac{(V_{CS} + V_D) \times D_{MAX} \times N_{CS}}{(1 - D_{MAX}) \times I_{MAG}} = \frac{(0.43\ V + 0.6\ V) \times 0.6 \times 100}{(1 - 0.6) \times 1\ A} = 154.5\ \Omega \tag{72}$$

The total power dissipated using the current sense transformer can now be determined by (73).

$$P_{TCS} = P_{RCS} + P_{TCS(PRI)} + P_{TCS(SEC)} + P_{CS(DIODE)} \tag{73}$$

$$P_{TCS} = 10.53\ mW + 91.82\ mW + 8.42\ mW + 23.472\ mW = 134.242\ mW \tag{74}$$

Comparing the result of (74) to (65), the power dissipated using the current sense transformer technique of Figure 15 results in only 134.2 mW of total power dissipation compared to 1.05 W when a current sense resistor is used in series with the Q_{MAIN} MOSFET source. This is almost always the case for low input voltage, high current design applications and even for some offline applications it may be worthwhile to compare the losses for each of the two current sensing techniques.

4.7 Summary of Power Stage Losses

The power dissipated by the output inductor still has to be calculated. Looking at the data sheet for the inductor chosen, the winding resistance is 2.5 milliohms.

$$D_{CRLO} = 2.5\ m\Omega \qquad I_{LO\_RMS} = 30.037\ A$$

$$P\_D_{CRL0} = I_{LO\_RMS}^{2} \times D_{CRLO} = 2.255\ W \tag{75}$$

The core losses are so small relatively speaking that they are ignored.

The total full load power dissipation (from a 100 W load) in only the power stage is summarized in Figure 16 and is estimated to be approximately 10.75 W, resulting in an estimated full load efficiency of 90%. The power estimate of Figure 16 neglects the losses in the input and output capacitors, as well as the loss in the Q_{AUX} MOSFET, but these are assumed to be minimal within the scope of this estimation.

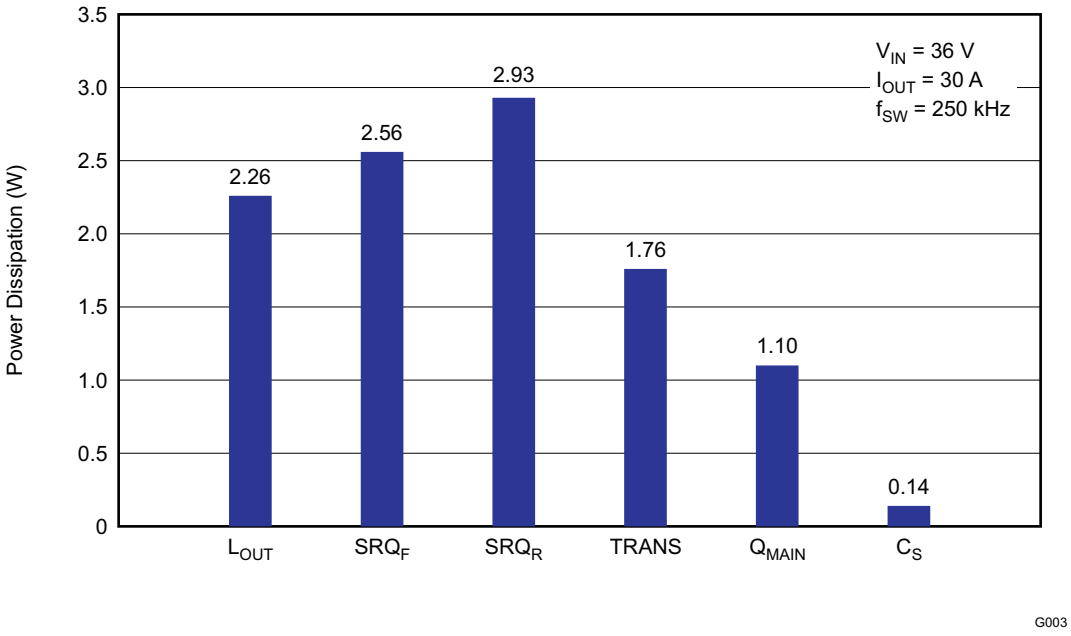

Figure 16. Power Stage Loss Estimate

5 Optocoupler Voltage Feedback

The UCC2897A PWM controller modulates the duty cycle using current mode control (CMC). The current sense information is derived from the primary side as discussed in the previous section. However, the dc error signal necessary for the voltage loop portion must be fed back from the secondary side to the primary side. Crossing the isolation boundary can be accomplished by using magnetic feedback or optocoupler feedback. Since the output inductor already provides the primary referenced bootstrap bias, adding a second coupled winding to gather the error voltage feedback signal is not desirable for this example. Therefore to keep all the component choices OTS, an optocoupler is used and is configured as shown in Figure 17.

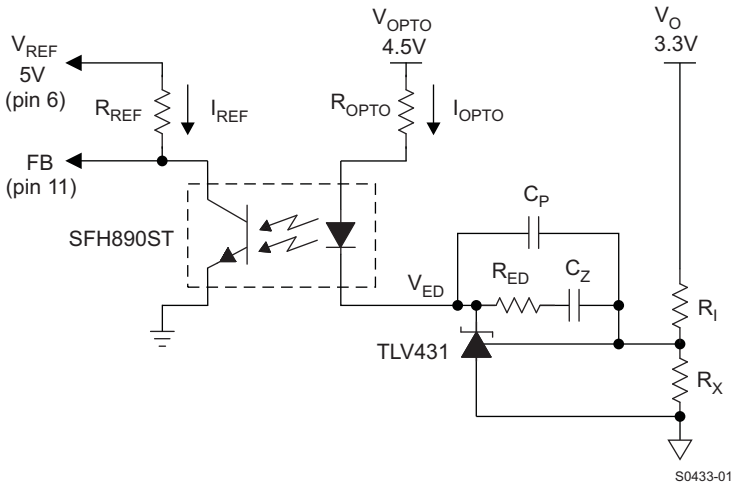

Figure 17. Optocoupler Feedback and Secondary Side Compensator

There are several components that are added to the feedback loop to overcome the turn on overshoot that is inherent to an integrating feedback loop. The discussion and analysis need to select and place these is discussed in *Defeating Turn On Overshoot* and will not be dealt with here other than to refer the reader to the article reference [14].

The minimum voltage on the feedback pin to get output pulses is defined by the Current Sense Level Shift voltage times the resistor ratio within the device which yields (0.48V × 5) 2.4V.

The recommended usable voltage at the FB pin of the UCC2897A is within the range of 2.4 V < V_{FB} < 5 V. When V_{FB} is less then 2.4 V the UCC2897A operates in a pulse skipping mode.

Since the converter has synchronous rectification the converter should never go into pulse skipping mode. This means that because of the sync rectifier action the feedback pin should never go below 2.4V.

Therefore over the full 2:1 V_{IN} range, the FB voltage can be expected to change proportionally within the range of 2.4 V < V_{FB} < 5.0 V. The next consideration is that the reference voltage of the UCC2897A can only source 5 mA of current. Since V_{REF} is used as the pull-up voltage for the optocoupler output, the maximum allowable I_{REF} of less than 2 mA during operation.

Arbitrarily we will choose a 2 kΩ resistor.

$$I_{REF(MIN)} = \frac{V_{REF} - V_{FB(MAX)}}{R_{VREF}} = \frac{5\ V - 2.4\ V}{2\ k\Omega} = 1.3\ mA \quad (76)$$

From equation (76) we are well under the design limit during operation at minimum duty cycle.

The SFH690BT has a Current Transfer Ratio (CTR) between 100% and 300%. If the optocoupler is biased for the minimum CTR of 100%, then the current, I_{OPTO}, should be equal to the result of (77). This means that it should operate even if the CTR is 100%.

$$I_{OPTO(MIN)} = \frac{I_{REF(MIN)}}{CTR_{(MIN)}} = \frac{1.3\ mA}{1} = 1.3\ mA \tag{77}$$

Since the TLV431 can sink up to 25 mA of cathode current, there is plenty of headroom for driving the optocoupler. In order to minimize the DC gain of the optocoupler, 20 percent of the maximum TLV431 current is allowed. The optocoupler biasing resistor, R_{OPTO}, can be determined from (78). V_{OPTO} is selected based upon the minimum transformer secondary voltage of 6 V minus 1.5 V of headroom for a simple series pass regulator design.

Since the probability is that the CTR will be more to the middle we will assume a CTR for calculation of 200%. All this will do is reduce the required current through the biasing resistor.

Testing however highlighted a noise immunity problem with the series regulator under certain load conditions and the circuit was modified to produce a voltage of approximately 9 volts before the series regulator but kept the 4.5 V DC level at the output of the series regulator. The current through the optocoupler photodiode has to be able to go from a maximum of 1.3 mA to near 0 mA. The forward voltage drop of the opto-coupler diode is 1.3 V at 5 mA and the TLV431 minimum usable voltage will be defined as 1.24V. Theoretically there is approximately 2 V variation needed on the secondary side to achieve a 1.3 mA change through the optocoupler and photo diode but because the conditions are not the ideal defined conditions this was cut to 1/3.

$$R_{OPTO} = \frac{V_{OPTO} - V_F - V_{SC}}{I_{TLV431}} = \frac{\left[4.5\ V - \left(1.3\ V + 1.24\ V\right)\right] \times 0.33}{1.3\ mA} = 497.538\ \Omega \tag{78}$$

Based on the selected biasing resistors and the minimum CTR, the minimum gain of the optocoupler is given by (79).

$$G_{OPTO} = \left(\frac{R_{VREF}}{R_{OPTO}}\right) \times CTR = \frac{2\ k\Omega}{497\ \Omega} \times 2 = 8.048 = 18.114\ dB \tag{79}$$

Since the maximum duty cycle requires that the voltage on the Vfb pin approach Vref then the voltage across the photo diode must approach the forward volt drop of the photo diode. Since we have synchronous rectifiers the minimum current through the current sense resistor on the primary will be half the ripple current on the output inductor translated to the current sense resistor. The voltage on Vfb will be less than the Vref under all normal operational conditions.

Once the circuit is built and tested the overall control loop needs to be optimized. Since the gain of the optocoupler is part of the overall converter gain, the optocoupler biasing resistors may be adjusted to optimize the PWM feed back voltage.

Because of the undocumented pole of the CTR at higher frequencies (reference [15]) provision was made for a zero to be added to the optocoupler gain by R30 and C25.

These components will be added if needed at test.

6 Compensating the Feedback Loop

The overall control loop is shown in Figure 18. The loop consists of five gain blocks denoted by K, Gcl(s), Gf(s), Gc(s) and Gopto(s). K represents the primary side of the converter and consists of the current sensing circuit, slope compensation and feedback voltage all used as controlling inputs to the PWM comparator. The UCC2897A includes slope compensation circuitry that is internal to the control device but externally programmable by a single resistor from R_{SLOPE} to ground reference.

A discussion of the effect of the active clamp on the feedback loop is discussed in reference [8].

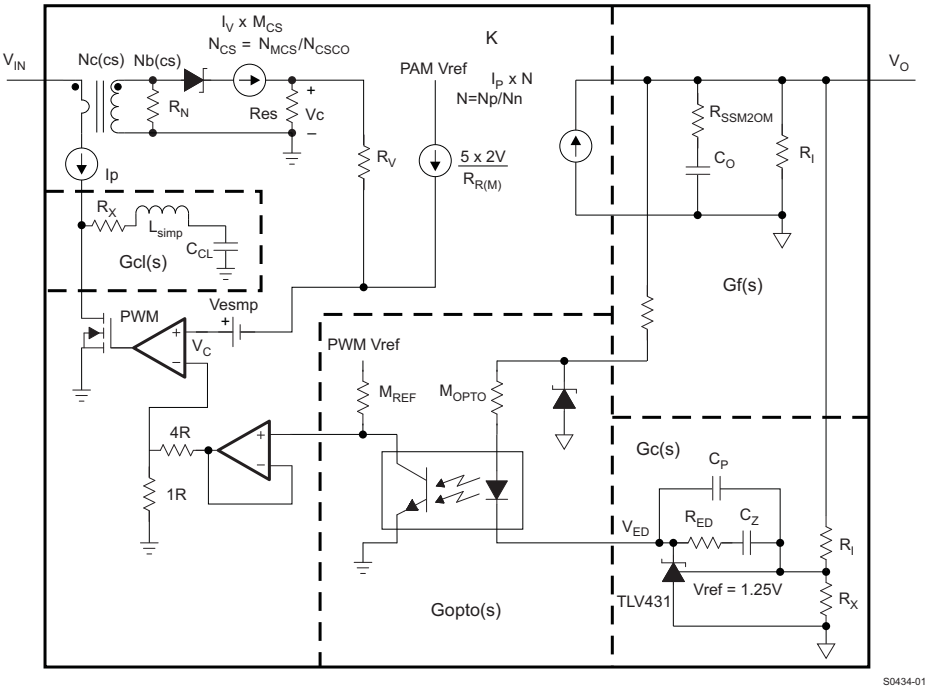

Figure 18. UCC2897A Control Schematic

Gcl(s) is the second order resonance effect formed between the transformer primary magnetizing inductance and clamp capacitor. This gain has a $(1\text{-}D)^2$ function because the only time the magnetizing inductance is connected to the clamp capacitor is during the *OFF* time of the main switch. As such, it has no direct impact on the control loop but does influence the gain as it's effect affects the residual magnetizing current in the transformer and will impact both phase and gain at the resonant frequency of the primary side magnetizing inductance and the clamp capacitor's capacitance. This resonant frequency is a function of the duty cycle. The author has been unable to find a satisfactory mathematical means of adding this to the control loop equation however the documentation clearly indicates that the gain crossover must be before this resonance.

Even though the control loop of a voltage mode converter using this power topology does not suffer from the same feedback loop limitation, the impact of the resonance of the clamp capacitor and the magnetizing inductance on the voltage across the clamp capacitor and the potential for saturation of the transformer imposes similar restrictions on the loop bandwidth.

Gf(s) is the secondary side of the power stage shown with the output inductor removed. Because the output inductor current is one of the control variables, the double pole effect normally seen in voltage mode controlled converters is removed thus simplifying the compensation.

Gc(s) is the secondary side compensator using a TLV431 set up in a type 2 configuration. Because of its low cost, the TLV431 is a very popular choice for use as the error amplifier.

Gopto(s) is the optocoupler gain block as described in the previous section. The varying TLV431 cathode voltage sets the diode current of the optocoupler. The gain and CTR of the optocoupler determine the emitter current seen on the primary side. The varying emitter current is then used to set the DC control voltage seen by the UCC2897A. Inside the UCC2897A, the feedback voltage is buffered and divided down by 1/5 before the inverting input of the PWM comparator.

From the control schematic of Figure 18, a simplified gain block diagram is shown in Figure 19. With the exception of Gc(s), the components that make up each block are known and can now be used to define the control to output transfer, Gco(s).

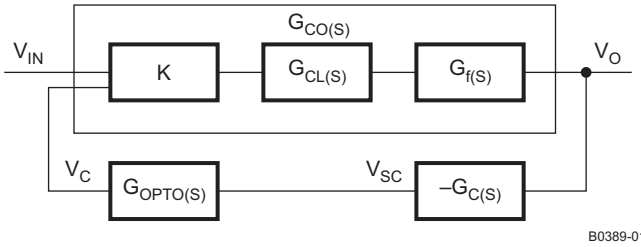

Figure 19. UCC2897A Simplified Control Block Diagram

The gain constant K is simplified and defined by (80). The additional voltage placed on the current sense pin due to slope compensation also has a small negligible effect on K, but it is omitted here for simplification. The ratio of the internal resistors which divide down the control signal to meet the voltage of the current sense pin is included here. Vcontrol (Vc) is the voltage at the feedback pin.

$$K = \frac{\Delta V_O}{\Delta V_C} = \frac{N \times R_L}{\frac{R_{CS}}{N_{CS}} \times 5} = \frac{N \times N_{CS} \times V_O}{I_{O(MAX)} \times R_{CS} \times 5} = 1.913 \tag{80}$$

Unique to the active clamp operating in peak CMC, is a resonant effect occurring between the transformer magnetizing inductance and the clamp capacitor. This will impact the control loop design and is discussed in more detail in references [7] and [8]. Because the clamp capacitor is only connected during the time that Q_{AUX} is *ON* it results in a shift in the resonance as a function of $1/(1\text{-}D)^2$.

Since the clamp capacitor is not the only capacitance that is involved, the impact on the frequency is not as clean as the equation suggests. The effective capacitance of the synchronous switches on the output, add into the equation resulting in the resonant frequency being lowered further than the analysis suggests. We will ignore them and recognize the cause of the tested results occurring at a lower than expected frequency. Also ignored will be any core losses which would tend to dampen the peak of the resonance.

$L_{MAG} = 86.25\mu H$ $C_{CL} = 24.699\ nF$ $D_{MIN} = 0.3$ $D_{MAX} = 0.6$

$$G_{CL\_DMIN} = \frac{1}{L_{MAG} \times \frac{C_{CL}}{(1-D_{MIN})^2}} \times \frac{1}{(j \times \omega)^2 + j \times \omega \times \frac{R_{DCPRI}}{L_{MAG}} + \frac{1}{L_{MAG} \times \frac{C_{CL}}{(1-D_{MIN})^2}}} \tag{81}$$

$$G_{CL\_DMAX} = \frac{1}{L_{MAG} \times \frac{C_{CL}}{(1-D_{MAX})^2}} \times \frac{1}{(j \times \omega)^2 + j \times \omega \times \frac{R_{DCPRI}}{L_{MAG}} + \frac{1}{L_{MAG} \times \frac{C_{CL}}{(1-D_{MAX})^2}}} \tag{82}$$

The change of the resonant frequency due to the different duty cycles with different input voltages are shown in Figure 20.

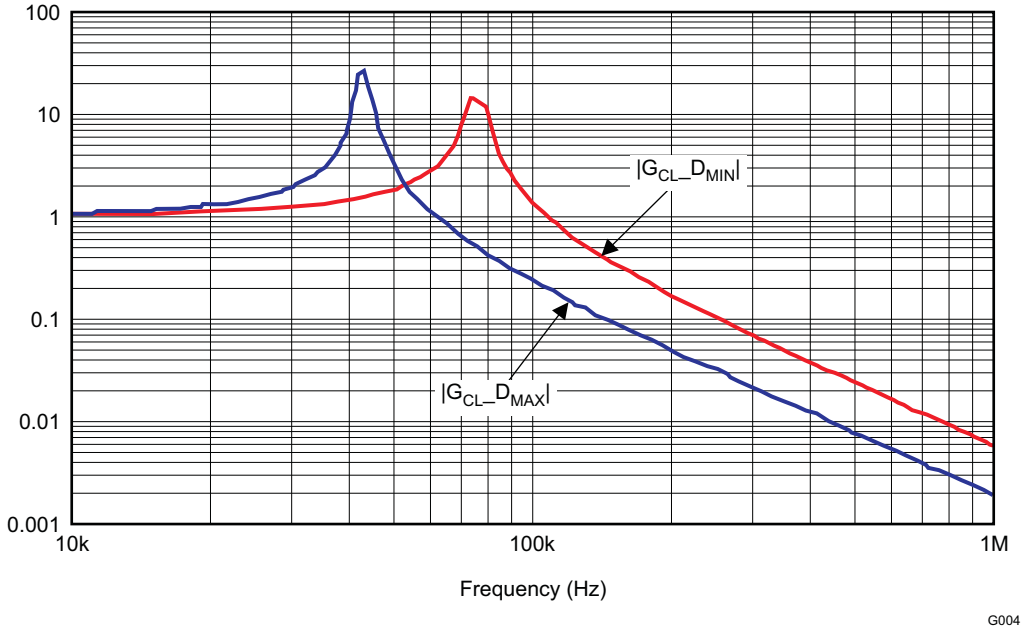

Figure 20. Effect of the Magnetizing Inductance and Clamp Capacitor on Part of the Control to Output Gain Loop

Since the clamp capacitor is not connected to the current sense resistor you might think that there is no impact from this resonance but in reality it impacts the magnetizing current which forms a part of the current that is sensed.

To illustrate this imagine that the converter is in a steady state minimum load condition. This has the voltage across the capacitor in a stable oscillation.

Now assume there is load change to maximum. The control loop responds by increasing the duty cycle and this results in an increase delta in the magnetizing current during the *ON* time and less time for a decrease in the magnetizing current during the shortened *OFF* time. This repeats over several cycle creating a net increase in the magnetizing current and the voltage across the clamp capacitor. The changed magnetizing current which becomes significant is added into the total current being monitored. The control loop which has increased to get a certain current to the load is delivering that magnitude of current but a disproportionate amount of that current is the magnetizing current. This effectively reduces the control to output gain of the loop.

In addition the phase delay of this current will also impact the control loops phase shift. Both of these effects are felt at the resonant frequency of the effective clamp capacitor and the magnetizing inductance as a function of $1/(1-D)^2$.

The rest of the control loop is straight forward.

The transfer function, Gf of the output filter is reduced to a first order system given by (83). This function is the output impedance of the load in parallel with the output filter normalized about the DC impedance of the output filter. Therefore as the load impedance changes so does the gain. In Figure 21 are the gains as a function of frequency, shown for the maximum load and for a load that is 10% of the maximum DC load.

$$G_F = \frac{j \times \omega \times C_O \times R_{ESR} + 1}{j \times \omega \times (R_{LOAD} + R_{ESR}) \times C_O + 1} \tag{83}$$

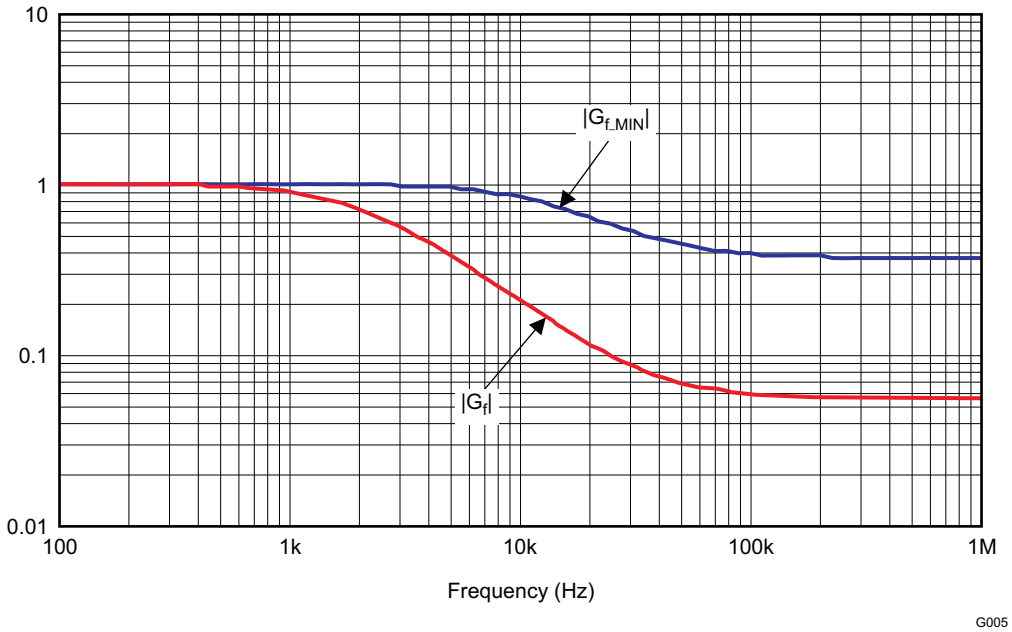

Figure 21. Gain of the Output Load and Capacitor as a Function of Frequency and Rload

As shown in Figure 19, the control to output gain of the system is given by (84) and specifically in the frequency domain by equation (85). The equation is a function of the load (Rload) as shown in equation (85)

$$G_{CO(S)} = K \times G_{f(S)} \tag{84}$$

$$G_{CO} = \left(\frac{N \times N_{CS} \times V_O}{I_O \times R_{CS} \times 5} \right) \times \left(\frac{j \times \omega \times C_O \times R_{ESR(OUT)} + 1}{j \times \omega \times (R_L + R_{ESR(OUT)}) \times C_O + 1} \right) \tag{85}$$

The control to output gain is plotted below. There are two separate conditions considered. These are at full load and at 10% load.

They break down as follows:

G1 is maximum load,
G2 is 10% load

The effects of the resonance of the primary side magnetizing inductance with the clamp capacitor are ignored as there is no satisfactory way to mathematically model then but they will be a factor is choosing the 0 db crossover point and test results will be used to fine tune the crossover point.

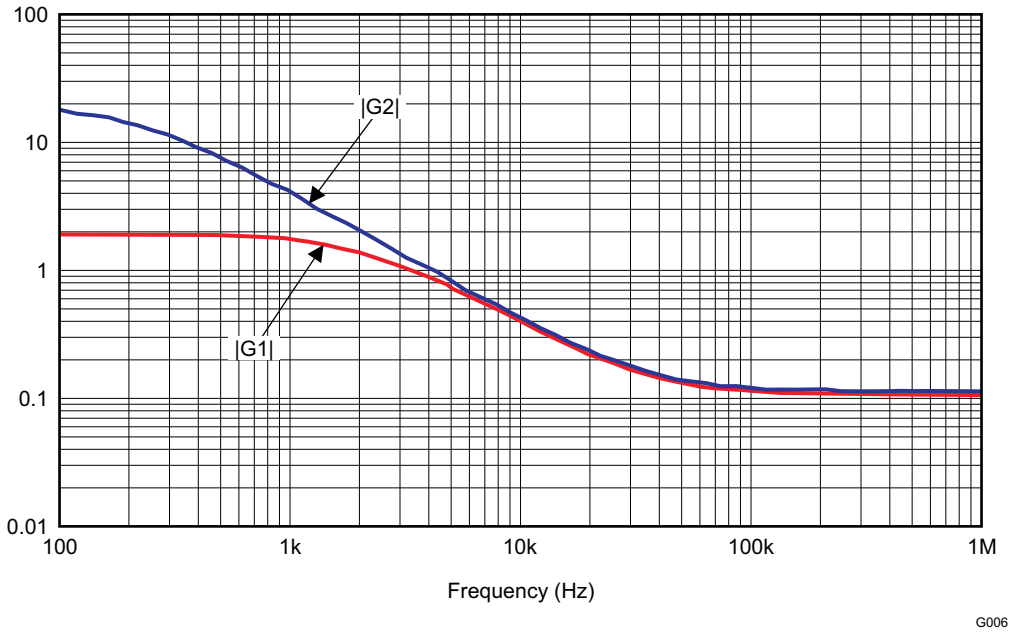

Figure 22. Graph Showing the Plot of the Control to Output Gain Incorporating all the Previous Defined Equations

From (79), the dc gain of the optocoupler, Gopto, has already been calculated as 12 dB. However, the optocoupler also exhibits an undocumented single pole roll off occurring at roughly 30 kHz, and can be combined with Gopto to give (86), which represents the optocoupler performance with frequency. (See reference [15])

Since the small signal response of an optocoupler is not specified within the manufacturer's data sheet and can vary for a given application, it should be measured in circuit to validate the assumptions used in the control loop model.

$$G_{OPTO(S)} = \frac{G_{OPTO}}{1 + S \times \left(\frac{1}{2 \times \pi \times 3\ \text{kHz}} \right)} \tag{86}$$

For a forward converter operating in peak CMC, a type 2 compensation network is generally used. For the CMC active clamp forward converter this compensation scheme can be used when the overall crossover frequency is designed to be at least a factor of 5 lower than the resonant frequency of the clamp. The desired crossover frequency is defined by (88).

$$F_{CL} = \frac{1}{2 \times \pi \times \sqrt{L_{MAG} \times \frac{C_{CL}}{(1-D)^2}}} = \frac{1}{2 \times \pi \times \sqrt{86\ \mu\text{H} \times \frac{25\ \text{nF}}{(1-0.6)^2}}} = 43.417\ \text{kHz} \tag{87}$$

$$F_O \le \frac{F_{CL}}{5} \tag{88}$$

From (88) the crossover frequency, F_0, of the control loop is selected to be 8 kHz.

By plotting (86) (opto coupler gain assuming a CTR of 200%) and adding the result to G1, the total closed loop uncompensated gain and phase are now known and the compensation network that makes up Gc(s) in Figure 18 can now be designed as follows. From Figure 23, and equation (89) the uncompensated overall gain is about 12.5 dB at F0=8 kHz.

The required absolute gain at F_0 is the inverse of that given by (89). The compensator needs to be designed to have a –12.5 dB gain at the crossover frequency.

$$G_{dB} = 20\log\left(\left|G2\right|\right) + 20\log\left(\left|\frac{\frac{2\ k\Omega}{479\ \Omega}\times 2}{1+\frac{j\times\omega}{2\times\pi\times 30\ kHz}}\right|\right) = 12.585 \quad (89)$$

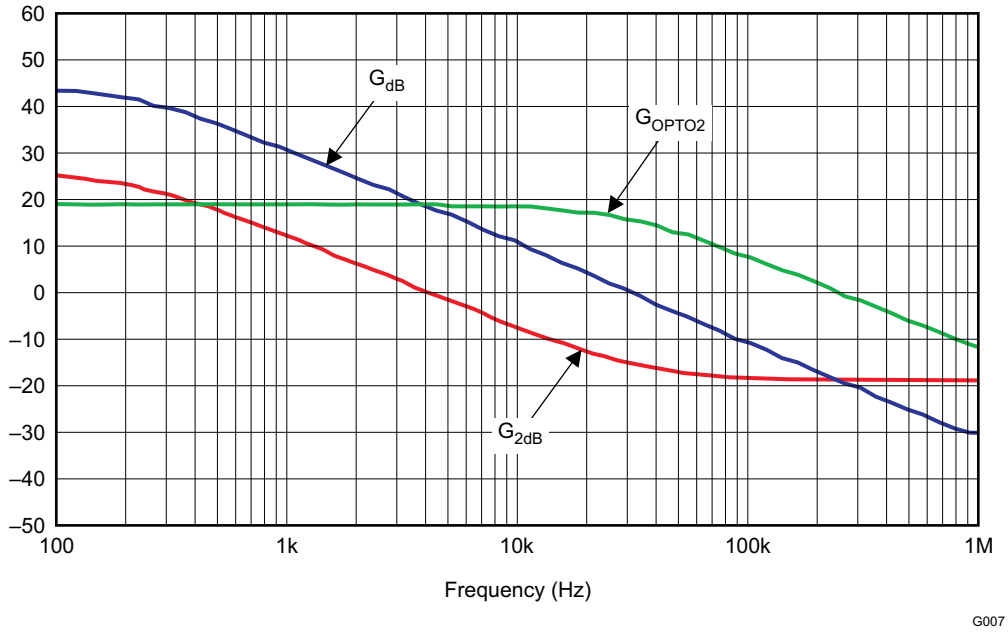

Figure 23. Control to Output gain

Figure 23 showing the Control to Output gain, with (GdB) and without (G2dB), the opto-coupler gain added in, and the optocoupler gain (Gopto) all by itself. The optocoupler gain is assuming a CTR of 200%.

If R_X (Figure 18) is arbitrarily chosen to be 17.4 kΩ, then R_I can be calculated from (90). Actual component values used in the final design are in the text after the equation.

$$R_I = R_X \times \frac{V_O - V_{REF}}{V_{REF}} = 17\ k\Omega \times \frac{(3.3\ V - 1.25\ V)}{1.25\ V} = 27.88\ k\Omega \quad (90)$$

R_X is two resistors in series R27 is 12.1 k and R28 is 4.99 k for a total of 17.09 kΩ. The input resistor RI is also made of two resistors R25 which is 51.1 Ω and R26 which is 28.7 kΩ for a total of 28.75 kΩ. This should result in about 50mV more than the 3.3V and help compensate conduction losses in the connector.

The required gain at cross over is calculated from (91) and the feedback resistor, R_{FB}, is chosen to provide the required negative gain at F_0 and is calculated from (92) where.

$$gc(F_0) = \frac{1}{\frac{2k\Omega}{479\Omega} \times 2 \times |G2|} = 0.227 \tag{91}$$

$$R_{FB} = gc(F_0) \times R_I = 0.227 \times 27.88\,k\Omega = 6.329\,k\Omega \tag{92}$$

The actual value used after testing for RFB was 5.11 k to decrease the measured loop gain. The most probable cause of the higher than calculated gain was the optocoupler CTR. The design assumed a CTR of 200% and in reality it is probably somewhere between 200% and 300%. In addition, a zero was added across R18 to shift the phase at the crossover frequency to remove the phase shifting effect of the pole in the opto-coupler.

The pole formed by R_{FB} and C_P is used to roll off the noise from the switching frequency and is set at half the oscillator frequency by the formula (93). This is standard practice for a forward CMC converter.

$$R_{FB} = 5.11\,k\Omega$$

$$C_P = \frac{1}{2 \times \pi \times F_{OSC} \times 0.5 \times R_{FB}} = 249.166\,pF \tag{93}$$

C_P is set to 220 pF.

The zero formed by R_{FB} and C_Z is used to provide additional phase boost at F_0. It was desirable to have the phase shift from the error amp essentially flat when the loop goes through the 0dB point. To this end C_Z is determined to equal R_{FB} at 1/20th the crossover frequency F_{co} from (94).

$$F_{CO} = 8\,kHz$$

$$C_Z = \frac{1}{2 \times \pi \times R_{FB} \times 0.05 \times F_{CO}} = 77.864\,nF \tag{94}$$

We choose 82 nF for the value. This gives an equation for the gain of the opamp of (95)

$$G_{AMP} = \left(\frac{1}{\frac{1}{5.11\,k\Omega - \frac{1_j}{\omega \times 82\,nF}} + 1_j \times \omega \times 0.22\,nF} \right) \frac{}{28.7\,k\Omega} \tag{95}$$

The opto-coupler had a zero added by adding a series resistor/capacitor across R_{opto} that introduced a zero at about 40 kHz and then a pole at 400kHz. This introduced a phase shift that boosted the phase starting at 4 kHz and improved the gain margin for better stability specifically over the frequency of the double pole perturbations introduced by the active clamp capacitor and the magnetizing inductance.

Equation 96 shows the gain equation for the optocoupler in this configuration with a CTR of 100% which is the minimum. If we increase this to 200% (assumed nominal) or 300%, the defined maximum, we will need to multiply this by 2 or 3 respectively. These gain of the minimum opto-coupler frequency response with the additional zero/pole circuit is shown in figures 25 A (gain) and B (phase).

Figure 24 shows the gain and phase of the opto-coupler and components.

$$\text{Gain} = \frac{2\,\text{k}\Omega}{\dfrac{1}{\dfrac{1}{499\,\Omega} + \dfrac{1}{51.1\,\Omega - \dfrac{\text{j}}{\omega \times 8.2\,\text{nF}}}}} \times \frac{1}{\left(1 + \dfrac{\text{j} \times \omega}{2 \times \pi \times 30\,\text{kHz}}\right)} \quad (96)$$

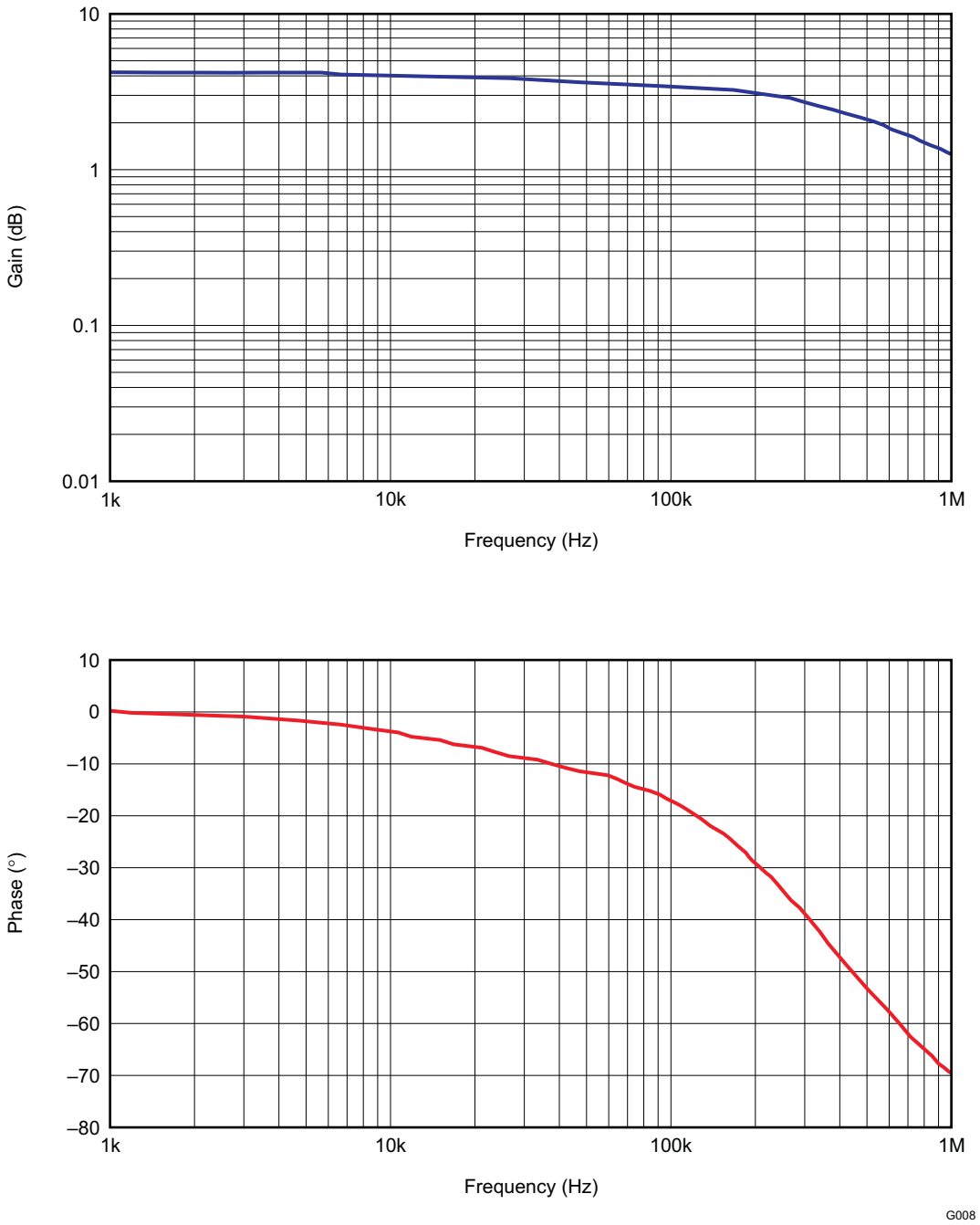

Figure 24. Gain and Phase of the Opto-Coupler and Components

The final component values tested in the actual design were only slightly changed from calculated values and are shown for completeness in Figure 25.

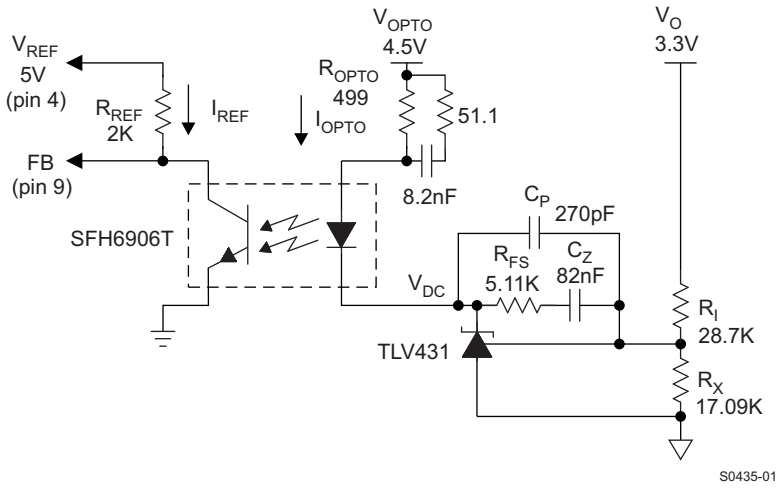

Figure 25. Type 2 Compensator (Final Component Design Values Shown)

The calculated gain and phase responses of the compensated TLV431 are shown in Figure 26.

At F_0=8 kHz, the compensator has a gain of –15 dB. Also shown in Figure 26, is a blue line indicating the maximum gain bandwidth product (GBW) of the open loop TLV431. For this design, the compensated network is well below the GBW limit, but it should be noted nonetheless. Figure 25 shows the phase compensator boost of nearly 0° at the designed crossover frequency.

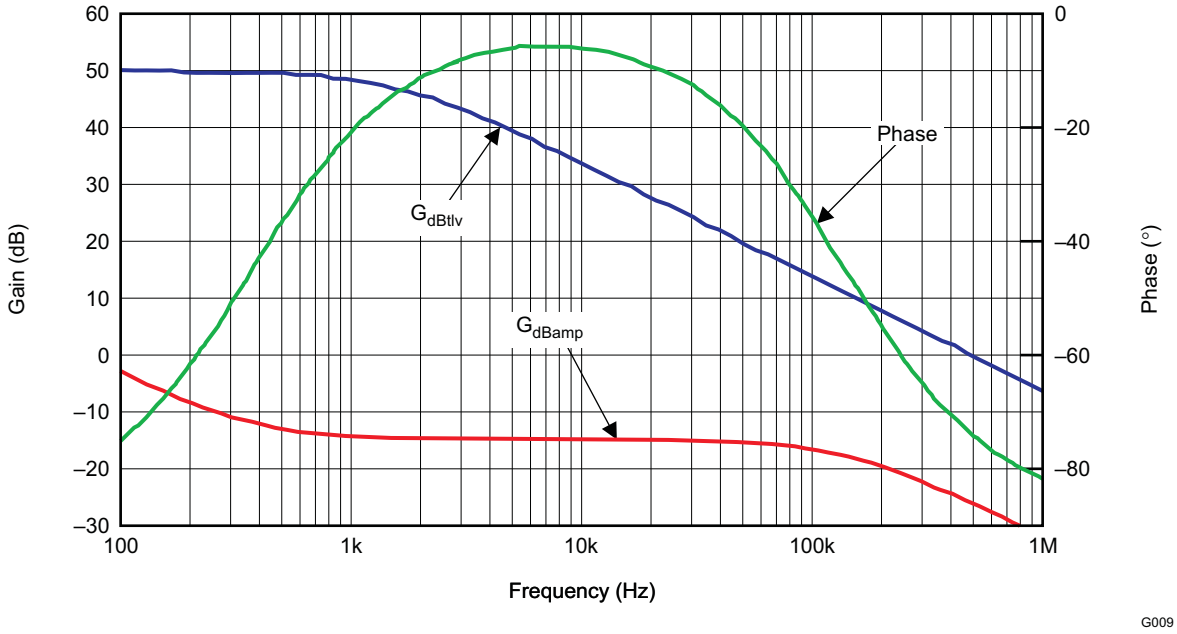

Figure 26. Type 2 Compensation Gain and Phase

With the circuit of Figure 24 introduced into the design, and adding in the gain and phase shift of the optocoupler the calculated total open loop gain and phase responses are shown in Figure 27. This does not include any perturbation caused by the magnetizing inductance and clamp capacitor resonance but does include the nominal and extremes for the current transfer ratios of the optocoupler.

From the loop gain response of Figure 27, the crossover frequency of 8 kHz is achieved with a gain of about 40 dB at low frequency gain.

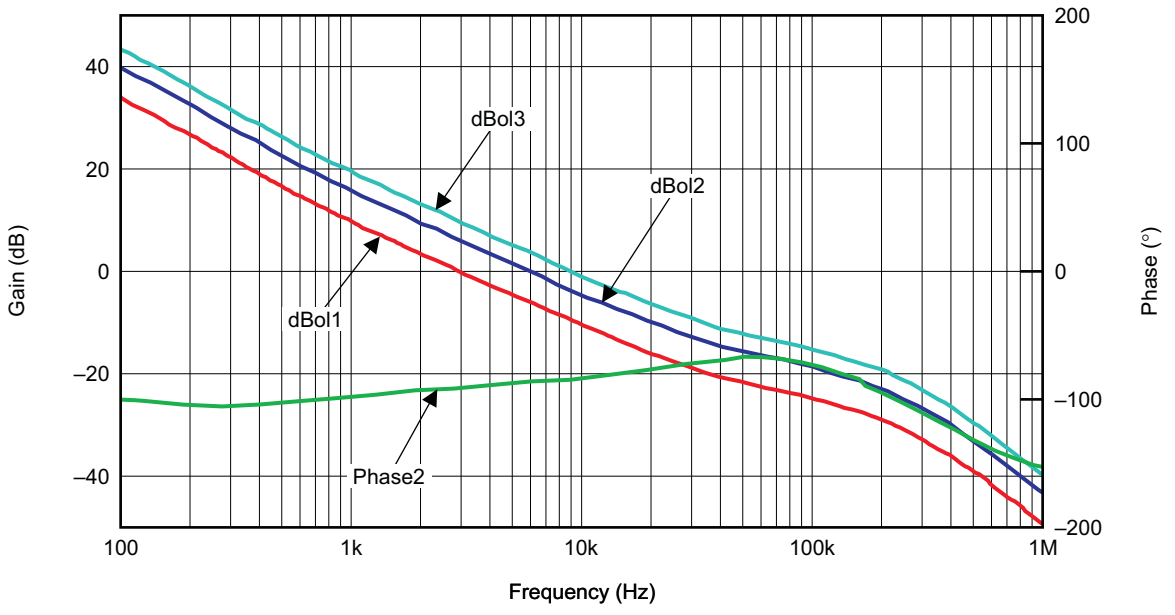

Figure 27. Calculated Total Overall Loop Gain and Phase

7 Programming the UCC2897A PWM Control IC

Using design information from the power stage, the PWM controller can now be set up. This is generally the final step in completing the power converter design. The following design equations are intended to complement the step by step, set up procedure shown in the application section of references [1] and [2]. Actual component values used in the design are shown to the right of each result.

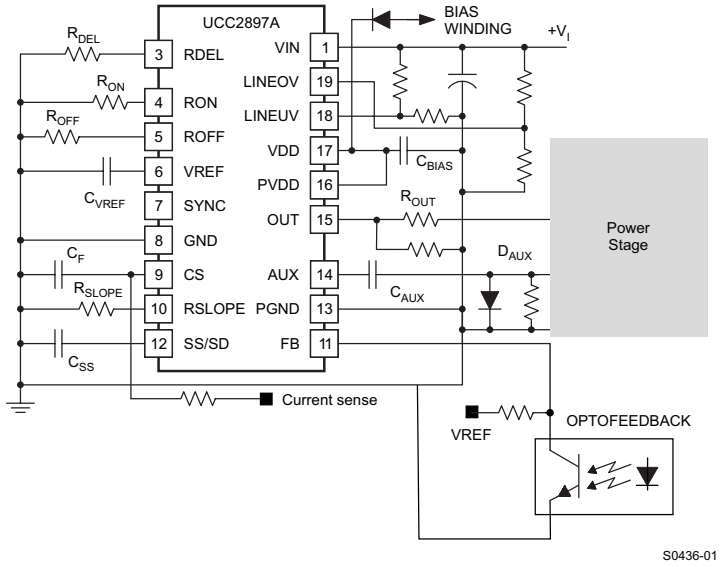

Figure 28. UCC2897A Set Up Diagram

7.1 Step 1. Oscillator

From the power stage design we know the maximum on time and the desired frequency. We will arbitrarily set the delay time to 0.1 µs.

$$F_{OSC} = 250\ \text{kHz} \qquad D_{MAX} = 0.6 \qquad t_{DEL} = 0.1\,\mu\text{s}$$

$$t_{ON} = 36.1\times10^{-12}\times R_{ON}\times\left(\frac{S}{\Omega}\right) + t_{DEL}\,(S) \tag{97}$$

$$t_{OFF} = 15.0\times10^{-12}\times R_{OFF}\times\left(\frac{S}{\Omega}\right) + t_{DEL}\,(S) + 170\times10^{-9}\times(S) \tag{98}$$

The oscillator frequency and maximum duty cycle clamp are set by R_{ON}, R_{OFF}, and R_{delay} according to (99) (100) and (101).

$$R_{DEL} = \frac{t_{DEL} - 15.0\times10^{-9}\times(S)}{11.1\times10^{-12}\times\left(\frac{S}{\Omega}\right)} = 7.658\ \text{k}\Omega \tag{99}$$

$$R_{ON} = \frac{t_{ON} + t_{DEL}}{36.1\times10^{-12}\times\left(\frac{S}{\Omega}\right)} = 69.252\ \text{k}\Omega \tag{100}$$

$$R_{OFF} = \frac{t_{OFF} + t_{DEL}\,(S) - 170\times10^{-9}\times(S)}{15.0\times10^{-12}\times\left(\frac{S}{\Omega}\right)} = 88.667\ \text{k}\Omega \tag{101}$$

The actual numbers used were 8.45K for R_{DEL}, 69.8K for R_{ON} and 88.7K for R_{OFF}.

7.2 Step 2. Soft Start

The soft start capacitor is set according to a desired soft start time applied to (102). For this example a soft start time of 30 ms is arbitrarily chosen.

$$C_{ss} = \frac{2.5\ V \times 0.43 \times t_{SS}}{R_{ON} \times (4.5\ V - 2.5\ V)} = \frac{2.5\ V \times 0.43 \times 30\ ms}{69.8\ k\Omega \times (45\ V - 2.5\ V)} = 231.017\ nF \rightarrow 0.22\ \mu F \quad (102)$$

This time only covers the time that the capacitor is going from 2.5 volts to 4.5 volts. In actual fact the Ic is active but not switching from the time the the voltage on the softstart capacitor starts to increase even though no switching is present. This means that the soft start capacitor should be full charged about 60 ms after the Vref voltage goes to 5 volts.

The softstop discharge current is the same as the charge current so in this gives about 30ms of soft stop time.

However, turn-on overshoot proved to be a problem and additional circuitry was added on the secondary to provide an override to this softstart although the softstart capacitor was left in place as it is also used for soft stop which prevents the self oscillation of the synchronous rectifiers described in reference [12].

The soft start method is discussed in detail in reference [14].

7.3 Step 3. VDD Bypass Requirements

First the high frequency filter capacitor is calculated based on gate charge parameters of Q_{MAIN} and Q_{AUX}. Assuming that the switching frequency ripple should be kept below 100 mV across C_{HF}, its value can be approximated by (103). From the data sheet for the SI7846 $Q_{G(QMAIN)}$ is 35 nC, and from the IRF6216 AUX MOSFET data sheet, $Q_{G(AUX)}$ is also 35 nC.

$$C_{HF} = \frac{Q_{G(QMAIN)} + Q_{G(QAUX)}}{0.1\ V} = \frac{35\ nC + 35\ nC}{0.1\ V} = 700\ nF \rightarrow 1\ \mu F \quad (103)$$

When the VDD reaches the minimum turn on voltage the Vref voltage comes up to 5 volts and the device starts to draw current to power the internal electronics. Current starts to flow to the Css capacitor but the output switches can not start until after Vss reaches 2.5 volts. After Vss reaches 2.5 volts the output switches can start.

The design is such that the Vss takes 30 ms to go from 2.5 volts to 4.5 volts so it will take slightly longer to go from 0 V to 2.5 V. This energy must be added to the energy needed to power the device for the time it takes to go from 2.5 V to 4.5 V.

This will be calculated in 3 equations. Equation 104 will be the energy in the Vref capacitor.

$$Q_{CREF} = 5\ V \times 0.1\ \mu F = 500\ nC \quad (104)$$

Equation 105 will deal with the energy from the charging of the Vref capacitor to the start of the main switches.

$$Q_{SS\_1} = 3\ ma \times 30\ ms \times \frac{2.5\ V}{4.5\ V - 2.5\ V} = 112.5\ \mu C \quad (105)$$

Equation 106 deals with the energy involved from the time the switches start operating until the maximum voltage is reached.

The number of switch cycles is the 30 ms times the operating frequency. Each of those cycles based on the devices choosen has to charge the gate input capacitor and it has been calculated that this is 2 amps of current for 20 ns and that both the Q_{AUX} and Q_{MAIN} have the same requirement.

$$I_{DD} = 3\ \text{ma} \qquad T_{RISE} = 30\ \text{ms} \qquad I_{GATE\_QMAIN} = 2\ \text{A} \qquad I_{GATE\_QAUX} = 2\ \text{A} \qquad T_{RISE\_SW} = 20\ \text{ns}$$

$$\text{Charge\_Cbias} = I_{DD} \times t_{RISE} + F_{OSE} \times t_{RISE} \times \left[\left(I_{GATE\_QMAIN} \times t_{RISE\_SW} \right) + \left(I_{GATE\_QAUX} \times t_{RISE\_SW} \right) \right]$$

$$= 3 \times \text{ma} \times 30 \times \text{ms} + \left[250 \times \text{kHz} \times 30 \times \text{ms} \times \left(2 \times \text{A} \times 20 \times \text{ns} + 2 \times \text{A} \times 20 \times \text{ns} \right) \right] = 690\ \mu\text{C} \tag{106}$$

The total charge needed by the device to start the converter is the sum of Equation 104 through Equation 106.

This gives a total charge calculated in Equation 107 and is equal to the change in charge required to change the capacitor voltage.

$$\text{ChargeVdd} = Q_{SS\_1} + \text{Charge\_Cbias} + Q_{CREF} = 803\ \mu\text{C} \tag{107}$$

This charge has to be delivered by the input capacitor during a change in voltage from 12.2 volts (minimum start voltage) and 7.8 volts (12.2 volts less minimum hysterisis voltage of 4.4 volts).

From this information the size of the capacitor can be determined by Equation 108.

$$\text{Cbias} = \frac{\text{ChargeVdd}}{12.2\ \text{V} - 7.8\ \text{V}} = 182.5\ \mu\text{F} \tag{108}$$

The difference between Equation 9 and Equation 108 is covered by the different softstart times and the amount of charge on each of the gates.

As stated after Equation 9 this capacitance did not include the variations on Iss and the impact this would have on the softstart time. If we take that into account the capacitance requirement increases to approximately 320 µF.

This was felt to be too large a capacitor to put on the test board as it would have taken too long to charge so a series regulator for the input Vcc was installed.

7.4 Step 4. Input Voltage Monitoring

The amount of hysteresis current fed back to the LINEUV comparator is first calculated by Equation 109.

$$I_{HYST} = \frac{2.5\ V}{R_{DEL}} \times 0.05 = \frac{2.5\ V}{8.45\ k\Omega} \times 0.05 = 14.793\ \mu a \tag{109}$$

The amount of hysteresis voltage is specified by the difference between V_{ON} and V_{OFF} in Table 1, and is used to calculate R_{IN1} from Equation 110.

$$R_{IN1} = \frac{V_{ON} - V_{OFF}}{I_{HYST}} = \frac{35\ V - 34\ V}{14.8\ \mu a} = 67.568\ k\Omega \rightarrow 26.7\ k\Omega \tag{110}$$

This lower value of resistor will in actual fact give us only about 0.4 volts of hysteresis. Which is what we are seeing on the unit.

The low-side resistor of the LINEUV divider is now easily calculated from Equation 111.

$$R_{IN2} = R_{IN1} \times \frac{1.27\ V}{V_{OFF} - 1.27\ V} = 26.7\ k\Omega \times \frac{1.27\ V}{34\ V - 1.27\ V} = 1.036\ k\Omega \rightarrow 1\ k\Omega \tag{111}$$

7.5 Step 5. Current Sense Filtering and Slope Compensation

The UCC2897A PWM controller uses an internal slope compensation scheme that is externally programmable by appropriately selecting two resistors, R_F and R_{SLOPE}. The current sense filter resistor, R_F, is selected based upon the chosen corner frequency of the low pass filter formed by R_F and C_F. As a starting point, a general rule of thumb is to select the corner frequency to be 10 times the switching frequency. Also, C_F should be chosen between the recommended limits of 47 pF≤C_F≤270 pF. Arbitrarily picking C_F equal to 100 pF, R_F can be determined from Equation 112.

$$R_F = \frac{1}{2 \times \pi \times (10 \times F_{SW}) \times C_F} = \frac{1}{2 \times \pi \times (10 \times 250\ kHz) \times 100\ pF} = 636.62\ \Omega \tag{112}$$

The actual value used on the EVM is 1.82 kΩ.

The closest standard resistor value of 536 Ω is chosen for R_F. The output inductor current slope must now be defined as it is reflected from the secondary, back to the primary and then translated to a voltage slope seen across the current sense resistor, R_{CS}. When a current sense transformer is used, the voltage equivalent compensation ramp can be determined from Equation 113.

$$\frac{dV_L}{dt} = \frac{(V_{IN(MIN)} \times N_S - V_O \times N_P) \times N_S \times R_{CS}}{N_P^2 \times L \times N_{CS}} \tag{113}$$

$$\frac{dV_L}{dt} = \frac{(36\ V \times 1 - 3.3\ V \times 6) \times 1 \times 6.9\ \Omega}{6^2 \times 2\ \mu H \times 100} = 0.016 \frac{V}{\mu s} \tag{114}$$

For applications that do not use a current sense transformer, Equation 113 can still be applied by making the NCS term equal to one. Using the calculated values of R_F and dV_L/dt, R_{SLOPE} can now be determined from Equation 115.

From the data sheet the Ct voltage goes from zero to 2 volts in the time that the converter main switch can be on.

$$R_{SLOPE} = \frac{5 \times 2\ V \times R_F}{\left(\frac{D_{MAX}}{F_{SW}}\right) \times m \times \left(\frac{dV_L}{dt}\right)} \tag{115}$$

$$R_{SLOPE} = \frac{5 \times 2\ V \times 636\ \Omega}{\frac{D_{MAX}}{250\ kHz} \times 1 \times 15.525 \times \frac{mV}{\mu s}} = 170.692\ k\Omega \tag{116}$$

The actual value used was 158 kΩ.

8 Schematic and List of Materials

The schematic diagram for the design example is shown in Figure 29. Component values shown may differ slightly from calculated values. Also shown in Figure 29 is each manufacturer and component part number corresponding to the schematic shown in Figure 29.

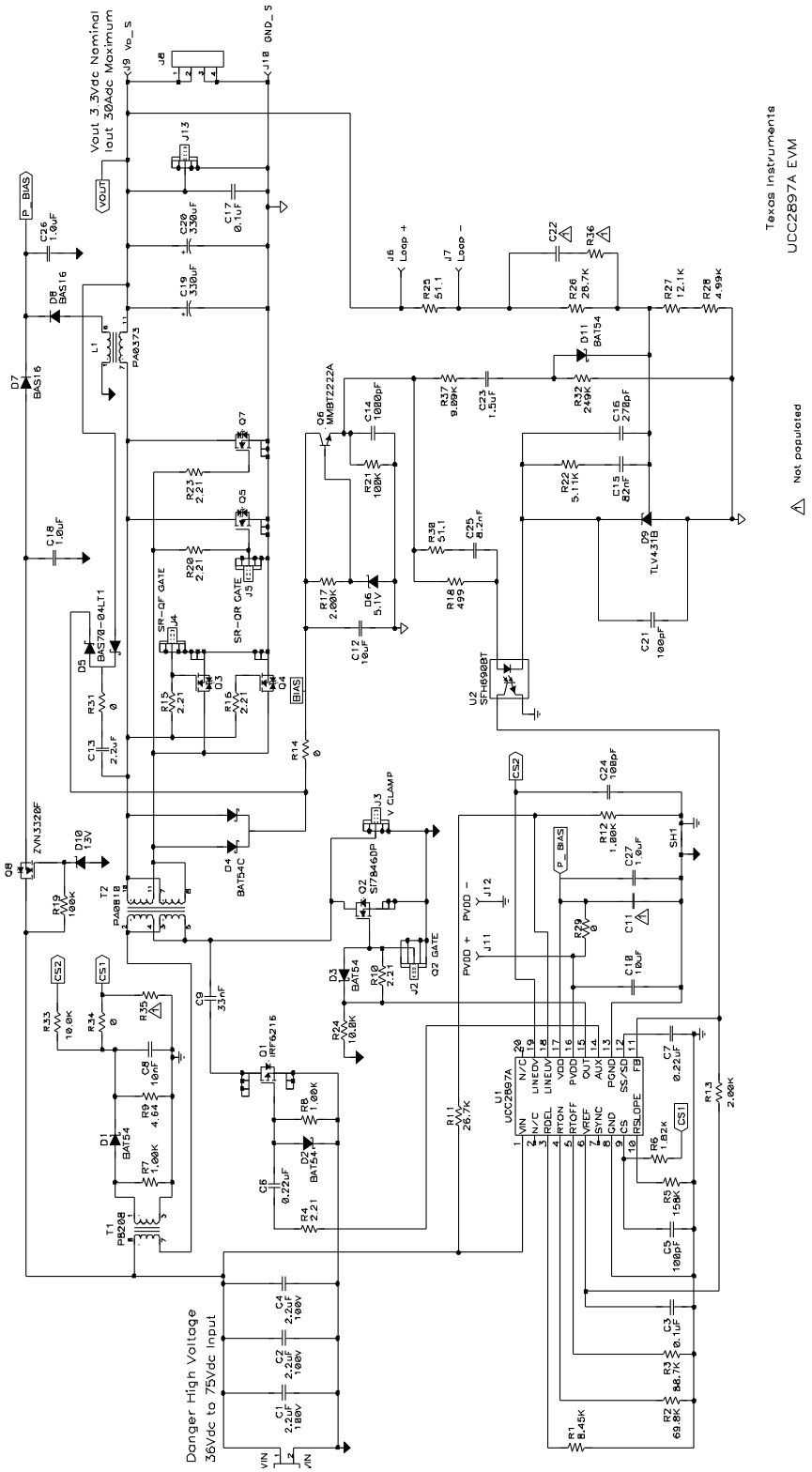

Figure 29. UCC2897A Design Example Schematic

Table 3. UCC2897A Design Example List of Materials

Count	Ref Des	Value	Description	Size	Part Number	MFR
3	C1, C2, C4	2.2uF	Capacitor, Ceramic, 2.2uF, 100-V, X7R, 20%	1812	C4532X7R2A225M	TDK
2	C10, C12	10uF	Capacitor, Ceramic, 16V, X5R, 20%	1206	std	std
0	C11	open	Capacitor, Ceramic, vvV, [temp], [tol]	1210	Std	Vishay
1	C13	2.2uF	Capacitor, Ceramic, 25V, X5R, 10%	0805	std	std
1	C14	1000pF	Capacitor, Ceramic, 50V, X7R, 20%	0805	std	std
1	C15	82nF	Capacitor, Ceramic, 50V, X7R, 10%	0805	std	std
1	C16	270pF	Capacitor, Ceramic, 50V, X7R, 10%	0805	std	std
3	C18, C26, C27	1.0uF	Capacitor, Ceramic, 25V, X7R, 10%	0805	std	std
2	C19, C20	330uF	Capacitor, POSCAP, 9.0 mOhms, 6.3V, 20%	7343 (D)	6TPF330M9L	Sanyo
0	C22	open	Capacitor, Ceramic, 50V, X7R, 10%	0805	std	std
1	C23	1.5uF	Capacitor, Ceramic, 16V, X7R, 10%	0805	std	std
1	C25	8.2nF	Capacitor, Ceramic, 50V, X7R, 10%	0805	std	std
2	C3, C17	0.1uF	Capacitor, Ceramic, 50V, X7R, 20%	0805	std	std
3	C5, C21, C24	100pF	Capacitor, Ceramic, 50V, NPO, 10%	0805	std	std
2	C6, C7	0.22uF	Capacitor, Ceramic, 50V, X7R, 20%	0805	std	std
1	C8	10nF	Capacitor, Ceramic, 50V, X7R, 20%	0805	std	std
1	C9	33nF	Capacitor, Ceramic, 250 V, X7R, 10%	1206	std	std
4	D1, D2, D3, D11	BAT54	Diode, Schottky, 200-mA, 30-V	SOT23	BAT54	Vishay
1	D10	13V	Diode, Zener, 13-V,150-mW	SOT23	BZX84C13-7-F	Diodes
1	D4	BAT54C	Diode, Dual Schottky, 200-mA, 30-V	SOT23	BAT54C	Vishay
1	D5	BAS70-04LT1	Diode, Dual series Schottky, 70-V	SOT23	BAS70-04LT1	On Semi
1	D6	5.1V	Diode, Zener, 5.1-V, 350-mW	SOT23	BZX84C5V1	Vishay
2	D7, D8	BAS16	Diode, Switching, 200-mA, 85-V, 350-mW	SOT23	BAS16	Fairchild
1	D9	TLV431B	Adjustable precision shunt regulator, 0.5%	SOT23	TLV431BQDBZT	TI
1	J1	Vin	Terminal Block, 2-pin, 15-A, 5.1mm	0.40 x 0.35	ED500/2DS	OST
5	J2, J3, J4, J5, J13	131435300	Adaptor, 3.5-mm probe clip (or 131-5031-00)	3.5-mm	131-4353-00	Tektronix
6	J6, J7, J9, J10, J11, J12	Test Pin	Printed Circuit Pin, 0.043 Hole, 0.3 Length	0.043	3103-1-00-15-00-00-08-0	Mill-Max
1	J8	Vo	Terminal Block, 4-pin, 15-A, 5.1mm	0.80 x 0.35	ED500/4DS	OST
1	L1	PA0373	Inductor, 2-uH, 1 pri, 1 sec	0.920x0.78	PA0373	Pulse
1	Q1	IRF6216	MOSFET, P-ch, 150-V, 2.2-A, 240-mOhm	SO8	IRF6216PBF	IR
1	Q2	Si7846DP	MOSFET, N-ch, 150-V, 6.7-A, 50-milliohm	S08	Si7846DP	Vishay
4	Q3, Q4, Q5, Q7	RJK0328DPB	MOSFET, N-ch, 30-V, 60-A, 1.6-milliohm	LFPAK	RJK0328DPB	Renesas
1	Q6	MMBT2222A	Bipolar, NPN, 40-V, 600-mA, 225-mW	SOT23	MMBT2222A	Vishay
1	Q8	ZVN3320F	MOSFET, N-ch, 200-V, 60-mA, 25-ohms	SOT23	ZVN3320F	Zetex

Table 3. UCC2897A Design Example List of Materials (continued)

Count	Ref Des	Value	Description	Size	Part Number	MFR
1	R1	8.45K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R11	26.7K	Resistor, Chip, 1/8W, 1%	0805	std	std
2	R13, R17	2.00K	Resistor, Chip, 1/8W, 1%	0805	std	std
4	R14, R29, R31, R34	0	Resistor, Chip, 1/8W, 1%	0805	Std	Std
1	R18	499	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R19	100K	Resistor, Chip, 1/10W, 1%	0603	std	std
1	R2	69.8K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R21	100K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R22	5.11K	Resistor, Chip, 1/8W, 1%	0805	std	Std
2	R24, R33	10.0K	Resistor, Chip, 1/8W, 1%	0805	std	std
2	R25, R30	51.1	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R26	28.7K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R27	12.1K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R28	4.99K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R3	88.7K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R32	249K	Resistor, Chip, 1/8W, 1%	0805	std	std
0	R35, R36	open	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R37	9.09K	Resistor, Chip, 1/8W, 1%	0805	std	std
6	R4, R10, R15, R16, R20, R23	2.21	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R5	158K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R6	1.82K	Resistor, Chip, 1/8W, 1%	0805	std	std
3	R7, R8, R12	1.00K	Resistor, Chip, 1/8W, 1%	0805	std	std
1	R9	4.64	Resistor, Chip, 1/8W, 1%	0805	std	std
1	T1	P8208	Transformer, Current Sense, 10-A, 1:100	SMD	P8208	Pulse
1	T2	PA0810	Transformer, High Frequency Planar	Planar	PA0810	Pulse
1	U1	UCC2897A	IC, Current-Mode Active Clamp PWM Controller	PW20	UCC2897APW	TI
1	U2	SFH690BT	IC, Phototransistor, CTR 100%-300%	SOP4	SFH690BT	Vishay
1	--		PCB, 3.6 In x 2.7 In x 0.062 In		HPA348	Any
4	--	Bumpon	Rubber bumpon transparent, 0.44"x0.2"	0.44"x0.2"	SJ5303	3M

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.
4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

9 Suggested Design Improvements

Once the design was built and tested, several areas of improvement were noticed and have been noted below. Component reference designations in the following notes refer to the schematic of Figure 29.

9.1 Output Sync Rectifiers

A possible design improvement would be to modify the drive to the output rectifying FETS so that if a voltage is applied to the output when the converter is unpowered the output FETs do not go into self oscillations.

9.2 Overcurrent Shutdown

Add a circuit that will shut the converter down in the event of an extended overcurrent condition. With the present method of powering the primary side control the converter will stay in peak current limit and not power down.

9.3 Component Changes

The EVM for the UCC2897A was released prior to the completion of this exhaustive analysis. As a result there are some changes to component values that could be incorporated to more closely bring the EVM in line with the specification.

10 Conclusion

A step by step design procedure of a 3.3 V, 100 W active clamp forward converter operating in peak CMC has been show. The design example is based upon using the UCC2897A Active Clamp PWM Current Mode controller, however the power stage design procedure is applicable to any low-side active clamp forward converter. The concept of ZVS has been explained as it applies to the active clamp forward topology. The details of the major component losses within the power stage have also been examined.

11 References

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4. Steve Mappus, *UCC2891EVM, 48-V to 1.3-V, 30-A Forward Converter with Active Clamp Reset*, User's Guide to Accommodate UCC2891EVM, (SLUU178)
5. Steve Mappus, *Reference Design PR265A 48V to 3.3V Forward Converter with Active Clamp Reset Using the UCC2897 Active Clamp Current Mode PWM Controller*, (SLUU192)
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