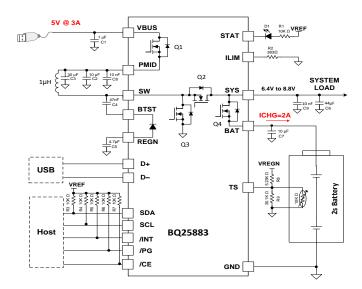
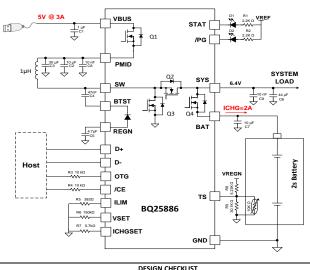


	DESIGN CHECKLIST								
PIN N	AME	REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement
VBUS	A1, B1	Required	C1		1 uF		Input supply	Place C1 as close to the IC as possible	Place C1 as close to the IC as possible
	A2, B2	Required	C2		10 uF		Blocking MOSFET Connection	Boost converter input. The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF.	Place as close to the IC as possible. C2 should have the second highest priority on placement over all components.
PMID		Recommended	C3		30 uF		Slow down voltage drop with high impedance capble during inrush	High resistance cable can cause significant voltage drop with higher inrush current. For optimal performance, an additiional 30 uF cap on PMID is recommended.	
		Optional	C8		10 nF		Optimal EMI performance	Place 0402 10 nF capacitor for high frequency EMI filtering	Place as close to the IC as possible. C8 should higher priority than C2, and C3
BTST	D5	Required	C4		47 nF		PWM high-side driver Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.
REGN	B4	Required	C5		4.7 uF		Gate drive supply	Connect a 4.7 uF cap from REGN to GND	Place as close to the IC as possible. C5 should have higher priority than R1, D1, R2, R7, and R8.
	B5	Required	C6		44 uF		System connection	Boost converter output. Connect at least 2 x 22 uF capacitance after derating closely to the SYS pin and GND	Place as close to the IC as possible.
SYS		Optional	С9		10 nF		Optimal EVM performance	Place 0402 10 nF capacitor from SYS pin to GND	Place as close to the IC as possible. C9 should have the highest piority on placement over all components.
BAT	C4, C5	Required	C7		10 uF		Battery Power connection	Minimum 10 uF capacitance after derating closely to BAT pin and GND	Place as close to the IC as possible.
BATN	E4						Negative battery sense terminal	Kelvin connect as close as possible to negative battery terminal	
BATP	E5						Positive battery sense terminal	Kelvin connect as close as possible to positive battery terminal	
ILIM	D3	Recommended	R2		*Ω		Input current limit resistor programming	IINMAX = KILIM / R2. If ILIM is not used, pull ILIM to ground.	
SDA	E2	Recommended	R2		10 kΩ		I2C interface data		
SCL	D2	Recommended	R4		10 kΩ		I2C interface clock		
/INT	С3	Recommended	R5		10 kΩ		Open drain active Interrupt Output		
/PG	C2	Recommended	R6		*kΩ		Open drain active low power good indicator	Current limiting resistor	
/CE	E1	Recommended	R7		10 kΩ		Active low charge eneable pin	/CE pin is internally pulled low with 900-k Ω resistor	
	E3	Required	R8		*Ω		Resistor network to set window for thermistor	$RT2 = \frac{R_{AVC,T} \times R_{AVC,T} \times \left(\frac{1}{V_{c1}} - \frac{1}{V_{c1}}\right)}{R_{AVC,T} \times \left(\frac{1}{v_{c1}} - 1\right) - R_{AVC,T} \times \left(\frac{1}{v_{c1}} - 1\right)}$	
TS		Required	R9		*Ω		temperature-based battery charging profile	$\begin{split} RT2 &= \frac{R_{way,rr} * R_{way,rr} * \left\{\frac{1}{V_{rr}} - \frac{1}{\Gamma_{rr}}\right\}}{R_{way,rr} * \left\{\frac{1}{V_{rr}} - 1\right\} - R_{way,rr} * \left\{\frac{1}{\Gamma_{rr}} - 1\right\}} \\ RT1 &= \frac{\frac{1}{\Gamma_{rr}} - 1}{\frac{1}{R_{rr}} + 1} - R_{way,rr} * \left\{\frac{1}{\Gamma_{rr}} - 1\right\} \end{split}$	
D+	C1						Positive USB data line		
D-	D1						Negative USB data line		
SW	A4, A5	Required	L		1 uH		Inductor connection	Connect to the swtiched side of the external inductor	
GND	A3, B3						Ground return		



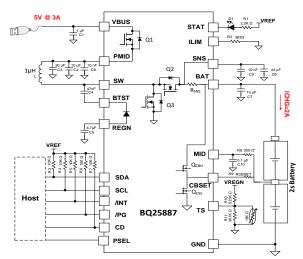
	DESIGN CHECKLIST								
PIN N	AME	REQUIREMENT	COMPONENT	MIN	TYP N	AX DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement	
VBUS	23	Required	C1		1 uF	Input supply		Place C1 as close to the IC as possible	
		Required	C2		10 uF	Blocking MOSFET Connection	Boost converter input. The minimum recommended total input low-ESR capacitance on VBUS and PMID, nominal is 10 uF.	Place as close to the IC as possible. C2 should have the second highest priority on placement over all components.	
PMID	21, 22	Recommended	C3		30 uF	Slow down voltage drop with high impedance capble during inrush	High resistance cable can cause significant voltage drop with higher inrush current. For optimal performance, an additiional 30 uF cap on PMID is recommended.		
		Optional	C8		10 nF	Optimal EMI performance	Place 0402 10 nF capacitor as close to the IC as possible. This cap should have the highest piority on placement.	Place as close to the IC as possible. C8 should higher priority than C2, and C3	
BTST	12	Required	C4		47 nF	PWM high-side driver Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.	
REGN	11	Required	C5		4.7 uF	Gate drive supply	Connect a 4.7 uF cap close to the IC.	Place as close to the IC as possible. C5 should have higher priority than R1, D1, R2, R7, and R8.	
		Required	C6		44 uF	System connection	Boost converter output. Connect at least 2 x 22 uF nominal capacitance closely to the SYS pin and PGND	Place as close to the IC as possible.	
SYS	15, 16	Optional	С9		10 nF	Optimal EVM performance	Place 0402 10 nF capacitor as close to the IC as possible. C9 should be placed closer to IC comparing to C6.	Place as close to the IC as possible. C9 should have the highest piority on placement over all components.	
BAT	13, 14	Required	C7		10 uF	Battery Power connection	Minimum 10 uF nominal capacitance closely to BAT pin and GND	Place as close to the IC as possible.	
STAT	2	Recommended	R1		*kΩ	Charging status indicating LED	Current limiting resistor		
JIAI		Optional	D1			Charging status indicating LED			
ILIM	8	Recommended	R2		*Ω	Input current limit resistor programming	IINMAX = KILIM / R2. If ILIM is not used, pull ILIM to ground.		
SDA	4	Recommended	R2		10 kΩ	I2C interface data			
SCL	5	Recommended	R4		10 kΩ	I2C interface clock			
/INT	6	Recommended	R5		10 kΩ	Open drain active Interrupt Output			
/PG	9	Recommended	R6		*kΩ	Open drain active low power good indicator	Current limiting resistor		
/CE	3	Recommended	R7		10 kΩ	Active low charge eneable pin			
	7	Required	R8		*Ω	Resistor network to set window for thermistor	$RT2 = \frac{R_{NTC,T} \times R_{NTC,T} \times \left[\frac{1}{\nu_{TA}} - \frac{1}{\nu_{TA}}\right]}{R_{NTC,TA} \times \left(\frac{1}{\nu_{TA}} - 1\right) - R_{NTC,TA} \times \left(\frac{1}{\nu_{TA}} - 1\right)}$		
TS		Required	R9		*Ω	temperature-based battery charging profile	$RT2 = \frac{R_{SVCFF} \times R_{SVCFF} \times \left[\frac{1}{V_{FT}} - \frac{1}{V_{FT}}\right]}{R_{SVCFF} \times \left[\frac{1}{V_{FT}} - 1\right] - R_{SVCFF} \times \left[\frac{1}{V_{FT}} - 1\right]}$ $RT1 = \frac{\frac{1}{V_{FT}} - 1}{\frac{1}{V_{FT}} + \frac{1}{R_{SVCFF}}}$		
D+	24					Positive USB data line			
D-	1					Negative USB data line			
SW	17, 18	Required	L		1 uH	Inductor connection	Connect to the swtiched side of the external inductor		
GND	19, 20					Ground return			
PwrPad	-					IC Thermal dissipation pad	http://www.ti.com/lit/an/snva183b/snva183b.pdf	Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers for heat sink. Recommended to follow EVM design.	

BQ25886 Schematic



	DESIGN CHECKLIST								
PIN N		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement
VBUS	23	Required	C1		1 uF		Input supply		Place C1 as close to the IC as possible
		Required					Blocking MOSFET	Boost converter input. The minimum recommended total input low-ESR	
			C2		10 uF		Connection	capacitance on	the second highest priority on placement over all
								VBUS and PMID, after applied derating, is 10 uF.	components.
PMID	21, 22						Slow down voltage drop	High resistance cable can cause significant voltage drop with higher	
		Recommended	C3		30 uF		with high impedance	inrush current. For optimal performance, an additiional 30 uF cap on	
							capble during inrush	PMID is recommended.	Discourse days to the IC or provible. CO should bish as
		Optional	C8		10 nF		Optimal EMI performance	Place 0402 10 nF capacitor as close to the IC as possible. This cap should have the highest piority on placement.	Place as close to the IC as possible. C8 should higher priority than C2, and C3
							PWM high-side driver		
BTST	12	Required	C4		47 nF		Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.
							Supply		
REGN	11	Required	C5		4.7 uF		Gate drive supply	Connect a 4.7 uF cap close to the IC.	Place as close to the IC as possible. C5 should have
									higher priority than R1, D1, R2, R7, and R8.
		Descripted	C6		44 uF		6	Boost converter output. Connect at least 2 x 22 uF capacitance after	Discourse data to the IC or monihile
		Required	6		44 UF		System connection	derating closely to the SYS pin and PGND	Place as close to the IC as possible.
SYS	15, 16						Optimal EVM performance	Place 0402 10 nF capacitor as close to the IC as possible. C9 should be	Place as close to the IC as possible. C9 should have
		Optional	C9		10 nF			Place 0402 10 nF capacitor as close to the IC as possible. C9 should be placed closer to IC comparing to C6.	the highest piority on placement over all
								F	components.
BAT	13, 14	Required	C7		10 uF		Battery Power connection	Minimum 10 uF capacitance after derating closely to BAT pin and GND	Place as close to the IC as possible.
							Chausing status indicating		
		Recommended	R1		*kΩ		Charging status indicating LED	Current limiting resistor	
STAT	2						Charging status indicating		
		Optional	D1				LED		
	9 -				*1.0		VBUS power good status		
/PG		Recommended	R2		*kΩ		indicating LED	Current limiting resistor	
/PG		Optional	D2				VBUS power good status		
		Optional	DZ				indicating LED		
OTG	5	Recommended	R3		10 kΩ		Active high OTG enable nin	Pull OTG pin high to enable OTG function	
	-		-		-				
/CE	3	Recommended	R4		10 kΩ		Active low charge eneable	/CE pin is internally pulled low with 900-k Ω resistor	
							pin Input current limit resistor	IINMAX = KILIM / R5. If ILIM is not used, pull ILIM to ground to set the	
ILIM	8	Recommended	R5		*Ω			input current limit to maximum.	
							programming	RVSET< 18k Ω (short to GND) = 8.2 V	
	_	Recommended	commended R6				Battery charge voltage	$RVSET = 39k\Omega (\pm 10\%) = 8.8 V$	
VSET	6				*kΩ		limit	RVSET= $75k\Omega (\pm 10\%) = 8.7 V$	
								RVSET> $150k\Omega$ (floating) = 8.4 V	
								ICHG=RICHGSET/KICHGSET. Precharge and termination current is 1/10	
ICHGSET	10	Recommended	R7		*Ω		Battery charge voltage	of the fasst charge current. Shorting ICHGSET to GND clamps the	
ICHOSET	10	Recommended			32		limit	charge current to 30mA (typ). Floating ICHGSET to GND changes the	
		Required	R8		*Ω		Resistor network to set	$\begin{split} RT2 &= \frac{R_{SW(r)} * R_{SW(r)} * \left(\frac{1}{V_{rr}} - \frac{1}{1} \frac{1}{V_{rr}}\right)}{R_{SW(r)} * \left(\frac{1}{V_{rr}} - 1\right) - R_{SW(r)} * \left(\frac{1}{V_{rr}} - 1\right)} \\ RT1 &= \frac{\frac{1}{V_{rr}} - 1}{\frac{1}{K_{rr}} + \frac{1}{R_{SW(r)}}} \end{split}$	
TS	7						window for thermistor	$R_{_{NTC,T1}} \times \left(\frac{1}{V_{_{T1}}} - 1\right) - R_{_{NTC,T3}} \times \left(\frac{1}{V_{_{T3}}} - 1\right)$	
		Required	R9		*Ω		temperature-based	$\frac{1}{V_{21}} - 1$	
							battery charging profile	$\frac{1}{R_{T_2}} + \frac{1}{R_{NTC,T_1}}$	
D+	24						Positive USB data line		
D-	1						Negative USB data line		
SW	17, 18	Required	L		1 uH		Inductor connection	Connect to the swtiched side of the external inductor	
GND	4, 19, 20						Ground return		
-	,,0								
PwrPad									Ensure that there are sufficient thermal vias directly
							IC Thermal dissipation pad	http://www.ti.com/lit/an/snva183b/snva183b.pdf	under the IC, connecting to the ground plane on the other layers for heat sink. Recommended to follow
									other layers for heat sink. Recommended to follow EVM design
L	-								LVIVI GCSIBII

BQ25887 Schematic



	DESIGN CHECKLIST							
PIN NAME		REQUIREMENT	COMPONENT	MIN		MAX DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	PCB Placement
VBUS	23	Required Required	C1 C2		1 uF 10 uF	Input supply Blocking MOSFET Connection	Boost converter input. The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF.	Place C1 as close to the IC as possible Place as close to the IC as possible. C2 should have the second highest priority on placement over all components.
PMID	21, 22	Recommended	C3		30 uF	Slow down voltage drop with high impedance capble during inrush	High resistance cable can cause significant voltage drop with higher inrush current. For optimal performance, an additiional 30 uF cap on PMID is recommended.	
		Optional	C8		10 nF	Optimal EMI performanc	Place 0402 10 nF capacitor as close to the IC as possible. This cap should have the highest piority on placement.	Place as close to the IC as possible. C8 should higher priority than C2, and C3
BTST	12	Required	C4		47 nF	PWM high-side driver Supply	Connect a 47 nF bootstrap capacitor from SW to BTST	BTST to SW path should be as short as possible.
REGN	11	Required	C5		4.7 uF	Gate drive supply	Connect a 4.7 uF cap close to the IC.	Place as close to the IC as possible. C5 should have higher priority than R1, D1, R2, R7, and R8.
0.45		Required	C6		44 uF	System connection	Boost converter output. Connect at least 2 x 22 uF capacitance after derating closely to the SYS pin and PGND	Place as close to the IC as possible.
SYS	15, 16	Optional	С9		10 nF	Optimal EVM performan	e Place 0402 10 nF capacitor as close to the IC as possible. C9 should be placed closer to IC comparing to C6.	Place as close to the IC as possible. C9 should have the highest piority on placement over all components.
BAT	13, 14	Required	C7		10 uF	Battery Power connectio		Place as close to the IC as possible.
STAT	2	Recommended	R1		*kΩ	Charging status indicating LED		
5.7.1		Optional	D1			Charging status indicating LED	3	
ILIM	8	Recommended	R2		*Ω	programming	r IINMAX = KILIM / R2. If ILIM is not used, pull ILIM to ground to set the input current limit to maximum.	
SDA	4	Recommended	R3		10 kΩ	I2C interface data		
SCL	5	Recommended	R4		10 kΩ	I2C interface clock		
/INT	6	Recommended	R5		10 kΩ	Open drain active Interrupt Output		
/PG	1	Recommended	R6		*kΩ	VBUS power good status indicating LED	Current limiting resistor	
CD	3	Recommended	R7		10 kΩ	Active high chip disable	Pull CD low to enable the IC. Pull CD high to disable the IC.	
MID	9	Optional	R8		300 Ω	Voltage sense input for mid point between cells i 2S1P configuration	$\ensuremath{300-\Omega}$ resistor is used to limit the current in the case where the bottom cell is plugged in reversely	
		Optional	C10		0.1 uF	VBUS power good status indicating LED	Noise filtering for the mid voltage sense	
CBSET	10	Required	R9		*Ω	Cell balancing current pa	Connect CBSET to the mid point between the two cells with a current h limit resistor. The maxiumu cell balancing current can be calculated as ICB_MAX = VCELLREG/R9.	
	7	Required	R10		*Ω	Resistor network to set window for thermistor	$RT2 = \frac{R_{ATC,T} \times R_{ATC,T} \times \left[\frac{1}{P_{eT}} - \frac{1}{T_{eT}}\right]}{R_{ATC,T} \times \left[\frac{1}{P_{eT}} - \frac{1}{T_{eT}} - R_{ATC,T} \times \left[\frac{1}{T_{eT}} - 1\right]\right]}$	
TS		Required	R11		*Ω	temperature-based battery charging profile	$RTI = \frac{\frac{1}{F_{r_1}} - 1}{\frac{1}{R_{r_2}} + \frac{1}{R_{SCT}}}$	
PSEL	24					Power source selection p	in HIGH = 500mA; LOW=3A	
SW	17, 18	Required	L		1 uH	Inductor connection	Connect to the swtiched side of the external inductor	
GND	4, 19, 20					Ground return		
PwrPad	-					IC Thermal dissipation pa	d http://www.ti.com/lit/an/snva183b/snva183b.pdf	Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers for heat sink. Recommended to follow EVM design.