Optimal Buck Converter Output Filter Design for Point-of-Load Applications

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***Abstract*—This paper presents a novel method to design the output filter of low-voltage/high-current buck dc–dc switching regulators. The method is based on the concept of acceptability boundary curves (ABCs). ABCs are the curves bounding the regions in the space of parameters, including commercial components which ensure an acceptable output voltage ripple and a load-transient surge based on design specifications. ABCs help in quickly finding tradeoff design solutions, as well as in a better understanding of the functional correlations among power components. Examples regarding buck converters for point-of-load applications are discussed to highlight the flexibility and reliability of the ABC-based design method. Experimental measurements confirm the analytical results and numerical predictions.**

***Index Terms*—DC/DC converter design, point of load (POL), power supplies, voltage regulator module.**

I. Introduction

THE RAPID advancement of processor devices technology has posed stringent challenges to the design of low-voltage/high-current step-down power supplies dedicated to devices like microprocessor, digital signal processors, and field programmable gate arrays [1]–[5]. A number of constraints must be considered for the output filter design in these applications. An output voltage must comply with a *maximum ripple constraint* $\Delta V_{\rm opp} < \Delta V_{\rm opp\_max}$ at steady state, where $\Delta V_{\rm opp}$ is the peak-to-peak ripple, and a *load-transient constraint* $V_o \in [V_o - \Delta V_{\rm oreg}, V_o + \Delta V_{\rm oreg}]$ during load transients, where V_o is the nominal required voltage and $\Delta V_{\rm oreg}$ is the maximum allowed surge magnitude. Compliance with such specifications depends on output filter parameters, as well as on the controller's characteristics. Dynamic performance, efficiency, and cost also depend upon output filter components, and a designer often wishes to find a good compromise of these figures of merit among different design solutions [6]–[8]. One pressing issue is the dynamic voltage regulation during fast load transients, where load-current slew rate is much higher than the average output inductor current slope. The difference between inductor and load currents causes unbalanced charge that needs to be sourced/sunk by an output capacitor. Consequently, a capacitor current shows a pulse that may strongly affect the output voltage, depending on the equivalent series resistance (ESR) and capacitance C of the component. If the output voltage deviates more than a few percent or even a few tens of millivolts from the nominal value due to step load-current change, proper load operation is not guaranteed.

Many studies have been devoted to find ways to minimize the output capacitor's size required to limit the effects of fast load variations. Different approaches have been adopted. A first one consists in modifying the basic buck converter topology, by means of additional circuitry or special devices [9]–[12]. Such kind of solution requires more components and a more complicated control circuit. A second approach consists in adopting special control techniques [13], including digital control one [14], [15], which require a deep knowledge of the problems and a high-level skill to achieve optimal results. Many other special design solutions are presented in literature, which can give good results in minimizing the output capacitors, at a price of some circuit complication and additional components whose cost may balance, and even overcome, the benefit of reduced output capacitor size. Moreover, in most cases, methods relying on new topologies and/or control techniques do not provide general practical design rules for determining the limit values for ESR, L, and C parameters of output filter components complying with the load-transient specifications. Most of the power supply designers look for cheap, reliable, and quick-to-design regulators. This is true particularly for point-of-load (POL) applications with an output current of up to 20 A, where multiphase architectures and digital control are preferentially avoided. In these applications, simple single-phase voltage-mode- or peak-current-mode-controlled synchronous buck converters are the preferred choice. An example of a different design approach to solve load-transient issues by means of engineering insight, rather than by means of topological and/or control changes, is given in [16], where a relationship between control bandwidth and inductance of output inductor in a buck converter is discussed. Such an approach allows one to determine the critical inductance value as a function of feedback control, step current magnitude, and steady-state operating point and provides a practical design tool and an opportunity to understand the load-transient issues at the same time. A critical inductance approach provides a guideline to find the minimum capacitances, minimum inductances, and maximum ESR of components of output filter. Unfortunately, as in other design formulas suggested in literature, boundary conditions are formulated separately for different parameters of the same component (e.g., the capacitors' C and ESR). This may yield a selection of oversized commercial components. In fact, a drawback is caused by the practice based on taking the minimum ESR and maximum capacitance between values provided by an output voltage ripple and load-transient

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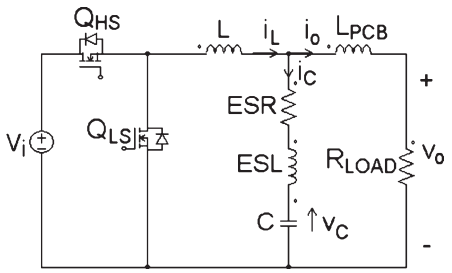


Fig. 1. Buck-SR converter.

voltage over/undershoot constraints: Theoretical solutions may not match with any device in the space of commercial components, so that some oversizing (bigger capacitance and/or smaller ESR) of the selected commercial output capacitor is necessary. To avoid this, adequate parametric models of devices and adequate parametric design equations can be used to figure out a set of possible design solutions, each one corresponding to a given set of commercial components and offering a possible tradeoff in terms of cost, size, efficiency, power density, and other features.

The main goal of this paper is to discuss a design approach, based on a set of acceptability boundary curves (ABCs), which provide a designer with a straightforward, clear, and reliable tool to explore the space of solutions that can be realized by means of commercial components. ABCs, including both ripple and load-transient constraints, allow one to identify the combinations of capacitors and inductors, ensuring the overall minimization of passive components. In Section II, a steady-state ripple analysis is presented, and the ABC concept is introduced. Section III discusses the load-transient analysis. In Section IV, the unified boundary curve (UBC) concept is introduced by means of some design examples. Section V is devoted to the application of ABC concept to some POL converter design problems: Comparisons among analysis, simulations, and experimental measurements are provided. The discussion of the design method presented in this paper is supported by a reference example regarding a buck converter complying with the following operation conditions: $V_i = 3.3$ V, $V_o = 1.1$ V, $D = 0.33$, $I_o = 8$ A, $\Delta I_{o\max} = 7.2$ A, $\Delta V_{\rm oreg} = 55$ mV, $\Delta V_{\rm oacc} = 11$ mV, $\eta > 85\%$, and $f_s = 530$ kHz. $\Delta V_{\rm oreg}$ and $\Delta V_{\rm oacc}$ represent the maximum allowed surge magnitude and the dc error, respectively.

II. Steady-State Ripple Analysis

Fig. 1 shows a synchronous rectification (SR) buck converter, including parasitic inductances in the output branches.

Given the inductor ripple current amplitude $\Delta i_{\rm Lpp}$, the following provides the current flowing into the output capacitor

$$i_C(t) = \begin{cases} -\frac{\Delta i_{\rm Lpp}}{2} + \frac{\Delta i_{\rm LPP}}{DT_s}t, & t \in [0, DT_s] \\ \frac{\Delta i_{\rm Lpp}}{2} - \frac{\Delta i_{\rm LPP}}{D'T_s}(t - DT_s), & t \in [DT_s, T_s] \end{cases} \quad (1)$$

where $T_s = 1/f_s$ is the switching period, D is the duty cycle of the high-side FET, and $D' = 1-D$. Depending on the resistance ESR and capacitance C of the output capacitor,

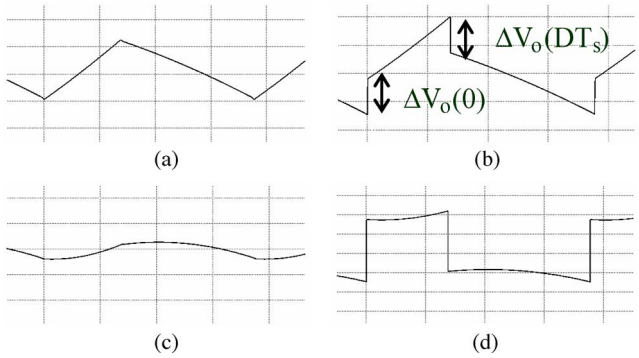


Fig. 2. Output voltage ripple. (a) High $ESR \cdot C$ cap without stray inductances. (b) High $ESR \cdot C$ cap with stray inductances. (c) Low $ESR \cdot C$ cap without stray inductances. (d) Low $ESR \cdot C$ cap with stray inductances.

the output voltage waveform can change from quasi-triangular to quasi-sinusoidal, as shown in Fig. 2. The effect of stray inductances can be easily separated from the effect of the principal parameters ESR and C of the capacitor. In fact, stray inductances produce additive step-up and step-down effects on the output voltage, whose amplitude is given by

$$\Delta V_o(0) = -\Delta V_o(DT_s) \cong (ESL + L_{\rm PCB})\frac{V_i}{L}. \quad (2)$$

The remaining part of the peak-to-peak output ripple voltage can be determined by analyzing the circuit in the time intervals between switching instants. In particular, the output voltage can be derived by integrating (1)

$$\nu_o(t) = \begin{cases} ESR\, i_C + \nu_C(0) + \frac{1}{C}\cdot\int_0^t i_C(\tau)d\tau, & t \in [0, DT_s] \\ ESR\, i_C + \nu_C(DT_s) + \frac{1}{C}\cdot\int_{DT_s}^t i_C(\tau)d\tau, & t \in [DT_s, T_s] \end{cases} \quad (3)$$

where

$$\nu_C(0) = V_o - \frac{1}{12 f_s C}\Delta i_{\rm Lpp}(1-2D) \quad (4)$$

$$\nu_C(DT_s) = \nu_C(0) + \frac{1}{C}\int_0^{DT_s} i_C(\tau)\, d\tau. \quad (5)$$

Equation (3) supposes $ESL = L_{\rm PCB} = 0$; their contribution will be taken into account at the end of this section.

In order to determine an analytical expression of the output voltage ripple, the maximum and minimum values of output voltage waveform must be computed using (3). The instant at which the minimum value occurs is

$$t_{\min} = \begin{cases} -C \cdot ESR + \tau_s, & \text{if } C \cdot ESR < \tau_s \\ 0, & \text{if } C \cdot ESR \geq \tau_s \end{cases} \quad (6)$$

whereas the instant at which the maximum value occurs is

$$t_{\max} = \begin{cases} -C \cdot ESR + \tau_s', & \text{if } C \cdot ESR < \tau_s' \\ 2\tau_s, & \text{if } C \cdot ESR \geq \tau_s' \end{cases} \quad (7)$$

TABLE I
EXPRESSIONS FOR PEAK-TO-PEAK OUTPUT VOLTAGE RIPPLE ΔV_{opp} AND FOR MAXIMUM ALLOWED ESR: $D < 0.5$

D<0.5		
	ΔV_{opp}	$ESR_{\max}$
$ESR \cdot C > \tau_s'$	$ESR \Delta i_{Lpp}$	$ESR_H = \frac{\Delta V_{opp\,\max}}{\Delta i_{Lpp}} = R_{pp}$
$\tau_s < ESR \cdot C < \tau_s'$	$\frac{\Delta i_{Lpp}(D'+2ESR f_s C)^2}{8 f_s C D'}$	$ESR_M = \frac{1}{2 f_s C}\left[\sqrt{D' 8 R_{pp} f_s C} - D'\right]$
$ESR \cdot C < \tau_s$	$\frac{\Delta i_{Lpp}(DD'+4ESR^2 f_s^2 C^2)}{8 f_s C DD'}$	$ESR_L = \frac{1}{2 f_s C}\sqrt{D' D(8 R_{pp} f_s C - 1)}$

TABLE II
EXPRESSIONS FOR PEAK-TO-PEAK OUTPUT VOLTAGE RIPPLE ΔV_{opp} AND FOR MAXIMUM ALLOWED ESR: $D > 0.5$

D>0.5		
	ΔV_{opp}	$ESR_{\max}$
$ESR \cdot C > \tau_s$	$ESR \Delta i_{Lpp}$	$ESR_H = \frac{\Delta V_{opp\,\max}}{\Delta i_{Lpp}} = R_{pp}$
$\tau_s' < ESR \cdot C < \tau_s$	$\frac{\Delta i_{Lpp}(D+2ESR f_s C)^2}{8 f_s C D}$	$ESR_M = \frac{1}{2 f_s C}\left[\sqrt{D 8 R_{pp} f_s C} - D\right]$
$ESR \cdot C < \tau_s'$	$\frac{\Delta i_{Lpp}(DD'+4ESR^2 f_s^2 C^2)}{8 f_s C DD'}$	$ESR_L = \frac{1}{2 f_s C}\sqrt{D' D(8 R_{pp} f_s C - 1)}$

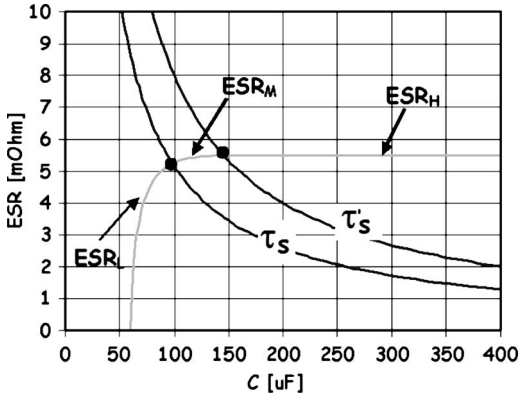
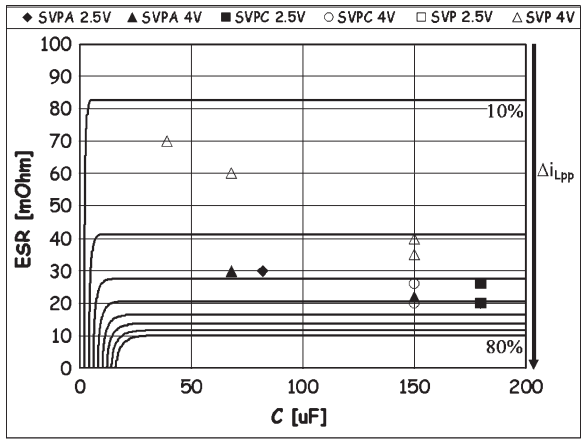


Fig. 3. ABC plots.



D<0.5

Fig. 4. ABC plotted for Δi_{Lpp} from (upper curves) 10% to (lower curves) 80% of I_o, together with the data points of OS-CON capacitors ($D < 0.5$).

where

$$\tau_s = \frac{D}{2 f_s} \tag{8}$$

$$\tau_s' = \frac{D'}{2 f_s}. \tag{9}$$

The functions (8) and (9) bound three regions in the ESR–C plane. According to (6)–(9), the peak-to-peak output voltage ripple $\Delta \nu_{\mathrm{opp}}$ as a function of ESR and C and the maximum allowed ESR as a function of peak-to-peak ripple $\Delta \nu_{\mathrm{opp}}$ and C can be calculated within each region: results are given in Tables I and II.

Fig. 3 shows the plots of $ESR_{\max}$ in the ESR–C plane according to Table II for $D < 0.5$ and $\Delta i_{\mathrm{Lpp}} = 50\%$ of I_o. A similar plot can be obtained for $D > 0.5$. The resulting curve represents the ABC bounding the couples $\{ESR, C\}$ which ensure the operation of the converter complying with the given constraints regarding ΔV_{opp} at the operated f_s and D.

The ABC allows one to figure out *real* feasible capacitors representing possible design solutions quickly. In fact, the data couples $\{ESR, C\}$ of the commercial capacitors of interest (selected according to voltage and current ratings, electrolytic/ceramic type, surface/lead mount, size, cost, and other technical/commercial issues) can be plotted together with the ABCs for different values of Δi_{Lpp}. For example, Fig. 4 shows the data points of some organic semiconductor (OS-CON) capacitors, with a voltage rating adequate for the reference application under study, plotted together with ABCs for Δi_{Lpp} from 10% to 80% of the average output load current I_o. A capacitor is acceptable for a certain ripple current Δi_{Lpp} if its

ESR and C correspond to a point lying below the ABC related to that ripple current Δi_{Lpp}.

The ABC can be used for a straightforward selection of the smallest capacitor complying with the design specifications regarding the operating parameters $\{V_i, V_o, I_o, f_s\}$ and the maximum output voltage ripple $\Delta\nu_{\mathrm{opp\,max}}$, for any given inductor current ripple $\Delta i_{\mathrm{Lpp}} \in [\Delta i_{\mathrm{Lpp\,min}}, \Delta i_{\mathrm{Lpp\,max}}]$. Given the set of commercial capacitors of interest ordered by increasing capacitance, the following procedure can be used for any Δi_{Lpp} from $\Delta i_{\mathrm{Lpp\,min}}$ to $\Delta i_{\mathrm{Lpp\,max}}$.

1) Pick the smallest capacitor in the set.
2) Calculate the time constant $ESR \cdot C$ of the capacitor.
3) Calculate the maximum value $ESR_{\max}$ allowed for the capacitor, depending on its capacitance C, according to Table I or Table II (depending on the D value).
4) If the ESR of the capacitor is smaller than $ESR_{\max}$, then stop the search; otherwise, pick the next capacitor, and go to step 2).

The effect determined by the equivalent series inductance (ESL) of the output capacitor and by the inductance of the printed circuit board trace L_{PCB} can be easily accounted for in the previous procedure. It is sufficient to replace the maximum allowed peak-to-peak output ripple voltage amplitude $\Delta V_{\mathrm{opp\,max}}$ with the net effective peak-to-peak ripple voltage $\Delta V_{\mathrm{oppeff}}$ allowed to ESR and capacitance C, given by

$$\Delta V_{\mathrm{oppeff}} = \Delta V_{\mathrm{opp\,max}} - (ESL + L_{\mathrm{PCB}})\frac{V_i}{L}. \qquad (10)$$

If ESL and L_{PCB} are unknown, (10) can also be used to determine the maximum allowed ESL compatible with the ESR and capacitance C of a capacitor selected with the algorithm not including the L_{esl}:

$$ESL_{\max} = \frac{L}{V_i}[\Delta V_{\mathrm{opp\,max}} - \Delta V_{\mathrm{oppeff}}]. \qquad (11)$$

The procedure presented earlier allows a quick and reliable detection of the best combination for inductor[1] and capacitor, which guarantees the required output voltage ripple with the smallest size of components, without resorting to complex—whether stochastic or not—numerical techniques. In the next section, load-transient constraint and relevant ABCs will be discussed.

III. Load Transients in a Buck Converter

In applications where tight output voltage regulation is required in the presence of load transients, particular attention must be paid to the output filter component selection. Three different cases can be considered.

1) *Stepwise load transient*. Load-transient duration T_{LT} is *much smaller* than the closed-loop system's time response, expressed by means of the crossover frequency f_c : $T_{\mathrm{LT}} \ll 1/(4f_c)$.

[1]The output inductor's inductance L is univocally determined by the output inductor's current ripple by means of the following relation: $L = V_o D'/\Delta i_{\mathrm{Lpp}} f_s$.

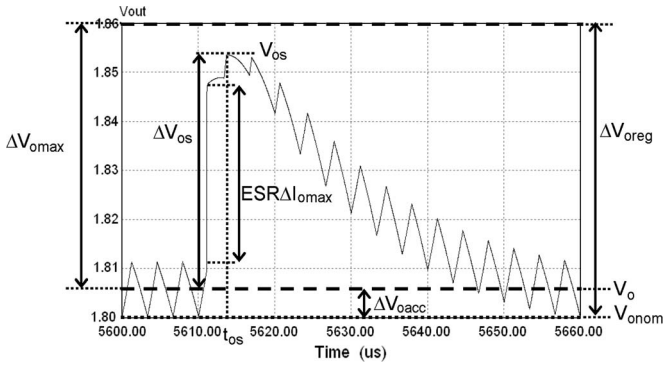


Fig. 5. Output voltage with overshoot.

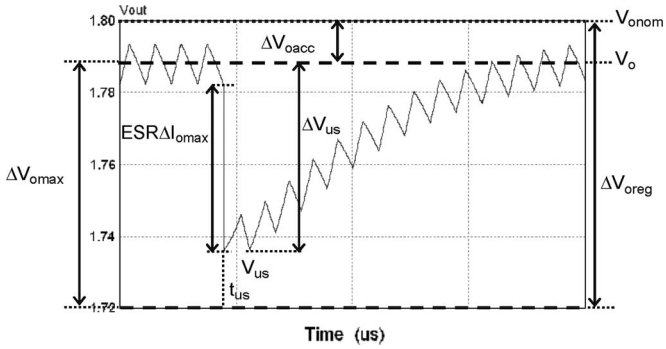


Fig. 6. Output voltage with undershoot.

2) *Fast load transient*. Load-transient duration T_{LT} is *smaller* than the closed-loop system's time response: $T_{\mathrm{LT}} < 1/(4f_c)$.
3) *Slow load transient*. Load-transient duration T_{LT} is *larger* than the closed-loop system's time response: $T_{\mathrm{LT}} > 1/(4f_c)$.

In cases 1) and 2), the control network is not able to start compensating the output voltage variations suddenly after load variations. Then, the output filter must be designed to keep the output voltage within the maximum required range in an early time after load transient. In case 3), the dynamic action of control network is fast enough to quickly compensate for load variations. The impact of load-transient constraint on the output capacitor size is, in this case, lower than in the previous ones. For this reason, in this paper, worst case stepwise load transient is treated. The output current slew rate will be considered as infinite ($T_{\mathrm{LT}} = 0$): This is a reasonable assumption in applications such as FPGA supplies, where the load-current slew rate may range up to 100 A/μs. When a sudden load change occurs, the output voltage exhibits a very fast variation followed by a positive (overshoot) or negative (undershoot) surge. Figs. 5 and 6 show the output voltage waveforms with an overshoot and an undershoot, respectively. The maximum allowed variation for the output voltage during load transient is $\Delta V_{o\,\max} = \Delta V_{\mathrm{oreg}} - \Delta V_{\mathrm{oacc}}$.

Design specifications usually provide a limit for window regulation amplitude ΔV_{oreg}, wherein over- and undervoltage surges must be contained. These perturbations are limited by the joint action of the output capacitor and the feedback control: the former limits the initial overshoot/undershoot caused by a

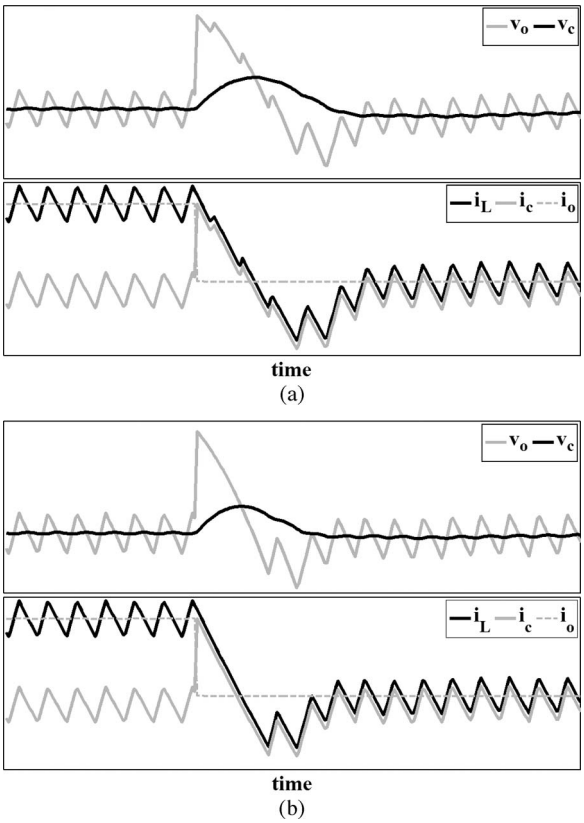


Fig. 7. Load variation from maximum to minimum current. (a) No saturated PWM. (b) Saturated PWM.

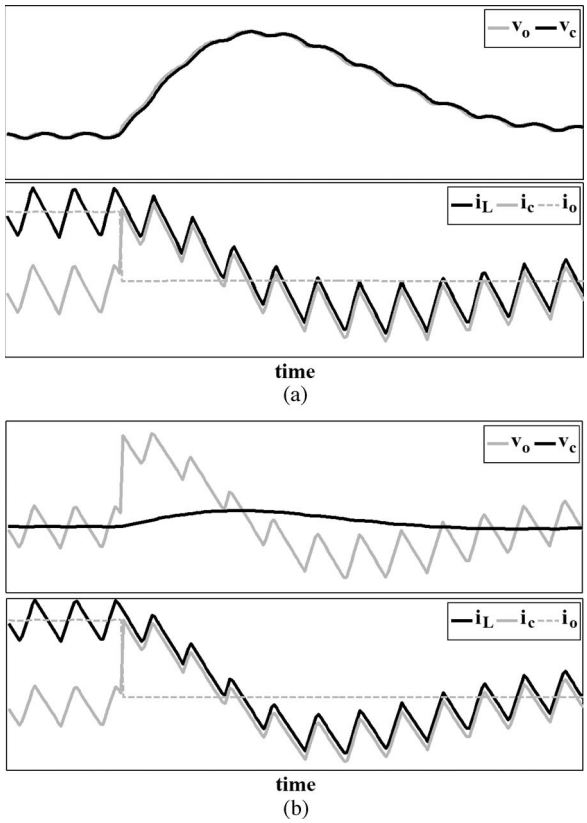


Fig. 8. Load variation from maximum to minimum current. (a) Ceramic capacitor. (b) Electrolytic capacitor.

sudden change in load current, whereas the controller behavior depends on the control circuit being used.

Two different cases may occur: If the controller is designed to achieve a very high crossover frequency, the compensation network produces sharp and wide variations of control signal at the pulsewidth modulation (PWM) modulator input terminals, when a sudden variation of the output voltage is triggered by the load transient. If the PWM modulator input is saturated (the control is signal greater than the peak value of the modulator's ramp), the duty cycle is locked either to one or zero over one or more switching cycles, if the load varies from minimum to maximum or from maximum to minimum, respectively. This allows to limit the overshoot and undershoot surges, and the time required for the output voltage is regulated to its nominal value. If the controller is designed for low crossover frequency, the PWM modulator is not saturated, the duty cycle is not locked, and no switching cycle is skipped by the modulator.

Fig. 7 shows the waveforms of the output capacitor voltage and the output inductor current load transients in the case of (a) low and (b) high crossover frequencies, respectively. In the following, a controller with a high crossover frequency will be considered.

A second important element which influences the output voltage during load transients is the type of the output capacitor. Fig. 8 shows the output voltage of a buck-SR converter during a step-down load transient with ceramic and electrolytic capacitors.

The plots clearly show that the peak overshoot is reached when the capacitor's current crosses zero for the ceramic capacitor, whereas it is reached earlier if an electrolytic capacitor is used. The exact point where the peak overshoot is reached, and its magnitude, must be calculated by taking into account the joint influence of the capacitor's capacitance and ESR, like in the case of the step-up load transients.

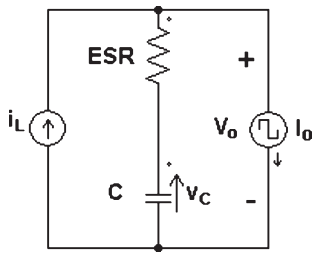


Fig. 9. Load-transient equivalent circuit.

During a load transient, the buck converter's output capacitor behavior can be analyzed by means of the simplified circuit shown in Fig. 9, in which the stray inductances are initially neglected.

The output capacitor design accounting for voltage surges within a regulation window during load transients must be done in the worst case conditions, occurring at DT_s for step-down load transient and at T_s for step-up load transient. This is proved by considering the capacitor's current and output voltage within the time intervals $[0, DT_s]$ and $[DT_s, T_s]$ as in (1)–(4).

If a charging (step-down) load transient occurs at t_{LT} [the same analysis can be performed for a discharging (step-up) load

transient], then the capacitor's current and output voltage are given by

$\underline{0 < t_{\rm LT} < {\rm DT}_s}$

$$i_C(t) = -\frac{\Delta i_{\rm Lpp}}{2} + \Delta I_{o\max} + \frac{\Delta i_{\rm Lpp} f_s}{D'}\left(\frac{t_{\rm LT}}{D} - t\right) \quad (12)$$

$$v_o(t) = V_o - \frac{\Delta i_{\rm Lpp}}{12C}\left(\frac{(1-2D)}{f_s} + 6t_{\rm LT}\left(1 - \frac{f_s t_{\rm LT}}{D}\right)\right) + ESR\, i_C(t) + \frac{1}{C}\int_{t_{\rm LT}}^{t} i_C(\tau)d\tau \quad (13)$$

$\underline{DT_s < t_{\rm LT} < T_s}$

$$i_C(t) = \frac{\Delta i_{\rm Lpp}}{2} + \Delta I_{o\max} + \frac{\Delta i_{\rm Lpp}}{D'}\cdot(D - f_s t) \quad (14)$$

$$v_o(t) = V_o - \frac{\Delta i_{\rm Lpp}}{2C}\left(\frac{1}{6D' f_s}(3D + 2D^2 + 1) - \left(1 + \frac{2D}{D'}\right)t_{\rm LT} - \frac{t_{\rm LT}^2 f_s}{D'}\right) + ESR\, i_C(t) + \frac{1}{C}\int_{t_{\rm LT}}^{t} i_C(\tau)d\tau. \quad (15)$$

If $0 < t_{\rm LT} < DT_s$, then the overshoot peak is located at instant

$$t_{\rm os} = \frac{D'}{f_s}\left(\frac{1}{r} - \frac{1}{2}\right) - ESRC + \frac{t_{\rm LT}}{D} \quad (16)$$

and its value is given by (16)

$$V_o(t_{\rm os}) = V_o + \frac{\Delta I_{o\max}}{2f_s CD'r} \times \left[D^2\left(1 - \frac{1}{12}r^2\right) - {\rm r}\left(1 - \frac{1}{12}r\right) + (1-2D) + rD(2-D) + (ESRf_sCr)^2 + rf_s\left(r + 2(D-2) + \frac{1}{D}(2-r)\right)t_{\rm LT} + r^2 f_s^2 \frac{D'}{D^2}t_{\rm LT}^2\right]. \quad (17)$$

The derivative of (16) is given in (17)

$$\frac{dV_o(t_{\rm os})}{dt_{\rm LT}} = \frac{\Delta I_{o\max}}{CD'} \times \left(\frac{1}{2}\left(r + 2(D-2) + \frac{1}{D}(2-r)\right) + rf_s\frac{D'}{D^2}t_{\rm LT}\right) \quad (18)$$

where

$$r = \frac{\Delta i_{\rm Lpp}}{\Delta I_{o\max}}. \quad (19)$$

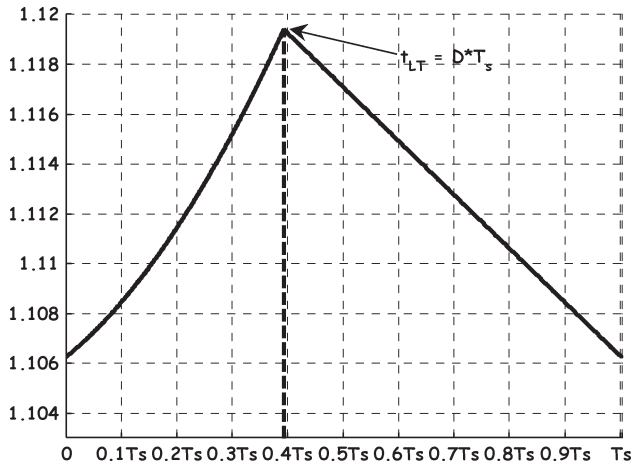


Fig. 10. $V_{\rm os}$ versus $t_{\rm LT}$.

It can be easily found that the derivative given in (18) is always positive. If $DT_s < t_{\rm LT} < T_s$, then the overshoot peak is located at instant

$$t_{\rm os} = \frac{1}{f_s}\left(\frac{(1+D)}{2} + \frac{D'}{r}\right) - ESRC \quad (20)$$

and its value is given by

$$V_o(t_{\rm os}) = V_o + \frac{\Delta I_{o\max}}{2f_s rD'C}\left[r(1-D^2)\left(1 + \frac{1}{12}r\right) - D'^2 + (ESR\, f_s rC)^2 - 2f_s rD' t_{\rm LT}\right]. \quad (21)$$

The derivative of (20) is

$$\frac{dV_o(t_{\rm os})}{dt_{\rm LT}} = -\frac{\Delta I_{o\max}}{C}. \quad (22)$$

According to (18) and (22), the worst case output voltage overshoot $V_{\rm os}(t_{\rm LT})$ corresponds to $t_{\rm LT} = DT_s$. For example, Fig. 10 shows the plot of $V_{\rm os}(t_{\rm LT})$ for $ESR = 0.5$ mΩ and $C = 500$ μF.

Assuming that a step-down load transient occurs at $t_{\rm LT} = DT_s$, the instant at which the output voltage reaches its peak and the amplitude of such a peak are

$$t_{\rm os} = T_s\left(\frac{1}{2}(1+D) + \frac{D'}{r}\right) - ESRC \quad (23)$$

$$V_{o\,{\rm os\,max}} = V_o + \frac{\Delta I_{o\max}}{f_s CD'r}\left[D'^2(1+r) + \frac{1}{12}r^2(1-D^2) + (ESR\, r f_s C)^2\right]. \quad (24)$$

The peak output voltage overshoot is located at the instant $t_{\rm os}$ if the value given by (23) is bigger than DT_s, and its magnitude, according to (24), depends on both capacitance C and ESR values. If $t_{\rm os} \le DT_s$, then the peak of the output voltage overshoot is located at DT_s (the same instant where the load step occurs), and its amplitude is $\Delta v_{o\,{\rm os\,max}} = \Delta I_{o\max} ESR$. The maximum value of ESR for the overshoot peak of capacitor voltage lying within the regulation window is determined by solving different equations, depending if the overshoot instant

$t_{\rm os}$ is equal or greater than the load step instant $t_{\rm LT}$. In the first case, the equation to solve is

$$\Delta V_{\rm oreg} - \Delta V_{\rm oacc} + V_o = ESR\Delta I_{o\max} + \nu_o(DT_s) \quad (25)$$

otherwise, the equation to solve is

$$\Delta V_{\rm oreg} - \Delta V_{\rm oacc} + V_o = \nu_o(t_{\rm os}). \quad (26)$$

A singular condition occurs when $dv_o(t)/dt$ at $t_{\rm os}$ is equal to zero. The locus of points in the ESR–C plane for which this occurs is obtained by putting $t_{\rm os} = DT_s$ in (23), i.e.,

$$T_s\left(\frac{1}{2}(1+D) + \frac{D'}{r}\right) - ESRC = DT_s. \quad (27)$$

By solving the system of equations (25)–(27) in the Maple environment with respect to ESR yields the following, which provide the maximum ESR as a function of capacitance C, thus allowing to identify which commercial capacitor is suitable for the load-transient regulation

$$ESR_L = \frac{\sqrt{D'\left(2rR_{\rm LT}f_sC - (1+r)D' - \frac{1}{12}r^2(1+D)\right)}}{rf_sC} \quad (28)$$

$$ESR_H = \frac{1}{2+r}\left(2R_{\rm LT} + \frac{r(1-2D)}{6f_sC}\right) \quad (29)$$

$$ESR\cdot C = \tau_s'\left(\frac{1}{r} + \frac{1}{2}\right) = \tau_{\rm crit} \quad (30)$$

where τ_s' is defined in (9) and

$$R_{\rm LT} = \frac{\Delta V_{o\max}}{\Delta I_{o\max}}. \quad (31)$$

The three curves cross at the following boundary value of capacitance C_B:

$$C_B = \frac{1}{f_sR_{\rm LT}r}\left(\frac{r^2}{12}(1+D') + D'(1+r)\right). \quad (32)$$

Fig. 11 shows the plots of the curves given by (28)–(30) for $\Delta i_{\rm Lpp} = 50\% I_o$. The union of the dotted and straight lines represents the upper limit for the ESR. In (29), the first term, which does not depend on C, dominates the second one, so that the behavior of ESR_H seems to be not affected by C.

A real capacitor whose values of ESR and C correspond to a point located below this curve can be considered suitable to maintain the output voltage within the regulation window in the presence of a step-down load transient. The union of ESR_H and ESR_L curves provides the ABC for capacitors suitable to maintain the output voltage within the regulation window during a step-down load transient. The ABCs for the different values of $\Delta i_{\rm Lpp}$ from 10% to 100% I_o are shown in Fig. 12, together with the couples of values $\{ESR, C\}$ taken from a capacitor manufacturer's parameters list. The plots of Fig. 12 highlight the fact that, as the ripple increases, the feasibility curve moves downward and leftward. Consequently, capacitors with higher capacitance are needed if the inductance of the inductor is big, whereas capacitors with smaller ESR are needed if the inductance of the inductor is small. A simple

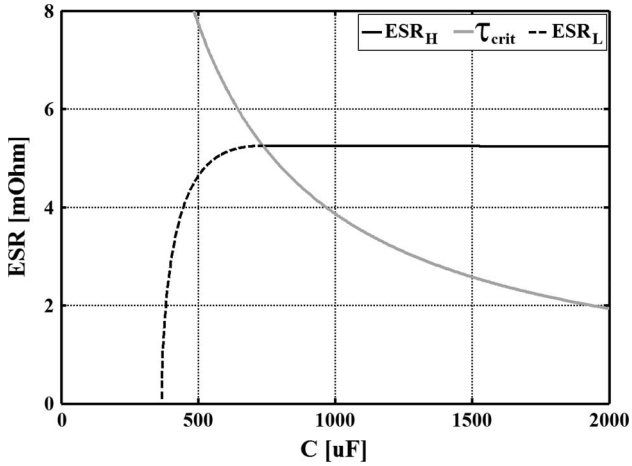


Fig. 11. ABC and $\tau_{\rm crit}$ for $\Delta i_{\rm Lpp} = 50\%\ I_o$.

explanation of this comes from the fact that big inductance makes the interval of time longer, during which the capacitor has to sink/source the unbalance of current between the load and inductor after load transients.

Operating higher inductor current ripple means smaller *inductance,* but this does not necessarily correspond to smaller size *inductor*: High peak current requires higher saturation current and involves higher core loss. Thus, the choice of inductor current ripple is a crucial point.

The curves in Fig. 12 help in understanding the impact of inductor current ripple on the output capacitor's size: They can be used to select the most convenient capacitor within a family or type of components of interest. A real capacitor is suitable for operating conditions corresponding to ABC under which it is located. Since each curve corresponds to a given inductor current ripple, all capacitors located under a curve are suitable only for the values of inductor current ripple smaller than the ripple corresponding to that curve. More capacitors in parallel can be necessary to fit with $ESR_{\max}$ versus $C_{\min}$ boundary curve. Same capacitance and resistance values can also be obtained by means of different parallel combinations. Fig. 12 shows two alternatives in evidence: to take either ceramic capacitors, having smaller ESR and C, or OS-CON capacitors, having bigger ESR and C. Choosing one solution rather than the other is dictated by cost, size, and impact on the dynamic behavior of converter (small ESR ceramic capacitors require more careful feedback control design to avoid instability). The curves show that the ceramic capacitor is suitable above a minimum current ripple $\Delta i_{\rm Lpp,min}$, corresponding to the value for which the couple of values $\{C, ESR\}$ of capacitor individuates a point lying on the boundary curve: For a current ripple smaller than such a minimum value, the boundary curve moves rightward, and the capacitor is no longer suitable. The OS-CON capacitor, instead, is suitable below a maximum current ripple $\Delta i_{\rm Lpp,max}$, corresponding to the value for which the couple of values $\{C, ESR\}$ of capacitor individuates a point lying on the boundary curve: For a current ripple bigger than such a maximum value, the boundary curve moves downward, and the capacitor is no longer suitable. The values of $\Delta i_{\rm Lpp,min}$ and $\Delta i_{\rm Lpp,max}$ can be calculated by inverting either (28) or (29), depending if the capacitance C is smaller or bigger

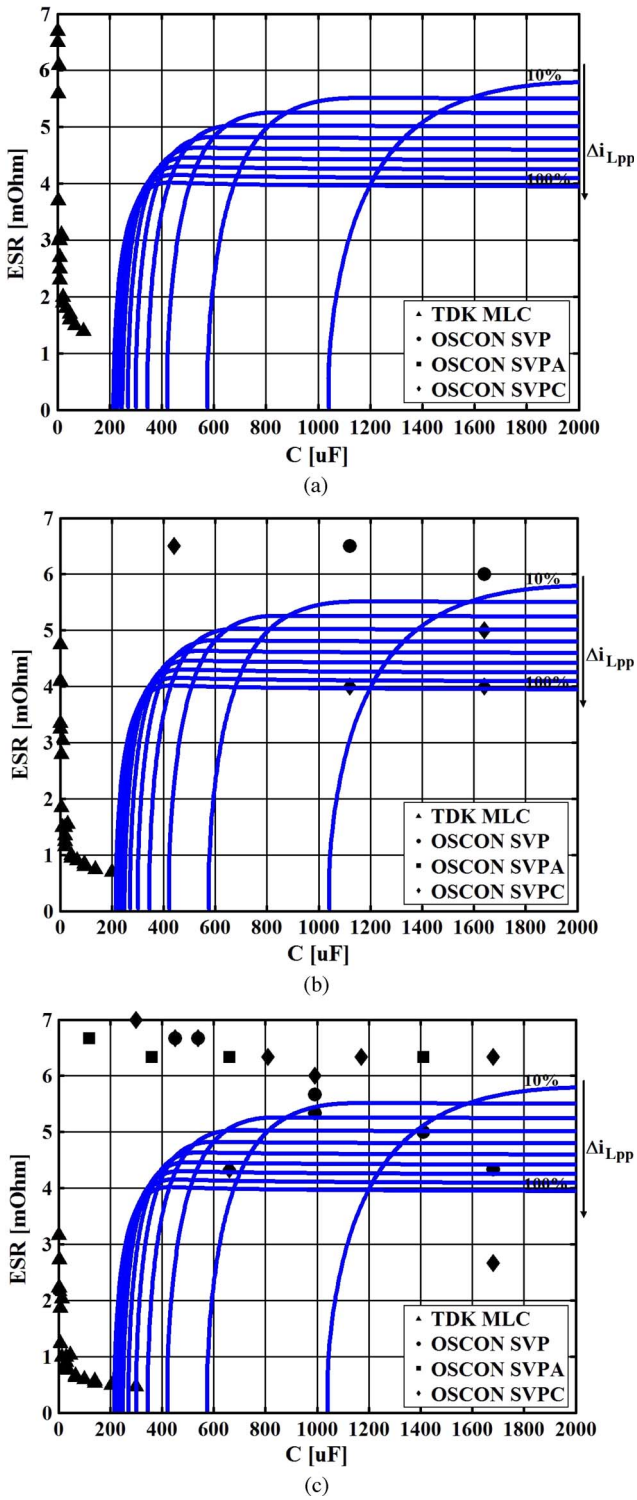


Fig. 12. ABC with real capacitor data. (a) Single capacitor. (b) Two capacitors in parallel. (c) Three capacitors in parallel.

than C_B, respectively. Similar to the case of ripple-based design illustrated in Section II, the ABC equations (28)–(30) can be used for a straightforward selection of the smallest capacitor complying with the design specifications regarding the operating parameters $\{V_i, V_o, I_o, f_s, \Delta I_{o\max}, \Delta V_{\text{oacc}}\}$ and the allowed output voltage regulation window ΔV_{oreg}, for any given inductor current ripple $\Delta i_{\text{Lpp}} \in [\Delta i_{\text{Lpp}\min}, \Delta i_{\text{Lpp}\max}]$. Given the set of commercial capacitors of interest ordered by

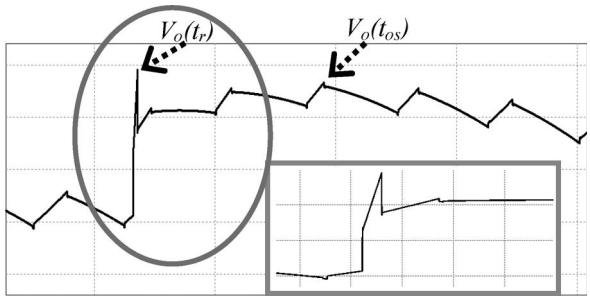


Fig. 13. Output voltage.

increasing capacitance, the following procedure can be used for any Δi_{Lpp} from $\Delta i_{\text{Lpp}\min}$ to $\Delta i_{\text{Lpp}\max}$.

1) Pick the smallest capacitor in the set.
2) Calculate the time constant $ESR \cdot C$ of the capacitor.
3) Calculate the maximum value $ESR_{\max}$ allowed for the capacitor, depending on its capacitance C, according to (28) or (29), depending on the time constant $ESR \cdot C$ of the capacitor.
4) If the ESR of the capacitor is smaller than $ESR_{\max}$, stop the search, and take that capacitor; otherwise, pick the next capacitor, and go to step 2).

The effect on the output voltage determined by the ESL of the output capacitor and by the inductance of the printed circuit board trace can be also accounted for in the approach proposed in this paper. The resulting effect of the total inductance L_{esl} is a sudden spike or droop when a change in the output current slope occurs. It makes sense to consider the effect of stray inductances only if the real slew-rate SR of the load-current transition is known. When a load-current variation with a given slew-rate SR occurs, the joint effect of the ESR and L_{esl} consists in rising the output voltage at

$$\Delta V_o(t_r) = \Delta I_{o\max} ESR + L_{\text{esl}} SR \tag{33}$$

at the instant $t_r = t_{\text{LT}} + \Delta I_{o\max}/SR$. After the instant t_r, the output voltage evolves in the time like if there was no ESL, as shown in Fig. 13. Thus, the load-transient condition is met if the capacitance C and resistance ESR of the capacitor and the total stray inductance L_{esl} of capacitor and traces are such that both conditions $\Delta V_o(t_r) < \Delta V_{o\max}$ and $\Delta V_o(t_{\text{os}}) < \Delta V_{o\max}$ are fulfilled. The effect of L_{esl} can be accounted for in the selection of the output capacitor by means of the following additional constraint for $\text{ESR}_{\max}$:

$$ESR_{\max} = \frac{\Delta V_{o\max} - L_{\text{esl}} SR}{\Delta I_{o\max}}. \tag{34}$$

The search algorithm for the selection of the minimum capacitance is the same as before, just taking the minimum value of $ESR_{\max}$ between the ones given by ABCs and constraint (34).

As L_{esl} is often not known, (34) can also be used to determine the maximum allowed $L_{\text{esl}\max}$ compatible with the ESR of a capacitor selected with the algorithm not including the L_{esl}

$$L_{\text{esl}\max} = \frac{\Delta V_{o\max} - ESR \Delta I_{o\max}}{SR}. \tag{35}$$

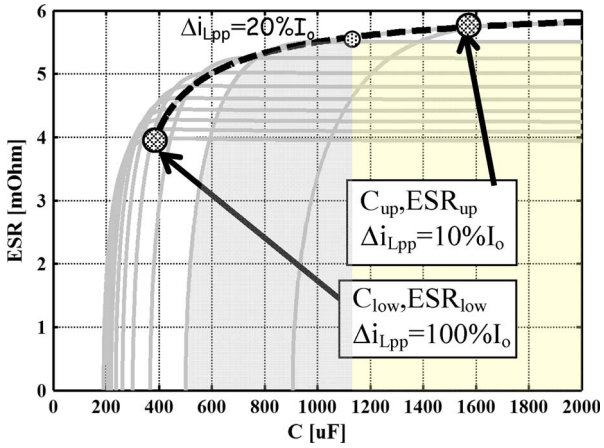


Fig. 14. ABC with UBC.

IV. UBC

To simplify the exploration of acceptability region for output capacitors, a UBC can be determined by assuming that the ESR component of voltage surge is equal to the voltage regulation window amplitude, namely, $ESR\Delta I_{o\max} = \Delta V_{o\max}$. This assumption corresponds to having $t_{\rm os} = DT_s$. At $t_{\rm os} = DT_s$, the curves (28)–(30) cross, thus assuming the same value $ESR_H = ESR_L = \tau_{\rm crit}/C$. The solution of one of the previous equalities provides the maximum ESR and the minimum C for the load-transient specification is met, as functions of the normalized current ripple $r = \Delta i_{\rm Lpp}/\Delta I_{o\max}$

$$ESR_{\max} = \frac{(2+r)R_{\rm LT}}{2\left(1+r+\frac{1}{12}r^2\left(1+\frac{1}{D'}\right)\right)} \tag{36}$$

$$C_{\min} = \frac{D' + rD' + \frac{1}{12}r^2(1+D')}{rR_{\rm LT}f_s}. \tag{37}$$

The ABC corresponding to the ripple inductor current from 10% to 100% (straight line) is shown in Fig. 14, together with the UBC obtained with the values of $ESR_{\max}$ and $C_{\min}$ given by (36) and (37) in the same range of inductor current ripple (dotted line). The UBC is the locus of intersection points of ESR_H and ESR_L upon $\Delta i_{\rm Lpp}$ variation. The extreme points $\{C_{\rm up}, ESR_{\rm up}\}$ and $\{C_{\rm low}, ESR_{\rm low}\}$ of the dotted curve correspond to the minimum and maximum inductor peak-to-peak current ripples, respectively.

An advantage of the dotted UBC is in the possibility of examining, by means of a single curve, both the impact of the peak-to-peak inductor current ripple value on the choice of output capacitor and the impact of the choice of output capacitor on the acceptable range for the output inductor peak-to-peak current ripple. A disadvantage consists in the possibility of excluding some suitable capacitor because of intrinsic conservativeness underlying the curve itself. For example, looking in Fig. 14 for capacitors such that 20% inductor peak-to-peak current ripple is acceptable, based on the unified dotted curve, the components staying within the light yellow shaded area only are suitable. Nevertheless, considering the specific boundary curve associated to 20% current ripple, also capacitors staying within the light gray shaded area are acceptable: Using the dotted unified curve involves cutoff of all acceptable "smaller" capacitors staying within the light gray shaded area. If an optimal design is sought (minimum size of capacitors), using specific current ripple boundary curves might be more convenient, whereas if design robustness and flexibility are sought (more alternative design solutions rather than just a single optimal design solution), using the unified dotted boundary curve is preferable. The convenience in choosing high-current ripple can be reasonably evaluated only if the inductor design is jointly considered. In general, it is quite rare to find a capacitor whose values of C and ESR are such that the corresponding points lie exactly "on" the dotted curve. Thus, more likely, a designer has to look for real capacitors staying "under" the dotted curve. Of course, the preferred capacitors are those ones staying as close as possible to the dotted curve, with a maximum ratio $r_C = ESR/C$, which is a figure of merit of the capacitor's size (higher r_C means smaller capacitor). Given any capacitor below the dotted curve, it is possible to determine the minimum and maximum inductance ripple limits bounding the range of possible values of output inductor inductance, which can be calculated by means of (38) and (39), shown at the bottom of the page.

V. Comparison Between Traditional and ABC-Based Design Approaches

In Fig. 15, the ABC, UBC, and the boundaries generated by means of the traditional design approach (40)–(42) are plotted together

$$L_{\min} = \frac{(V_i - V_o)DT_s}{\Delta i_{\rm Lpp}} \tag{40}$$

$$ESR_{\max} = \min\left(\frac{\Delta\nu_{\rm opp}}{\Delta i_{\rm Lpp}}, \frac{\Delta V_{o\max}}{\Delta I_{o\max}}\right) \tag{41}$$

$$C_{\min} = \max\left(\frac{L\Delta V_{o\max}}{ESR_{\max}^2 V_o} + \frac{D'}{2f_s ESR_{\max}}, \frac{\Delta i_{\rm Lpp}}{8f_s\Delta\nu_{\rm opp}}\right). \tag{42}$$

By assuming $\Delta i_{\rm Lpp} = 40\%\ I_o$, we have an $L_{\min}$ of 405 nH, $ESR_{\max} = 4.6\ \ \Omega$, and $C_{\min} = 859\ \ \mu$F. The values of

$$L_{\min} = \frac{V_o D'(D-2)ESR}{f_s\Delta I_{o\max}\left(3D'(2ESR - R_{\rm LT}) - \sqrt{12\left(ESR(ESR-R_{\rm LT})(1-3D+2D^2) + \frac{3}{4}R_{\rm LT}^2 D'^2\right)}\right)} \tag{38}$$

$$L_{\max} = \frac{V_o D'(D-2)}{f_s\Delta I_{o\max}6\left(D' - R_{\rm LT}f_s C + \sqrt{R_{\rm LT}f_s C(R_{\rm LT}f_s C - 2D') + \frac{1}{3} - D + \frac{2}{3}D^2}\right)} \tag{39}$$

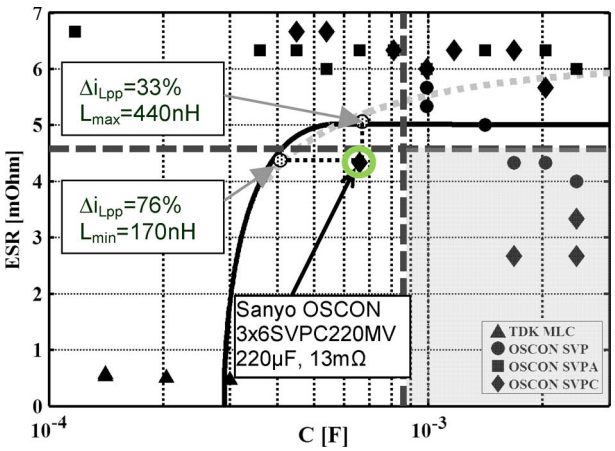


Fig. 15. Choice of a real capacitor below UBC.

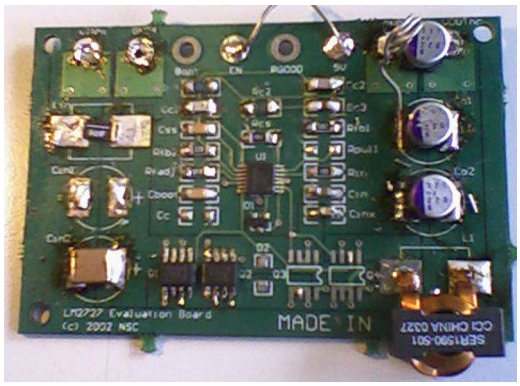


Fig. 16. Experimental board. $V_i = 3.3$ V, $V_o = 1.1$ V, $I_o = 8$ A, $\Delta V_{\text{oreg}} = 5\%$ of V_o, $\Delta V_{\text{oacc}} = 1\%$ of V_o, $f_s = 530$ kHz, $L = 0.5$ μH. 3×Sanyo OSCON-6SVPC220MV 220 μF, 13 mΩ.

$ESR_{\max}$ and $C_{\min}$ obtained are shown in Fig. 15 as the dashed bold black lines. The shaded region, where $ESR < ESR_{\max}$ and $C > C_{\min}$, is the corresponding acceptability region: This means that the traditional approach leads to oversized capacitors with respect to the one, circled in green, that can be chosen according to the proposed approach. The selected capacitor, circled in green in Fig. 15, allows operation with a range of peak-to-peak inductor current ripple from 14% to 100%, corresponding to the following inductance acceptability range [127, 901 nH]. It should be noted that the unified ABC always provides better design constraints with respect to the traditional design based on separate constraints on ESR and C. Fig. 16 shows the picture of the National Semiconductor evaluation board, including the buck-SR voltage-mode controller LM2727 used for experimental verifications, where the mounted power components have been selected according to the methodology discussed in this paper. Fig. 17(a) and (b) shows the measured surges in the output voltage determined by 10% to 100% step-up and 100% to 10% step-down load transients, respectively: The design constraints are fulfilled if the parameter values are designed according to the proposed approach. The voltage-mode control of the converter has been designed to achieve 45-kHz crossover loop gain, which is sufficiently high to guarantee that the voltage surge is not increased because of

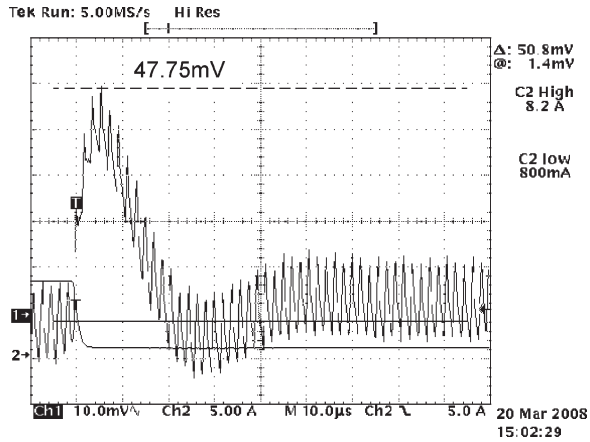


Fig. 17. Experimental measurement for the step-down load-transient overshoot.

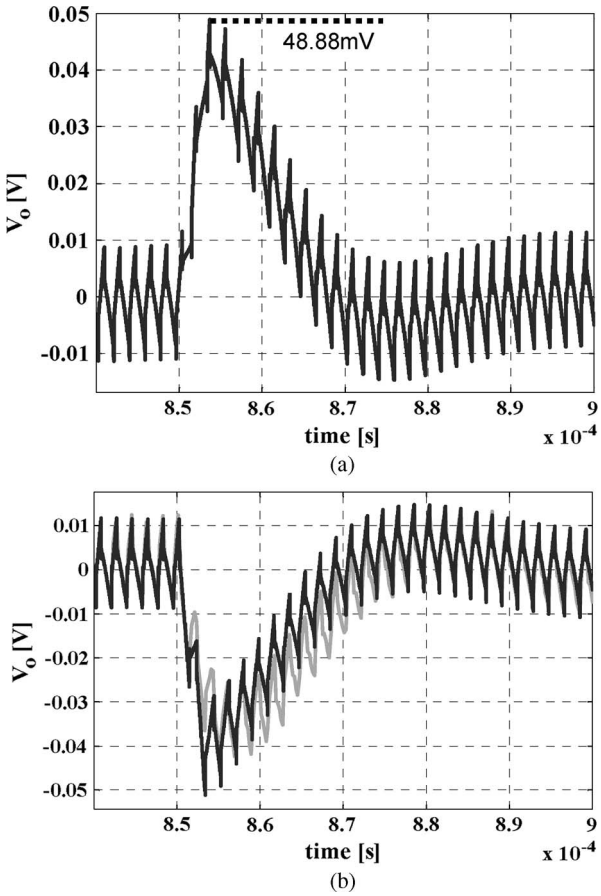


Fig. 18. (a) Simulation result for the step-down load-transient overshoot. (b) Comparison between (black line) simulation result and (gray line) experimental measurement for the step-up load-transient undershoot.

slow controller reaction, according to the assumptions made in Section III. Figs. 18 –20 show the excellent agreement between experimental measurements and simulation results.

VI. Conclusion

A unified analysis of output filter design equations for the buck-SR converter has been presented in this paper. The constraints for ripple and load-transient surge limiting have been

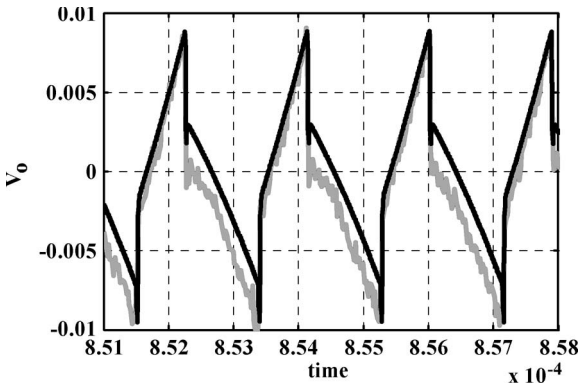


Fig. 19. Comparison between (black line) simulation result and (gray line) experimental result for steady-state output voltage ripple.

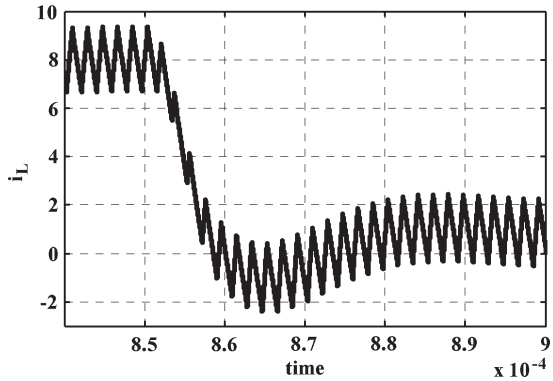


Fig. 20. Inductor current during step-down load transient.

integrated into a single equation defining an ABC, which relates minimum capacitance to maximum series resistance and which can be used to quickly figure out the commercial capacitors suitable for the design. The main benefits of the proposed method consist in the possibility to reduce the size of output capacitor, owing to the exact calculation of its transient and ripple behavior and to the consideration of the correlation existing between the series resistance and capacitance of the real components and between these parameters and the actual characteristics of the transient and ripple waveforms.

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